Design of a High Speed Communications Link Using Field Programmable Gate Arrays

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Introduction

A communication mechanism has been developed using two 8000 gate Field Programmable Gate Arrays (FPGAs). This mechanism was developed to provide high speed, serial communication between shelf processing units in a hierarchical control system. The mechanism provides the higher level processing board with a virtual memory link to the lower level processor boards. The link provides memory-to-memory transfers between the two processing tiers. The FPGAs are master/slave devices which provide the physical link across the backplane and access to the local memory on each unit. Multiple types of transactions can be sent across the link from the master to one or all of the slave devices on the bus. Each FPGA contains internal registers used to configure the devices for the desired transaction, a mechanism to do DMA transfers to and from the unit's memory, and a mechanism to transfer and receive serial data over the link. This paper concentrates on the board where the master FPGA resides, Satellite Processor (SPB).

System Description

SPB is a second tier module that provides the communication interface between the top level Processing System and the third tier Processor Elements for I/O modules and for matrix modules. The satellite processor is the second-level controller that resides in each shelf of the SI48 end stage and center stage shelf. It functionally provides the necessary Operation, Administration, Maintenance, and Provisioning (OAM&P) and protective switching. It distributes control to the third level (smart circuit cards) and controls the functions required of the dumb circuit packs, such as the Internal Protection (IPB 101) board. Figure 1 is a typical 1631 SX application system diagram.

Functional Overview

Figure 2 is a functional block diagram of the satellite processor. Each component is briefly described in the following paragraphs.

Central Processing Unit and Memory

The main processor is a 32-bit embedded microprocessor. A multitask real-time operating system handles the primary processing functions. The processor controls all functions and supports memory read/write access, fault detection, and interrupt control. The processor contains three types of memory: EPROM, local RAM, and system parameter RAM. The flash EPROM has asynchronous access via 16 bits of the available 32-bit data bus. It is used for power-up operations. Local RAM is addressed at 20 MHz over a 32-bit address bus, and data is exchanged over a separate 32-bit data bus. Local RAM includes real-time operating system, communications driver, application program, application data, and exception vector. The SPB has two Communication Controllers (CC) with system and parameter RAM. The main processor accesses both CCs via 16 bits of the available 32-bit data bus. Each CC has an associated parameter RAM for internal use.

Communication Controllers

The Communications Controller each provide a redundant HDLC interface (A and B) to the lower level processors and a redundant ACL bus to the top level processor. This includes fault recovery software that uses the other CC as a communication path to check the database of a failed satellite processor to reconfigure the new active partner processor if a failure occurs. CC1 and CC2 are initialized in the asynchronous mode to provide debug capability via a front-panel connector. Also, an HDLC communications link exists between the partner processors for data synchronization.

A system Integration Block (SIB) is part of each CC. They are called SIB-CC1 and SIB-CC2. SIBs control the following functions:

- Parallel I/O ports
- Timer
- Watchdog timer
- DMA interrupt controller
- Chip-select lines and wait-state generator logic
- On-chip clock generator with output signal

The SPB contains up to 12 general purpose inputs and 13 general purpose outputs, including the Card Presence Indicator (CPI), which is used to control dumb boards and provide alarm detection or activation of service control. The

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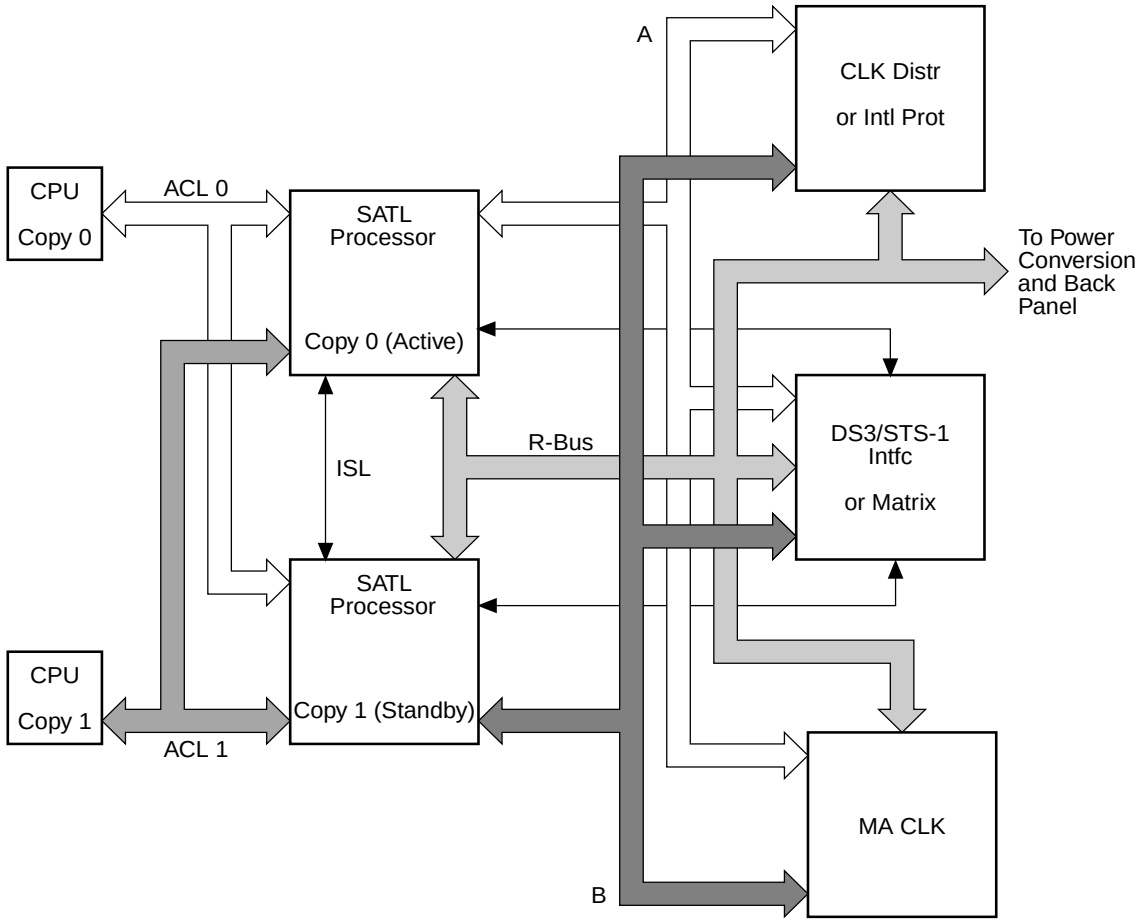

Figure 1 • *System Application Block Diagram*

CPI allows the top level processor to poll a missing satellite processor. This allows the top level shelf to determine if any satellite processors are not responding with an out-of-state switch failure or fuse failure response.

Arbiter

The bus arbiter prioritizes CC1s and CC2s Serial Direct Memory Access (SDMA). The arbiter allows multiple SDMA transfers to be multiplexed onto the common processor bus to access local RAM and different system and parameter RAM. It also allows Independent Direct Memory Access (IDMA) from the CCs and from the master FPGA.

CPU-CC Bus Adapter

The CPU-CC bus adapter logic circuit ensures full local RAM access for SDMA and IDMA of the CC controllers. It provides a 16- to 32-bit-wide bus adaption. The master FPGA has a 32-bit-wide interface to the main processor.

Interrupt Request Handler

The interrupt request handler responds up to 48 service request sources that are generated on the various user boards within a twin shelf. Any interrupt request within a shelf group of 24 board elements generates a fast board protection switch.

Memory Transfer Controller

The Memory Transfer Controller uses two redundant buses (copy 0 and copy 1) to access user boards and support protection switching. The Memory Transfer interfaces bus interfaces with third tier processors in the I/O and matrix shelves. This bus is a high-speed serial communication interface between the satellite processor and transmission circuits packs. The bus provides serial DMA transfers for a data rate faster than the HDLC link. This bus is used primarily for protection switching in the event of a system failure.

IIC Controller Section

The Remote Inventory link (called the RI-bus) provides access onto the remote inventory data bank (256- by 8-bit Electrically Erasable Programmable Read Only Memory [EEPROM]) implemented on each circuit pack, such as

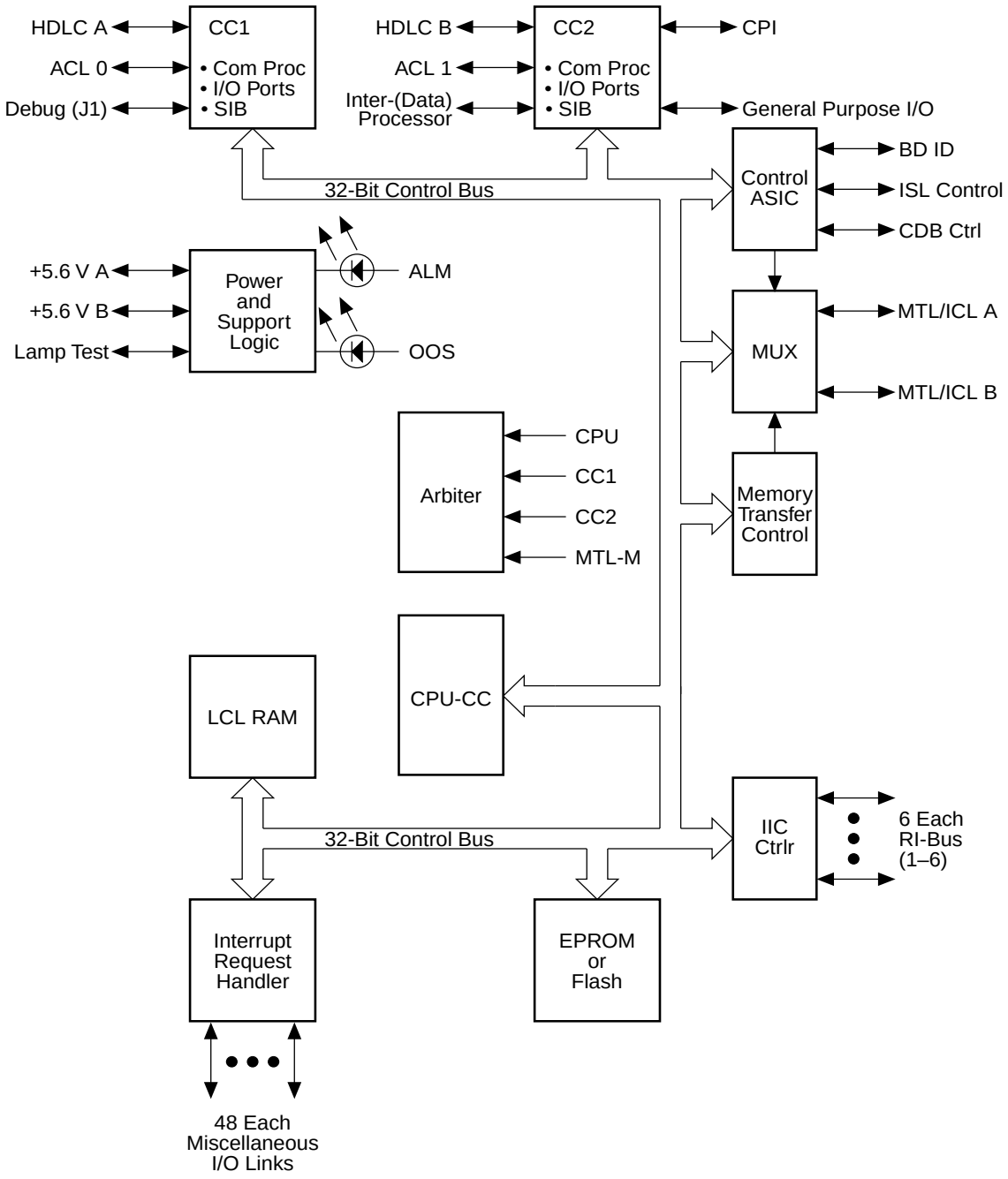

Figure 2 • *SPB Functional Block Diagram*

power converters, back panels, and user boards (with or without processors). Each SPB has one controller for each of the six bus blocks on the module. The IIC controller has an 8-bit processor interface and provides the R-bus master and slave function. It controls all sequencing, protocol, arbitration and timing.

Power Supply Circuit and Support Logic

The processor circuit pack is connected to two redundant 5 V power converters (copy 0 and copy 1). Each is C-sourced and fused. A reset circuit monitors the voltage at the input. In the event of low voltage, the ALM indicator lights and a power-on reset is generated. A blown fuse on the processor does not cause loss of service in the twin shelf.

The support logic provides the functions to access memory, level shifting to external interfaces and voltage supervision.

FPGA Implementation

Figure 3 is a block diagram of the circuitry implemented within the master FPGA. This FPGA is an Actel A1280-1 in a 160 pin Plastic Quad Flat (160PQFP) package.

The A1280 is an 8000 gate device which provided the design group with the capacity to fit a large amount of circuitry in a single chip and a small board space. Also, the low power consumption of the A1280-1 was an attractive feature. The slave FPGA on the third tier processing card is another A1280 with similar functionality.

The FPGA implementation started with drawing the schematic of the circuit using Viewlogic's schematic capture tool. Another tool used during FPGA implementation was ACTgen. ACTgen is a computer-aided engineering (CAE) tool, included with Actel's Designer software. With ACTgen's graphical user interface, we were able to build structured macros (counters, adders, etc.) by simply clicking on a few menu choices. ACTgen then creates functions that are optimized for Actel architecture. The shift registers and the 24-bit counters in this design were generated with minimal effort and no simulation effort using ACTgen.

Once all the blocks were generated and the top level hierarchical schematic was drawn, a functional simulation verified correct functionality of the design. The design was then netlisted into Actel Design Language (ADL). The pin assignment for this design was fixed before the FPGA design was initiated. This meant that the Actel's Automatic Place and Route program was not allowed any flexibility to move the pins around. Additionally, the A1280 was used to its near maximum capacity at 98% utilization. Nevertheless, the Automatic Place and Route program completed the FPGA layout. Once the chip layout was finalized, the delays were extracted and a post-layout simulation was performed. The same test vectors used in functional simulation were used in the post-layout simulation. The required system speed of 25 MHz was easily achieved and the FPGA was sent to be programmed for production.

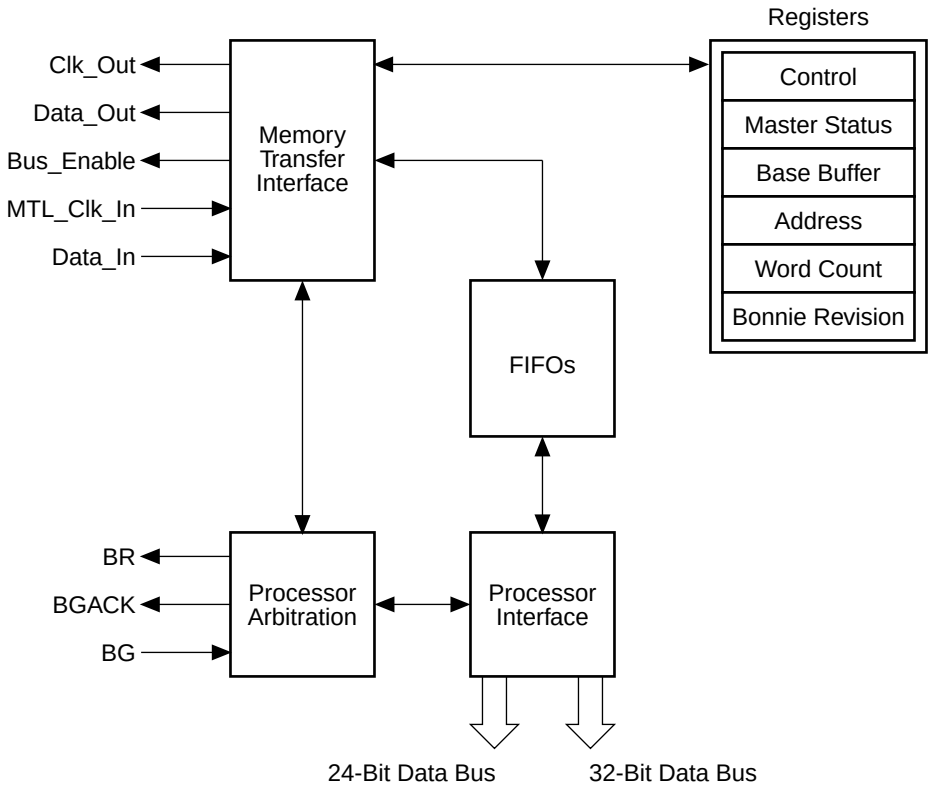

Figure 3 • *FPGA Implementation Block Diagram*

Conclusion

The Memory Transfer link was designed to provide high speed communication between processing units in a control system. FPGA technology was used in this project which provided a number of advantages. The density of the FPGA allowed considerable savings in board area. Most importantly, the FPGA provided tremendous flexibility for the design group. The FPGA chip layout was not even completely defined when the SPB board was layed out. A1280 allows this flexibility due to its architecture and abundant routing resources. Even at 98% utilization and with locked pin assignments and a few design change iterations, the FPGA was placed and routed with no problems.