For:sanjay
Printed on:Mon, Sep 7, 1998 14:01:42

Document:lab2
Last saved on:Mon, Sep 7, 1998 13:58:21

Lab 2: Static Load Inverters

Introduction

The purpose of this lab is to familiarize the students with the characteristics of static load inverters. You are to use spice as a 'testbench' for measuring the characteristics of these inverters, and then explain in the question portion what causes these inverters to act in the way that they do.

Static Load Inverters

The first thing to do is to create spice netlist file for each of the static load inverters. For all of the following circuits, the length of all NMOS and PMOS devices should be 0.6u. At NO point should device widths be less than 1.2u. Set the initial values of the nmos and pmos widths to those mentioned in each sub section. Set Vdd=3.3 volts. After creating the netlist file, you need to create the stimulus file for providing inputs to your circuit and making measurements. Copy the file ~sanjay/EE4253/lab2/default.sp to the directory where the spice netlist was created. Modify this file to also measure the following values:

1. Switching point (your first lab had an example of this)
2. Lowest output value when input = Vdd.
3. Highest output value when input = 0v.
4. DC current when input = Vdd.
5. DC current when input = 0v.
6. Resistance of the load element when input = Vdd.

For each inverter, you will need to produce a plot as described below.

PMOS Static Load Inverter

Simulate a PMOS Static load inverter (Gate tied to Vss) with PMOS width = 2.4u and NMOS width = 1.2u. Note that these 'W' values make for a fairly lousy inverter.

Find new 'W' values such that the constraints listed on next page are satisfied. Record your new DC values as well as the new 'W' values.

NMOS Enhancement Load Inverter

Simulate an NMOS enhancement load inverter (load is NMOS with Gate & Drain tied to Vcc) with the same 'W' values you ended up with on the PMOS static load inverter.

Find new 'W' values for the transistors such that the constraints listed on next page are satisfied. Record your new DC values as well as the new 'W' values.

Resistive Load Inverter

Create a resistive load inverter (the load element is a resistor). To choose a value for the resistor, look at the 'load resistance' plot that you produced for the static load PMOS inverter. Use the resistance value for Vin=Vcc as the load resistor value (if the PMOS effective resistance produced a good static PMOS inverter, then it should also be a good load value for this resistive load). The starting 'W' value for the NMOS pulldown should be the value you ended up with for the PMOS static load inverter.

Find new 'W' values such that the constraints listed below are satisfied. Record you DC measured values as well as the new 'W' values.

Constraints

These are the constraints to be met when adjusting W values:

1. Absolute values of both Noise margins > 0.33v (10% of Vcc)
2. Absolute value of gain > 10
3. Switching point between 1v and 2.0v.

If you can't meet all of the constraints, then sacrifice the constraints in the following order:

1. One of the Noise margins can be reduced to > 0.17 (5% of Vcc)
2. The switching point can be widened to 0.66v and 2.3v

Some of the inverters will be able to meet all of the constraints, others will not. Do your best.

Output Plot

For each inverter, when you arrive at the final W values, create a plot that has three panels. The three panels should plot Vin vs. Vout, Load resistance vs. Vin (the drain current will be near zero for certain ranges which will cause DC convergence problems if you try to calculate a resistance value), and drain current(of load) vs Vin.

You will need to use the "Set Zoom" command in MWAVES in the 'Load resistance' panel to set the Y axis to a reasonable range (select the panel, then click right and hold to get the local menu). The load resistance may vary WIDELY; you should set your Y–axis value so that the maximum Y–axis value is 100K.

Answer the following questions.

Important! Most of your grade will depend on how you answer these questions. Please make your answers brief and to the point.

1. Rank the inverters by how well they satisfied the constraints.
2. If an inverter was unable to satisfy all constraints, discuss why.
3. In general for the static inverters, if the effective resistance of the load is held constant (the W is held constant), and the width of the NMOS pulldown is INCREASED, what happens to the noise margins?
4. You measured the effective load resistance of the load device for the static inverters. From your DC measurement information, COMPUTE the effective 'on' resistance of the NMOS pulldown device when Vin = Vcc for each static load inverter. Show your Work.
5. From the drain current plots, discuss which inverters consume DC power and explain what conditions are necessary for this to happen. Rank the inverters in terms of DC current consumed (less is better).
6. Which inverters could NOT pull the output all the way up to Vcc. Why not?
7. Which inverters could NOT pull the output all the way down to 0v. Why not? What could be adjusted in the circuit to make the output go closer to 0v?

To Turn In

1. Final W,L values and DC measured values for each of the 3 inverters . Put the results for each inverter one below the other on a single page. Present the DC measurements in a neat tabular format. DC measured values should include 1–6 values on first page and also voh, vih, vol, vil, nm_l, nm_h and max_gain.
2. Attach for each of the inverters the spice stimulus file, spice circuit file and the plot, in that order.
3. Answers to the questions. Please type out your answers.