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Lab3: CMOS Inverter Using Schematic Entry

Introduction

The purpose of this lab is to introduce the student to the Cadence design system for schematic entry and simulation.

Part 1 – Schematic entry of a CMOS inverter

Enter the following schematic into Cadence. This is the inverter from Lab 1. After entering the schematic, extract the netlist and obtain the voltage transfer characteristic. From your simulation determine the switching point and the noise margin for this inverter. Note that for this inverter, VOH = Vcc, and VOL = Vss. Use a Cload value of 10fF. The switching point for this inverter should be close to 50% Vcc.

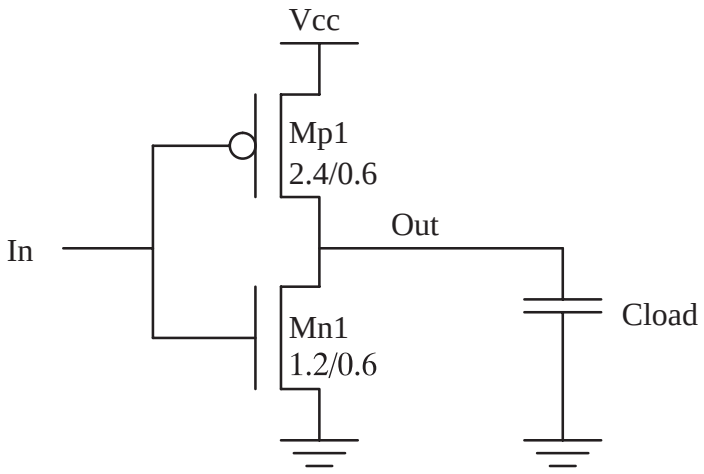

Figure 1. CMOS Inverter

Part2 – VI output characteristic (drain current vs drain–to–source voltage)

Obtain the VI output characteristics for the nmos transistor shown in the inverter above for values of Vgs = 1, 2 and 3v. Mark the linear and saturation regions on your plots.

Part3 – Designing for different switching points

Using the results of the simulation in Part 1, design the inverter for the following two cases

1. For a switching point around 25% Vcc. Also find the noise margin for this case.
2. For a switching point around 75% Vcc. Also find the noise margin for this case.

The power dissipation for both the above designs should be kept minimum.

To Turn In

1. The schematics for parts 1 and 3 and the corresponding transfer characteristics (mark the Vtn and the |Vtp| voltages on your plots)

2. The VI plot for part 2

3. The noise margin and switching point information for parts 1 and 3, in neat tabular column

4. Spice listing for parts 1 and 2

5. Answers to the following questions

a. You are required to design an inverter stage, which will have maximum immunity to noise. How would you design the inverter to achieve this.

b. You are required to set up an nMOS transistor to act as a constant current source. What scheme of biasing would you want to employ to achieve this.