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Lab 4: Complex gates and Static D flip–flop

Introduction

The purpose of this lab is to familiarize the students with complex gates and the D flip–flop.

Complex Gates

Set up the following complex gates in Hspice and verify their functionality:

Z = not (A and ((B and C) or D))
Z =not(A or ((B or C) and D))

Obtain Z for all possible input combinations of ABCD for each complex gate above. Also obtain the plot of the inputs and the output Z for each gate. Use a separate panel to display each waveform but print out all the panels for each complex gate on a single page.

D flip–flop

Set up a positive edge triggered static D flip–flop and verify its functioning.

Obtain the output Q for all possible combinations of CLK and D values. Show all the input and output waveforms on separate panels on a single page.

Transistor sizes

Use minimum gate length of 0.6u for all transistors. Use 1.2u for the widths of all nmos transistors and 2.4u for the widths of pmos transistors. Use VDD = 3.3v.

To Turn In

1. A schematic of your implementation of the complex gates and the D flip flop.
    (a neat hand drawn schematic is acceptable)
2. Your spice stimulus files and circuit files for each.
3. Mwave plots for each circuit as mentioned above.