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Lab 8:Standard Cell Layouts

Objective

To introduce the student to standard cell layouts. In this lab the student will do layouts for a complex gate and a 2–input multiplexer laid out in accordance with the MSU standard cell layout template.

Setup

Create a new library called lab8. Create schematic and layout cellviews for both the complex gate and the 2 – input multiplexer.

Part A: Complex Gate Layout

This part involves creating the layout for a complex gate. First, enter the complex gate design into schematic. Then do a stick layout of your gate before proceeding to the layout. Your stick layout must use an unbroken strip of diffusion for the NMOS and PMOS transistors. Use a 4 lambda width for the NMOS transistors and an 8 lambda width for the PMOS transistors in your layout.

Implement the layout for the function

F = not(A or ((B or C) and D))

Part B: 2–Input Multiplexer Layout

As for part A, enter the schematic and do a stick layout before proceeding to the layout of the 2–input multiplexer. The inputs to the multiplexer are A and B and the output is F. Sel is the control input. If Sel is ’0’ input A is output. If Sel is a ’1’ then input B needs to be output.

Your multiplexer design needs to have drive capability. You need to come up with the transistor sizing for the multiplexer.

Standard cell template rules

1. Cell height is 78 lambda

2. The cell width is a multiple of 8 lambda (there is no maximum). The cell width is determined by the outermost edges of the VCC/VSS rails.

3. Pins must be brought out to M1M2 contacts (via surrounded by minimum size metal 2). Valid X locations for pins are on an 8 lambda grid, where the first position starts at 4 (locations are 4, 12, 20, 28, etc.). The center location of the via must be on this grid. You must also give

the pin the connectivity property of TOP and BOTTOM. To do this, select the pin layer geome try (not the drawing layer), open its properties, and select on connectivity. You will see some selections for access directions. Make sure both Top and Bottom are selected. This also means that any input or output pin layer must be exactly the same size as the drawing layer it is over. The connectivity access direction allows the router to access this terminal from either the top or the bottom of the cell.

4. The power rails are in MET1 and are 10 lambda wide. (The center of the left edge of the VSS power rail is at location (0,0). Since the cell is 78 lambda high, then the center of the left edge of the VCC power rail is at location (0,68 lambda) or (0,20.4) in this technology.)

5. Active (diff and tap), poly, or metal layers (with the exception of the power rails) must be at least 2 lambda from the left and right edges of the cell.

6. Use of MET2 for routing inside the cell must be kept to an absolute minimum (it is preferable that you do not use it at all). If you do use MET2, then it should only be in the vertical direction and on the same grid as the pins.

To turn in

1. Schematic, stick layout and layout plot for Part A

2. Schematic, stick layout and layout plot for Part B

3. Show the schematic for a 2–input multiplexer implementation, if drive capability is not re quired. (use as few transistors as possible)