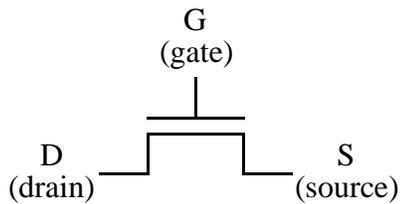


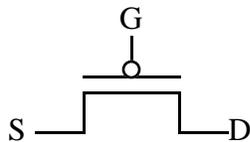
## MOS Transistors as Switches



*n*MOS transistor:

Closed (conducting) when  
Gate = 1 ( $V_{dd}$ , 5V)

Open (non-conducting) when  
Gate = 0 (ground, 0V)

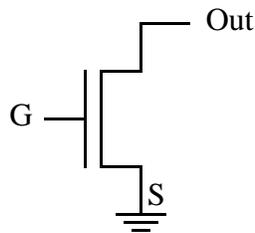


*p*MOS transistor:

Closed (conducting) when  
Gate = 0 (ground, 0V)

Open (non-conducting) when  
Gate = 1 ( $V_{dd}$ , 5V)

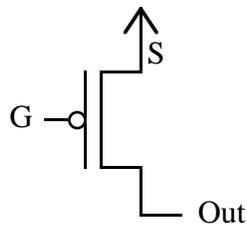
For *n*MOS switch, source is typically tied to ground and is used to *pull-down* signals:



when Gate = 1, Out = 0, (0V)

when Gate = 0, Out = Z (high impedance)

For *p*MOS switch, source is typically tied to  $V_{dd}$ , used to *pull* signals *up*:

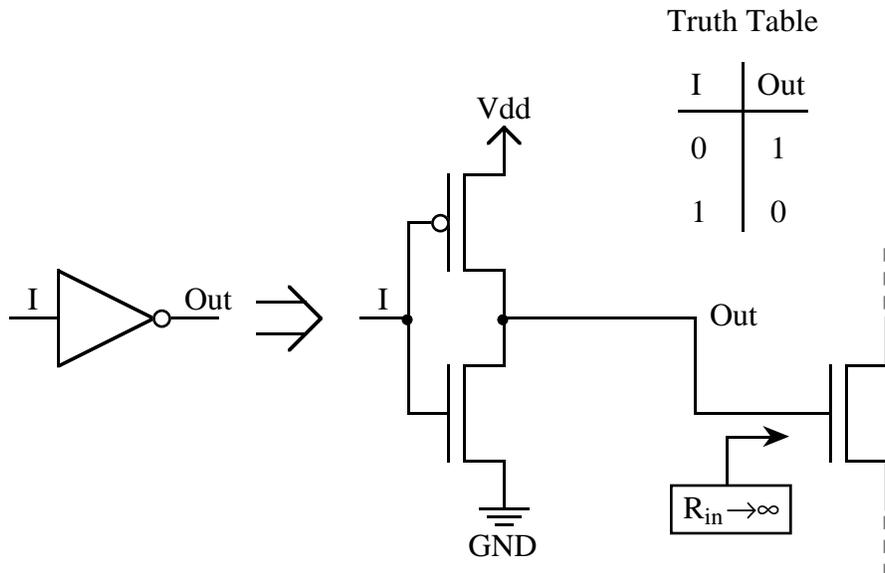


when Gate = 0, Out = 1 ( $V_{dd}$ )

when Gate = 1, Out = Z (high impedance)

Note: The MOS transistor is a symmetric device. This means that the drain and source terminals are interchangeable. For a conducting *n*MOS transistor,  $V_{DS} > 0V$ ; for the *p*MOS transistor,  $V_{DS} < 0V$  (or  $V_{SD} > 0V$ ).

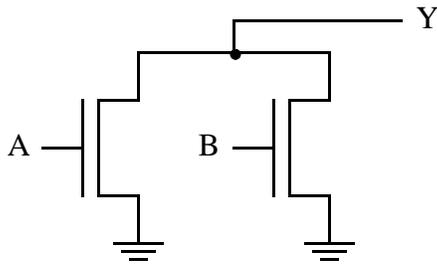
## The CMOS Inverter



Note: Ideally there is no static power dissipation. When "I" is fully *high* or fully *low*, no current path between Vdd and GND exists (the output is usually tied to the gate of another MOS transistor which has a very high input impedance).

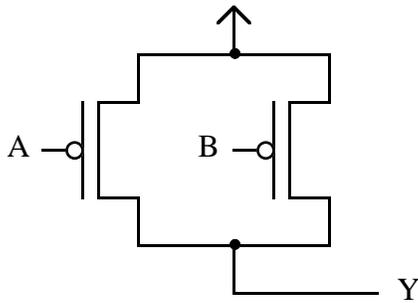
Power is dissipated as "I" transitions from  $0 \rightarrow 1$  and  $1 \rightarrow 0$  and a momentary current path exists between Vdd and GND. Power is also dissipated in the charging and discharging of gate capacitances.

## Parallel Connection of Switches



$Y = 0$ , if  $A$  or  $B = 1$

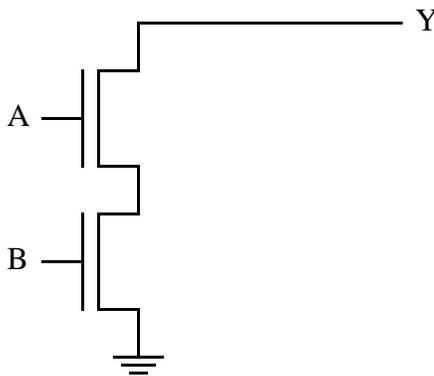
$$\overbrace{\quad}^{\downarrow} \underbrace{\quad}_{A + B}$$



$Y = 1$  if  $A$  or  $B = 0$

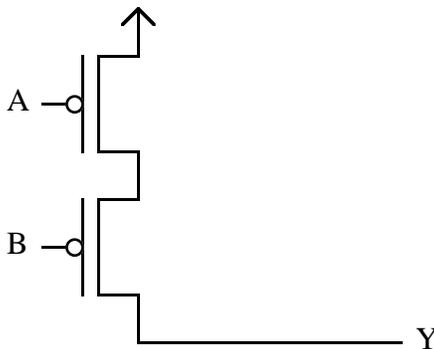
$$\overbrace{\quad}^{\downarrow} \underbrace{\quad}_{\overline{A + B}}$$

## Series Connection of Switches



$Y = 0$ , if  $A$  and  $B = 1$

$$\overbrace{\quad}^{\downarrow} \underbrace{\quad}_{A \cdot B}$$



$Y = 1$ , if  $A$  and  $B = 0$

$$\overbrace{\quad}^{\downarrow} \underbrace{\quad}_{\overline{A \cdot B}}$$

# NAND Gate Design

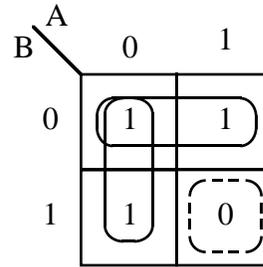
*p*-type transistor tree will provide "1" values of logic function

*n*-type transistor tree will provide "0" values of logic function

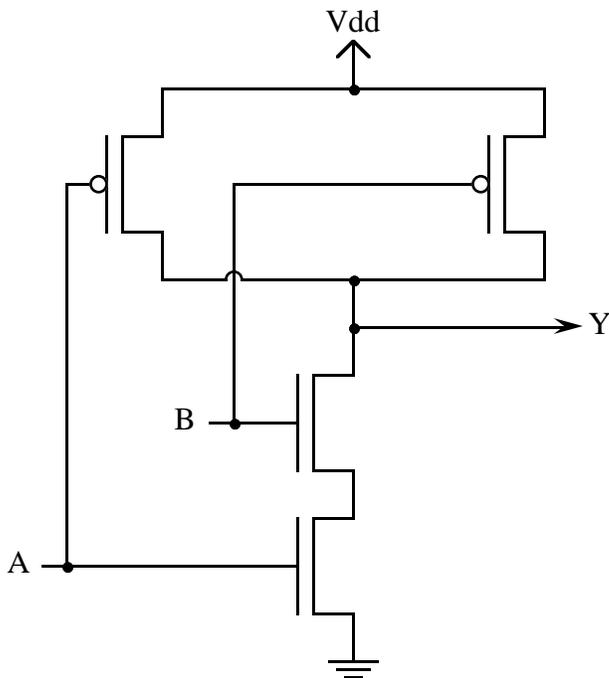
Truth Table (NAND):

AB	
00	1
01	1
10	1
11	0

K-map (NAND):

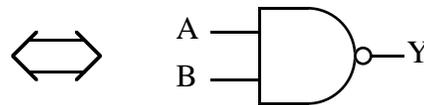


NAND circuit example:



$$P_{tree} = \bar{A} + \bar{B}$$

$$N_{tree} = A \cdot B$$



# NOR Gate Design

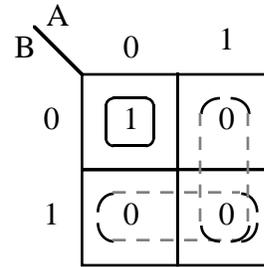
*p*-type transistor tree will provide "1" values of logic function

*n*-type transistor tree will provide "0" values of logic function

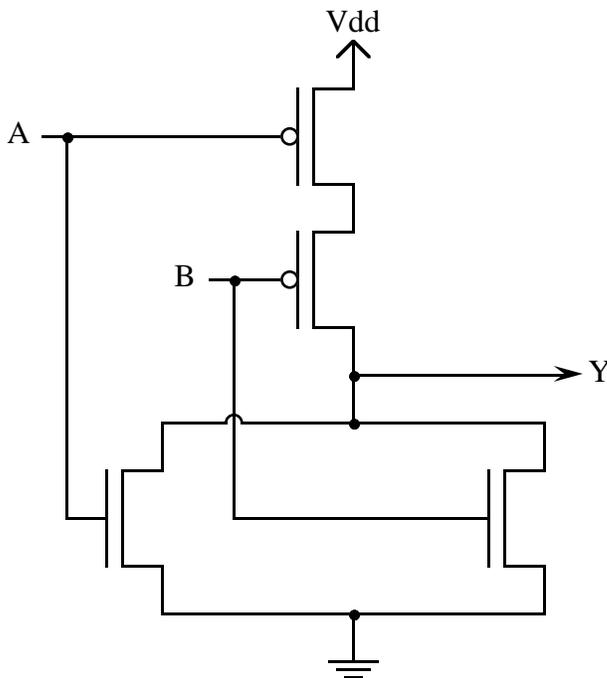
Truth Table:

AB	
00	1
01	0
10	0
11	0

K-map:

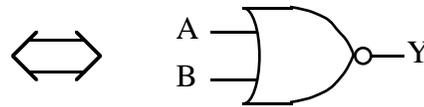


NOR circuit example:

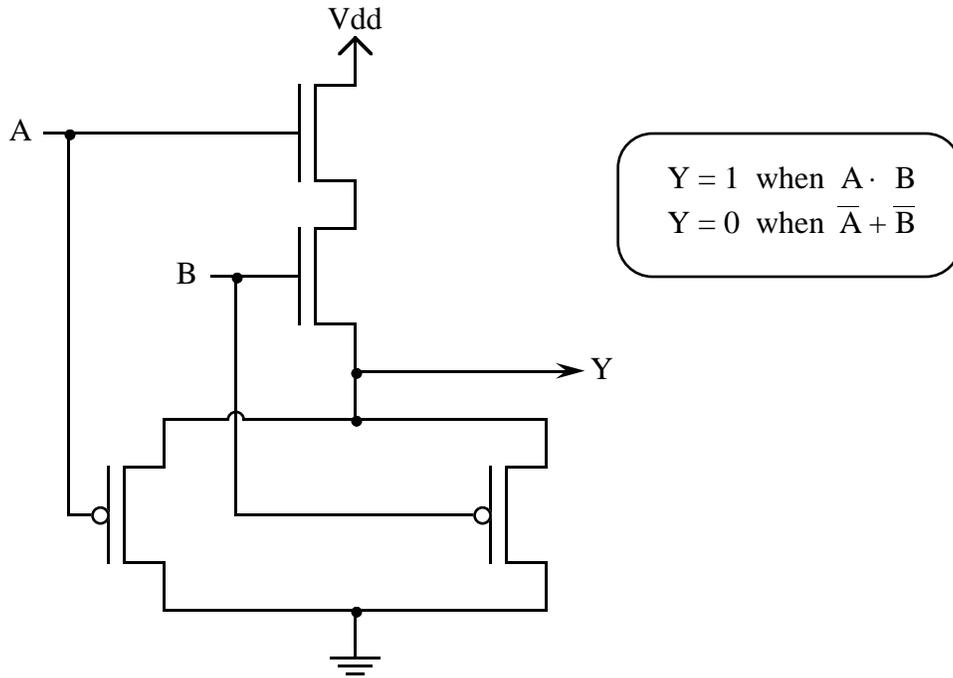


$$P_{tree} = \bar{A} \cdot \bar{B}$$

$$N_{tree} = A + B$$

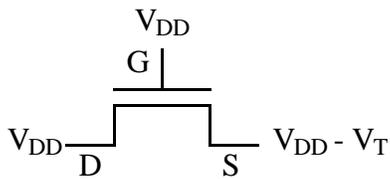


What logic gate is this?



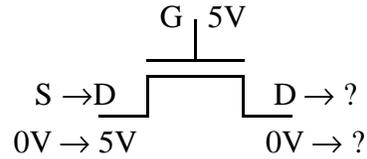
Answer: AND function, but poor design!

Why? *n*MOS switches cannot pass a logic "1" without a threshold voltage ( $V_T$ ) drop.



where  $V_T = 0.7V$  to  $1.0V$  (i.e.,  
 threshold voltage will vary)  
 output voltage =  $4.3V$  to  $4.0V$ ,  
 a *weak* "1"

The  $n$ MOS transistor will stop conducting if  $V_{GS} < V_T$ . Let  $V_T = 0.7V$ ,

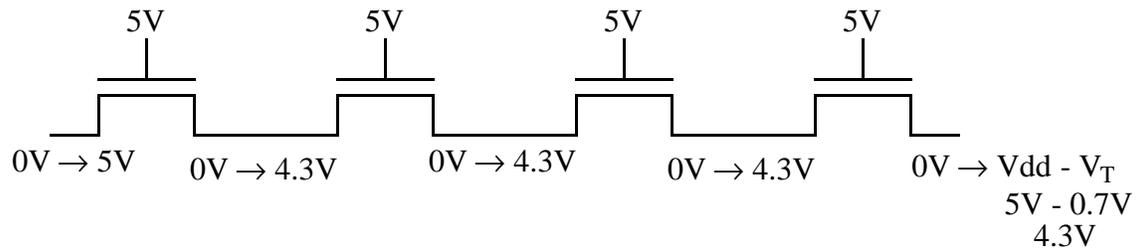


As source goes from  $0V \rightarrow 5V$ ,  $V_{GS}$  goes from  $5V \rightarrow 0V$ .

When  $V_S > 4.3V$ , then  $V_{GS} < V_T$ , so switch stops conducting.

$V_D$  left at  $5V - V_T = 5V - 0.7V = 4.3V$  or  $V_{dd} - V_T$ .

What about  $n$ MOS in series?

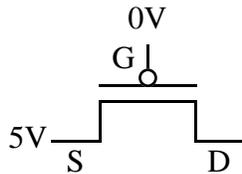


Only one threshold voltage drop across series of  $n$ MOS transistors

For *p*MOS transistor,  $V_T$  is negative.

*p*MOS transistor will conduct if  $|V_{GS}| > |V_{Tp}|$  ( $V_{SG} > |V_{Tp}|$ ),

or  $V_{GS} < V_{Tp}$



$$V_{Tp} = -0.7V$$

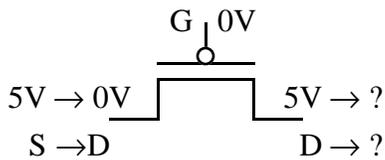
$$V_{GS} = 0V - 5V = -5V$$

conducting

$$V_{GS} < V_{Tp} \text{ or } |V_{GS}| > |V_{Tp}|$$

$$-5V < -0.7V \quad 5V > 0.7V$$

How will *p*MOS pass a "0"?



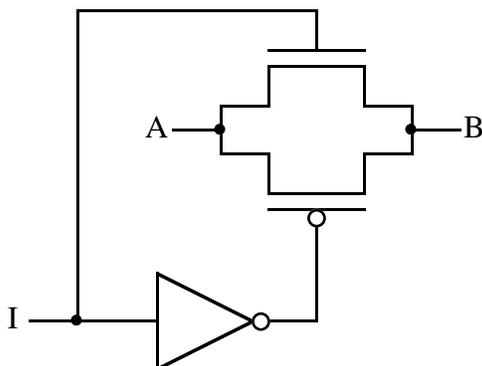
When  $|V_{GS}| < |V_{Tp}|$ , stop conducting

So when  $|V_{GS}| < |-0.7V|$ ,  $V_D$  will go from  $5V \rightarrow 0.7V$ ,

a weak "0"

How are both a strong "1" and a strong "0" passed?

Transmission gate pass transistor configuration



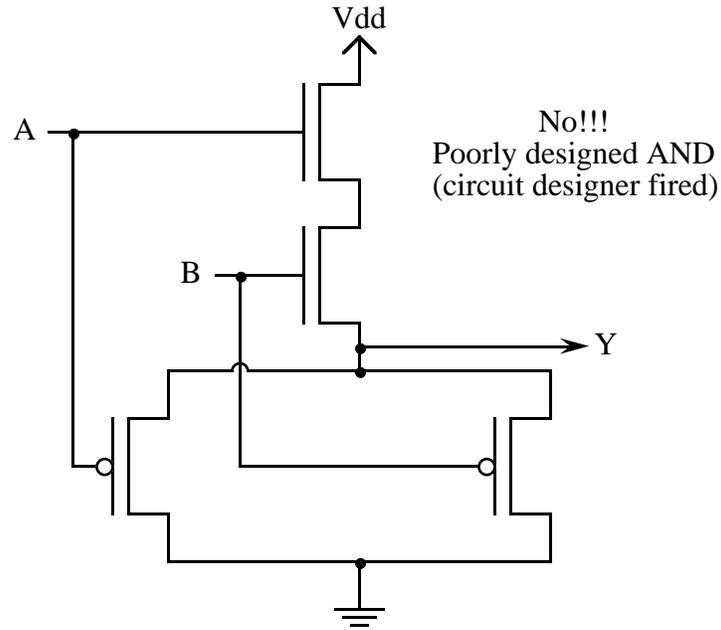
When  $I = 1$ ,

$B = \text{strong } 1, \text{ if } A = 1;$

$B = \text{strong } 0, \text{ if } A = 0$

When  $I = 0$ , non-conducting

# About that AND Gate...



Instead use this,

