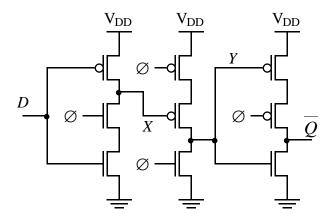
Back to TSPC D Flip-Flops: Falling Edge-Triggered Observations

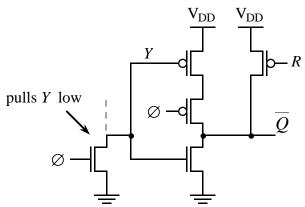


When clock = 0, Y node controls \overline{Q} , but X_{old} value controls \underline{Y} !

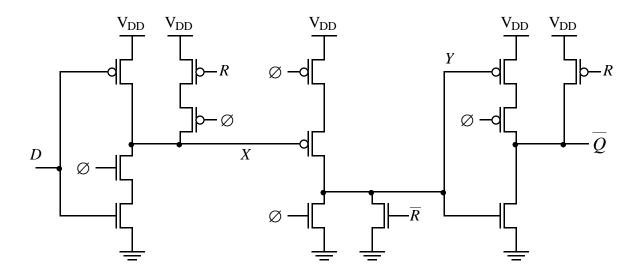
clock	D	X	Y	$\overline{\mathcal{Q}}$
0	1	$X_{\text{old}} = 0$	1	0
		= 1	$Y_{\text{old}} = 0$	1
			= 1	0

When clock = 0, reset will have to affect both X, Y nodes!!!

When clock = 1, only internal node which can affect \overline{Q} is Y and this is pulled <u>low</u>. This means we will <u>have to put a pullup directly on \overline{Q} (at least), also must set Y = 0.</u>



Falling Edge Triggered TSPC D-Flip Flop with Asynchronous Low-True Reset



$$R = 1 \qquad X = 1 \text{ or } X_{\text{old}} = 1$$

$$Y = 0 \qquad Y = Y_{\text{old}} = 0$$

$$\overline{Q} = 1$$

$$CLK = \emptyset$$

$$R$$

$$Y = 0$$

$$\overline{Q} = Q_{\text{old}} = 1$$

$$\overline{Q} = 1$$

$$X = \text{don't care}$$