# A MICROCONTROLLER WITH BUILT-IN SUPPORT FOR CCSDS TELECOMMAND AND TELEMETRY

Marc POLLINA[1] , Peter SINANDER[2], Sandi HABINC[2]

*[1]ADV Engineering, Parc Technologique du Canal, 15 Avenue de l'Europe,*
*F-31520 Ramonville Saint-Agne, France*
*Tel. +33 5 62 19 04 44, Fax. +33 5 62 19 03 54, pollina@dial.oleane.com*

*[2]European Space Agency, Electrical Engineering Department, Microelectronics Section*
*Postbus 299, NL-2200 AG Noordwijk, The Netherlands*
*Tel. +31 71 565 6565, Fax. + 31 71 565 4295, sandi@ws.estec.esa.nl, psi@ws.estec.esa.nl*

## Background

In the frame of an ESA activity, ADV Engineering is developing a microcontroller based on the well-known Intel 8052 device. The objective is to develop a microcontroller for applications with moderate processing requirements but needing high safety and easy accommodation of equipment interfaces.
This component is therefore a good candidate for embedding in a large variety of platform and payloads. It offers the possibility to distribute the intelligence into the equipments which is of particular interest for future telecommunication applications.

The full paper shall present the target applications and their requirements, the microcontroller features, its architecture and the development status.

## Main characteristics

The goal of the microcontroller is to allow low non-recurring and recurring costs for equipment and sub-systems, as well as ensuring low power consumption and mass. This is achieved by integrating specific CCSDS and spacecraft functions and interfaces on-chip, by optimising the memory interface, and by addressing software development aspects. Consequently the microcontroller core is fully compliant with the 8052 instruction set and can be programmed in C or assembler using standard commercial tools. Furthermore, the core is three times faster than a standard 8052, providing adequate computing performance for many applications.

Important memory interface features include:

- 512 bytes on-chip memory;
- full 64 kbytes addressing range for program and data, expansion up to 128 kbytes for data;
- memory protection and error correction;
- Direct Memory Access to the on-chip memory through a separate port.

## CCSDS support

The microcontroller includes a CCSDS Compatible Cyclic Redundancy Code (CRC) calculator to accelerate checking and generation of Telecommand and Telemetry packets. This, together with the built-in TTC-B-01 and MAP serial interfaces, allows the microcontroller to directly interface a Packet Telecommand Decoder and a Telemetry Encoder. The interfaces are fully compatible with the PTCD and the VCA/VCM devices from MITEL Semiconductor.

The CCSDS support will be further strengthened by the development of drivers allowing booting and software up loading through the telecommand link.

## Architecture

The full design is technology independent since it is VHDL based, including the microcontroller core which has been procured from an intellectual property provider. The long-term availability of the product is therefore independent of foundry processes evolution and it can be implemented in any technology.
The architecture of the microcontroller is modular with main functions broken down into specific VHDL blocks. This modularity both facilitates the current development as well as allows future evolution of the microcontroller without modifying the 8052 core. It is expected that the basic building blocks will be re-used when developing Application Specific Standard Products (ASSPs) for space applications. This approach is in line with the evolution towards "system-on-a-chip" where focus is placed on architecture optimisation and testability.

## Development status

The objective of the current activity is to demonstrate the microcontroller functionality by implementing it in a Field Programmable Gate Array (FPGA) from ACTEL. A breadboard is expected in Q3 1998 to be used in potential follow-on activities for validation of both the microcontroller concept and this particular implementation. It is anticipated that the microcontroller will be industrialised and provided to users as an ASSP manufactured in a radiation tolerant process by the end of 1999.

**Background**

The evolution of micro-electronics is driven towards « system-on-a-chip » approaches in which both hardware and software functions are being integrated in single chip devices. One of the key elements to succeed in this challenge is to use already qualified VHDL building blocks so that development time and cost are compatible with economical constraints.

In practice this means that « virtual components » are appearing in the market and it is in this context that ESA has initiated an action on microcontroller cores.

The choice of the 8052 core for developing a micro-controller dedicated to space applications has been motivated by two major reasons : the fact that the 8052 has become an industry standard in embedded applications and the availability of several processor cores in the form of VHDL macro-cells.

With shipments of over 100 millions units a year, representing close to 30 % of the 8 bit micro-controller market, the 8052/8051 family continues to grow at an outstanding rate into variety of applications. This predominant position ensures the availability of low-cost development environments, wide knowledge by software developers and long term support to the products.

In addition to this, the availability of the design in the form of a VHDL core ensures the capability to develop a product independently from the manufacturing technology. This is essential and solves the critical issues related to technology evolutions and obsolescence of products.

**Main characteristics**

The ADV 80S52 micro-controller has been designed to facilitate as much as possible the development of applications. This is achieved by its compatibility with commercial development environments and by specific architectural features related to memory management and interfacing versatility.

*Development environment*

The micro-controller ADV 80S52 is fully compliant with the 8052 instruction set. This compliance allows the application developers to use off-the shelf products and to fully benefit from low cost development environments. The current market offer for the 8051/8052 consists in a wide range of products supporting both hardware and software development (In-circuit emulators, C compilers, Simulators & debuggers,...).

In addition, the know-how on these environments is widely available which contributes significantly to costs reductions.

*Performances*

The real time performances of the processor have been improved with respect to the initial 8051.This has been achieved by using a processor core which requires less clock cycles to execute the instructions. In average, the performances have been increased by a factor of 3 which means a processing power of about 2.3 MIPS at 15 Mhz.

This increased capability is of particular interest for TM/TC applications which require reasonable real-time performances for I/O management.

*Memory features*

Specific features have been added to the basic 8051/8052 architecture, in particular with respect to internal and external memory management.

These features are summarised here below :

- 512 bytes of internal memory, of which 256 bytes are shared with external unit or used as a 32x32 bit event counter
- Full 64 K addressing range for program and data memory
- De-multiplexed Address/Data bus,
- Memory protection for both internal and external memory
- Memory access expansion up to 128 K on the data memory
- Program down loading capability and program execution from RAM
- DMA access by an external device without slowing down the performances.

Among the above features, the memory protection & correction capability is of particular interest since it provides a major improvement for space applications.

The implemented mechanism allows to detect and correct in real time the RAM bit errors without imposing delays to the processors. This detection/correction mechanism is totally transparent from user point of view.

The price to pay for this feature is an increased memory size but it allows to use non radiation hard memories which are less expensive.

An other important feature concerning the memory management is related to the internal memory XRAM 256 bytes (see fig 1).

This XRAM memory can be accessed via DMA by an external user (dedicated electronics or signal processor) and it can be used for two possible functions :

- either as a communication buffer to perform command & control exchanges between the micro-controller software and the external application
- or as a set of events counters (32x32 bits) which may be useful for certain applications.

**CCSDS support**

The support to CCSDS applications has been defined mainly through packet processing interfacing with TM/TC devices.

Concerning the packet processing, the microcontroller includes a CCSDS Compatible Cyclic Redundancy Code (CRC) calculator to accelerate checking and generation of Telecommand and Telemetry packets. The calculation is performed on 8 bit slices and the 16 bit result is provided in two registers. The processing of an 8 bits slice is performed in two clock cycles which represent a significant increase of performances and a release of the processing demand on the CPU core.

With respect to interfaces accommodation, a built-in TTC-B-01 and MAP serial interfaces, allows the microcontroller to directly interface a Packet Telecommand Decoder and a Telemetry Encoder. The interfaces are fully compatible with the PTCD and the VCA/VCM devices from MITEL Semiconductor.

In summary the interface features are the following :

- Four serial interfaces : one RS232 UART and three extra UART configurable (RS-232, MAP and TTC-B-01)
- Three 16-bit counter/timers with extended time count capabilities with respect to the original 8051
- 32 Event counters 32 bits each
- Four external interrupts with two-priority levels
- power down mode

The CCSDS support will be further strengthened by the development of drivers allowing booting and software up loading through the telecommand link.

**Architecture**

The microcontroller architecture is fully based on VHDL modules and is broken down into 3 major building blocks :

- the 8052 core including memory management and memory extensions
- the support modules (CRC, timers, IT controler) and the I/O peripherals (4 serial interfaces) connected on the internal command&control bus the « SFR bus ».
- the user interface which is the exchange area between the microcontroller and an external application.

The overall architecture is illustrated in figure 2 in which the SFR bus is shown as the internal command & control bus of the microcontroller.

The 8052 core is built around a VHDL macrocell (whose complexity is about 10 000 gates) which has been procured from an intellectual property provider. The macrocell design has been validated against the 8052 instruction set. Two major validations have been conducted to ensure the full compliance :

- instruction tests : each instruction has been tested individually with different sets of parameters,
- random routines tests : random sequences of instructions have been generated and their execution result is compared with the emulator execution.

Concerning random testing this technique has demonstrated its efficiency and it has allowed to execute over 1 million instructions.

The support modules have been developed specifically for the ADV 80S52 microcontroller and they are all commanded & controlled via the internal SFR bus which allows fast access via the processor core.

By means of SFR bus interfacing, the architecture of the microcontroller is modular since main support functions are corresponding to specific VHDL blocks.

This modularity both facilitates the current development as well as allows future evolution of the microcontroller without modifying the 8052 core. It is expected that the basic building blocks will be re-used when developing Application Specific Standard Products (ASSPs) for space applications.

For instance, most of the microcontroller design is used in the development of a 1553 smart coupler under CNES contract.

**Development status**

The on-going ESA contract is dedicated to the validation and demonstration of the micro-controller functionnalities.

The procured core has been submitted to complementary validations to reach an adequate level of confidence in the 8052 compliance.

The VHDL development of modules necessary to complement the core is being finalised and an FPGA demonstrator (based on ACTEL 3200 DX devices) will be available by September 98.

After this bread-boarding phase it is expected to implement the obtained micro-controller both in the form of an ASSP (ADV 80S52) and in the form of VHDL core for ASIC designs.

The industrialisation of the ADV 80S52 micro-controller is expected to occur early 99, the target being to propose a radiation hard product (MITEL SOS5) which should be available by end of 99.

It is expected to have a wide interest in this product since it satisfies the needs of small applications which are often encountered in payloads.

**Conclusions**

The activity on the 8052 microcontroller has allowed to define an architecture optimised for a wide variety of space applications demanding low porocessing power but high versatility in interfaces accomodation.

The expected outputs are in terms of products both in the form of ASSP devices such as the ADV80S52 microcontroller and in the form of re-usable VHDL macrocells.

The proposed approach offers the possibility to develop low cost on-board applications and to ensure long term availability of the design because of the technology independance provided by VHDL.

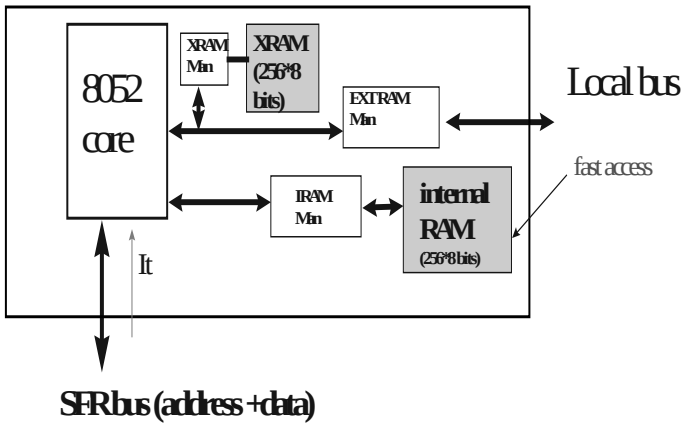


**Fig 1 : Internal RAM & memory protection**

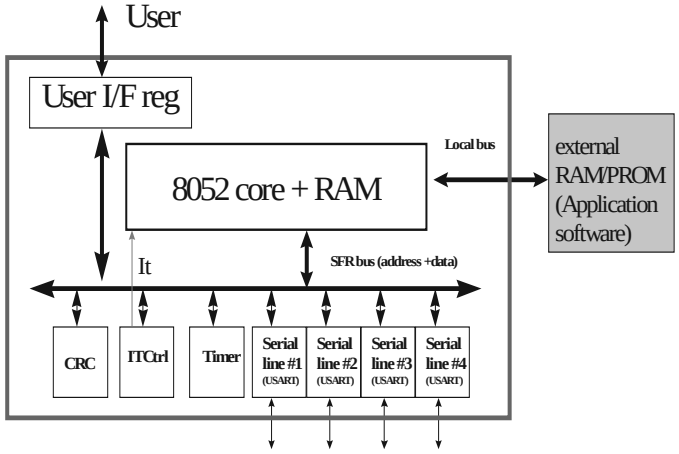


**Fig 2 : Overall architecture**

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