PETRA SSL40S100

Packetised Essential Telemetry Retrieval ASIC

Silicon Systems Limited

OVERVIEW

The Packetised Essential Telemetry Retrieval ASIC (PETRA) is a single chip, low power device for automatically retrieving spacecraft status and sensor data in analog or digital form. This device can be integrated to a spacecraft's Data Handling System (DHS) to provide Emergency Telemetry service or to function as a Packet Terminal. The PETRA presents its output as an ESA/CCSDS telemetry packet which can be communicated directly to a Telemetry (TM) Encoder or to another PETRA on its Virtual Channel Assembler (VCA) compatible serial interface, as well as to the on-board data handling bus via an RS232 serial output port. The PETRA can accept data from another PETRA or VCA compatible device on its cascade port.

By integrating the PETRA into the DHS, it is possible to allow essential telemetry data to be gathered independently of any failures which may occur in a complex centralised system. The PETRA solution results in a faster recovery time in the event of a power outage as only the TM Encoder and transmitter must be operational to function. The PETRA data is, however, not exclusive to emergency situations. It could be treated as an intelligent user and interrogated via the spacecraft data bus.

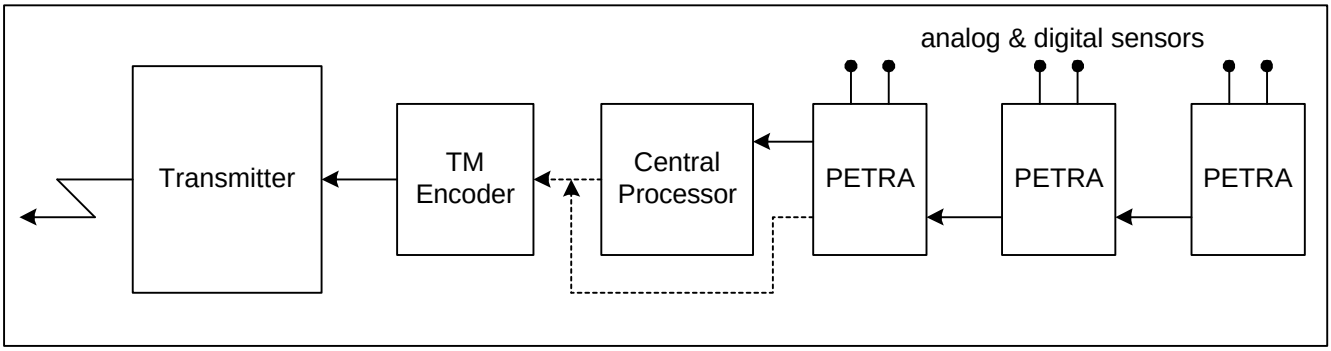
Digital and/or analog data can be scanned in a fixed sequence over 12 different scan periods. Multiple PETRAs can be cascaded to produce either a stream of separate telemetry packets (cascade mode) or a large composite telemetry packet with one header (merge mode). The PETRA can provide its own "time of origin stamp" to allow the exact sampling time of a discrete input to be determined. The PETRA also supports the optional insertion of a CCSDS compatible 16-bit CRC packet error control field. An event driven mode allows high time resolution combined with low packet generation for providing status information at regular intervals.

KEY FEATURES

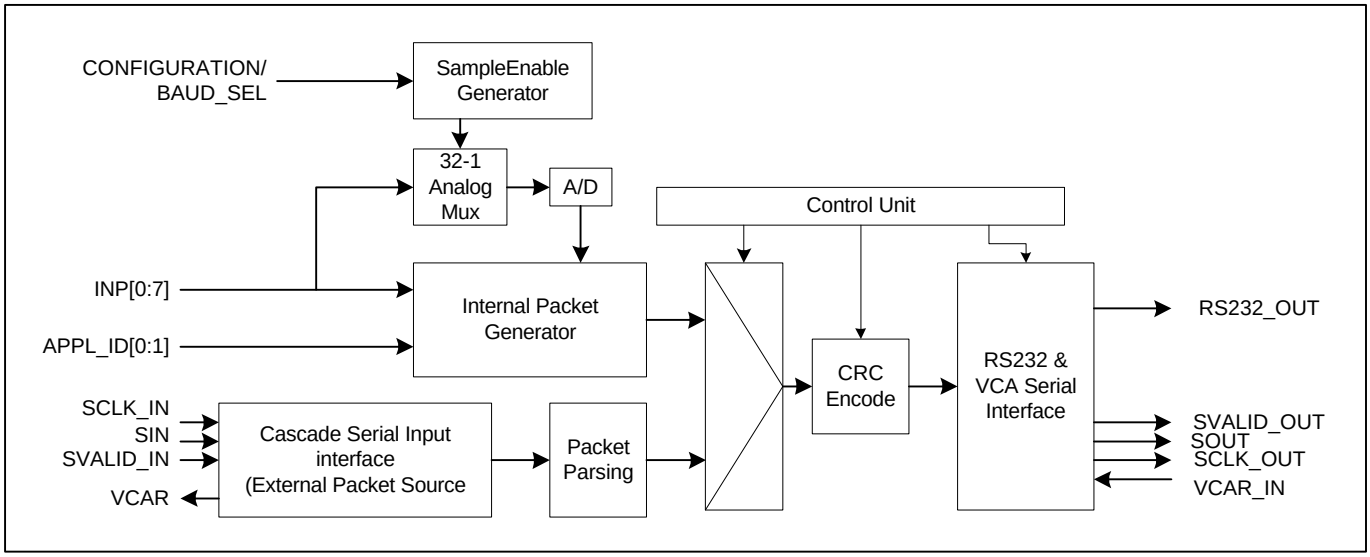
- Fully compliant with CCSDS/ESA Packet Telemetry Standard
- Synchronous VSA compliant serial interface
- RS232 interface with selectable 9600bps or 115200bps Baud Rate
- 40 discrete inputs, 32 can be configured to handle analog inputs
- 8-bit ADC resolution on selectable analog input ranges of 0-1V or 0-4V
- Optional CRC generation
- Optional CCSDS/ESA compatible Time reference field in the packet
- Selectable input Scan Period of 10ms, 20ms, 50ms, 100ms, 500ms, 1s, 2s, 5s, 10s, 50s
- 80mW power consumption at 4MHz

SYSTEM CONFIGURATION

PETRA communicating with the Central Processor or alternatively directly with the TM encoder.



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Non-operating)

Parameter	Max. Rating
Operating Temperature	-55 C to +125 C
Storage Temperature	-55 C to +150 C
Supply Voltage	-0.3V to +7.0V
Input Pin Voltage	-0.3V to (VDD + 0.3V)
Input Current on any pin	-/+ 50mA
Humidity Noncondensing	5% to 85%
Electrostatic Discharge	1000V

TECHNOLOGY

- 5V power supply (typical)
- Implemented in a 0.8um double metal, double poly CMOS process
- Digital Logic:synthesised onto a standard cell library
- Digital gate count:22k
- 10-bit full custom successive approximation charge redistribution ADC
- Die Area: 26mm2
- Packaged: 84 pin gull-winged hermetically sealed Quad Cerpac Kyocera QC-084405-WZ

DC PARAMETERS

TTL Input	Min.	Max.
Input low voltage		0.8V
Input high voltage	2.0V	
Input capacitance		0.2pF
Input impedance		10Mohms

CMOS Output	Min.	Max.
Output low voltage		0.4V
Output high voltage	4.0V	
Output static current	8.0mA	-8.0mA
Capacitance		0.45pF

Power Dissipation	Min.	Max.
Static Dissipation		30mW
Dynamic Dissipation		12.5mW/Mhz

AC PARAMETERS

Frequency	Min.	Max.
Crystal (system clock) frequency	0MHz	8MHz
Nominal crystal frequency	3.96MHz	4.04MHz

Reset	Min.	Max.
Reset assertion time	1us	

ADC	Min.	Max.
ADC resolution (volts/LSB)	3.9mV	
ADC frequency range	2kHz	350kHz
ADC voltage range (10 bits)	0V	4V

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