Development Plan for Turbo Encoder Core and Devices Implementing the Updated CCSDS Telemetry Channel Coding Standard

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Abstract

With requirements on increasing data rates for deep space missions, the commonly used standard concatenated Reed-Solomon and Convolutional coding is not always adequately meeting the available link budget. A new coding scheme known as Turbo Coding is therefore being introduced in the telemetry channel coding recommendations from the Consultative Committee for Space Data Systems (CCSDS). As turbo coding is being considered for several European scientific spacecraft (e.g. Smart-1, Rosetta and Mercury), the development of a turbo encoder core and devices, with the associated ground system, has been undertaken by the European Space Agency (ESA).

1 INTRODUCTION

Rosetta is the first of a series of ESA deep space missions to be launched in the next century. The nominal return link margins of Rosetta at the comet encounter are 1.5 dB below the requirement. It is therefore necessary to halve the return symbol rate from the scientists' preferred rate. Moreover, the link margins are also not met during other mission phases and in certain emergency conditions. Similar conditions are expected for Mars Express which is designed in strict commonality to Rosetta. Therefore, together with the National Aeronautics and Space Administration (NASA), ESA has investigated whether *Turbo Codes* (Ref. 1), (Ref. 2), (Ref. 3), (Ref. 4) could outperform the standard concatenated code by at least 1.5 dB on frame error rate. The results of the first study by Politecnico di Torino on this topic were encouraging (Ref. 5), for moderate complexity codes improvement as high as 2.7 dB were found.

In agreement with NASA and other national space agencies it was decided to include a set of turbo codes in a new issue of the CCSDS telemetry channel coding recommendation (Ref. 6). Turbo coding will be an add-on option to the recommendations without modifying the existing coding schemes and will retain compatibility with the CCSDS Packet Telemetry recommendation. *Pink sheets* updating the recommendation are currently being reviewed to formally establish turbo coding as an alternative to both Reed-Solomon and Convolutional coding for deep space and near-Earth missions (Ref. 7).

In this paper we present the turbo codes that are being proposed for the recommendation, followed by the expected coding gain with respect to the present encoding scheme. This is followed by an outline of the planned turbo encoder development related to the space segment, providing a specification of a turbo encoder core suitable for further implementations. The instantiation of this core will be discussed, covering both the implementation as a Field Programmable Gate Array (FPGA) for the Smart-1 mission, as well as a single chip encoder Application Specific Integrated Circuit (ASIC) for future missions. This is followed by a presentation of ongoing developments on the ground segment.

2 CCSDS TURBO CODE SPECIFICATION

Turbo codes can be seen as parallel concatenation of multiple simple component-encoders. In the case of the CCSDS recommendation, the component-encoders are two identical recursive convolutional encoders, each with only 16 states as opposed to the 64 states of the concatenated encoder. The input to the turbo encoder is a telemetry frame of a predefined number of information bits. The first component-encoder operates on the information bit sequence directly, whereas the second component-encoder receives the information sequence in a reordered manner via a permuter (or interleaver) which is basically a pseudo-random scrambling device. A complete frame is read bit-by-bit into the permuter and read out in the specified pseudo-random order. The output from the two component-encoders are periodically mixed with the uncoded information bits to form the resulting turbo encoded output.

The turbo code specification proposed for the CCSDS recommendations is summarised hereafter and is depicted in figure 1. Note that we do not claim that this is the scheme that will finally be approved by CCSDS. The reader is advised to contact CCSDS for the latest available version of the telemetry channel coding recommendation.

2.1 Code type and rate

The code type is a systematic parallel concatenated turbo code with two component codes (plus an uncoded component to make the code systematic). The nominal code rate is selectable with r = 1/2, 1/3, 1/4 or 1/6 bit per symbol.

2.2 Component codes

The component codes are recursive convolutional codes with 16 states each. They are implemented with backward and forward connection vectors. The backward vector for both component codes and all code rates is G0 = 10011.

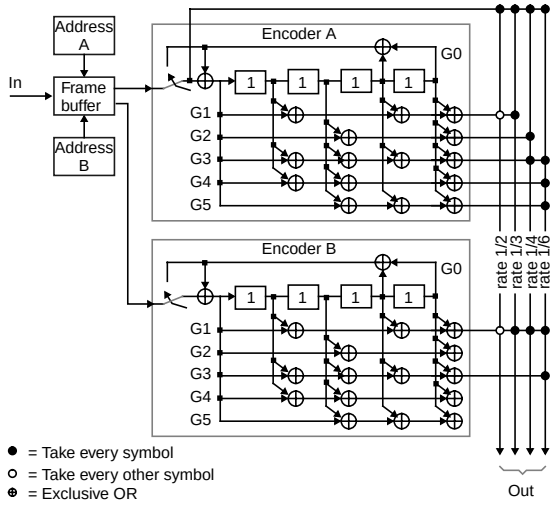

Figure 1: *Turbo encoder functional diagram*

The forward vector for both component codes and rates 1/2 and 1/3 is G1 = 11011. Puncturing on every other symbol from each component code is necessary for rate 1/2. No puncturing is done for rate 1/3.

The forward vectors for rate 1/4 is G2 = 10101, G3 = 11111 (1^{st} component code); G1 = 11011 (2^{nd} component code). No puncturing is done for rate 1/4.

The forward vectors for rate 1/6 is G3 = 11111, G4 = 11101, G5 = 10111 (1^{st} component code); G1 = 11011, G3 = 11111 (2^{nd} component code). No puncturing is done for rate 1/6.

2.3 Information block lengths

The information block lengths are given in table 1 and table 2. To be compatible with the existing frame lengths allowed by the current recommended concatenated coding scheme, the values allowed for the permuter length k have been chosen corresponding to those allowed when using Reed-Solomon encoding (on non-shortened codeblocks) with interleaving depths 1, 2, 4, and 5. A value of 16384 bits for highest coding gain is also allowed. Since the values for frame length proposed for the turbo code option in the CCSDS channel coding recommendation correspond to those allowed for Reed-Solomon encoding, it will be possible to keep unaltered the upper layers implementations of the telemetry encoder.

Information block length k, bits	Corresponding Reed-Solomon interleaving depth I	Notes
1784 (= 223 x 1 octets)	1	For very low data rates or low latency
3568 (= 223 x 2 octets)	2	
7136 (= 223 x 4 octets)	4	
8920 (= 223 x 5 octets)	5	
16384		For highest coding gain

Table 1: *Standard information block lengths*

Information block length k, bits	Codeblock length n, bits			
	rate 1/2	rate 1/3	rate 1/4	rate 1/6
1784	3576	5352	7152	10704
3568	7144	10704	14288	21408
7136	14280	21420	28560	42840
8920	17848	26772	35696	53544
16384	32776	49164	65552	98328

Table 2: *Standard codeblock lengths*

2.4 Permuter

The permuter (or interleaver) is a fixed bit-by-bit permutation of the entire input frame of data. Unlike the symbol-by-symbol rectangular interleaver used with Reed-Solomon codes, the turbo code permutation scrambles individual bits and resembles a randomly selected permutation in its lack of apparent orderliness. The recommended permutation for each specified block length k is given by a particular reordering of the integers 1, 2,..., k as generated by the following algorithm (see figure 2).

First express k as $k = k_1 k_2$. The parameters k_1 and k_2 for the specified block sizes are given in table 3. Next, the following operations for $s = 1$ to $s = k$ should be performed to obtain the permutation numbers $\pi(s)$. Note that p_q denotes one of the eight prime integers given in table 4.

$$m = (s-1) \bmod 2$$

$$i = \left\lfloor \frac{s-1}{2 \cdot k_2} \right\rfloor$$

$$j = \left\lfloor \frac{s-1}{2} \right\rfloor - ik_2$$

$$t = (19i + 1) \bmod \frac{k_1}{2}$$

$$q = t \bmod 8 + 1$$

$$c = (p_q j + 21m) \bmod k_2$$

$$\pi(s) = 2\left(t + c\frac{k_1}{2} + 1\right) - m$$

Figure 2: *Permuter algorithm*

Information block length k, bits	k_1	k_2
1784	8	223 x 1
3568	8	223 x 2
7136	8	223 x 4
8920	8	223 x 5
16384	128	128

Table 3: *Standard k_1 and k_2 parameters*

$p_1 = 31$	$p_2 = 37$	$p_3 = 43$	$p_4 = 47$
$p_5 = 53$	$p_6 = 59$	$p_7 = 61$	$p_8 = 67$

Table 4: *Prime integers*

2.5 Codeblock specification

The resulting codeblock contains $(k + 4)/r$ encoded symbols, where r is the nominal code rate as presented previously. The additional 4 input bits (producing 4/r encoded symbols) are required for terminating the Trellis and actually implementing a block code. A codeblock is consequently independent of any previous codeblock, as opposed to existing Convolutional code.

2.6 Attached synchronisation marker

The Attached Synchronisation Marker (ASM) differs for the four code rates. The number of bits are proportional to the code rate, with the marker length being $32/r$-bit for r = 1/2, 1/3, 1/4 and 1/6, e.g. r = 1/6 gives a sequence of 192 bits. As for Reed-Solomon coding, the ASM is used for frame synchronisation.

2.7 Pseudo-randomiser

The same pseudo-randomiser as for Reed-Solomon coding can be used with the turbo codes:

$$h(x) = x^8 + x^7 + x^5 + x^3 + 1$$

The sequence generator should be initialised to the all-one state at the start of each codeblock. The bit sequence is exclusive-OR-ed with the codeblock.

3 CODING GAIN

The coding scheme currently recommended by CCSDS is the concatenated Reed-Solomon (255, 223) and Convolutional (rate 1/2, 64 states) code for which both ESA and NASA have encoders and decoders available off-the-shelf, e.g. the RESCUE device (Ref. 11). For deep space missions like Rosetta and Mars Express or non deep space missions with moderate telemetry data rates, the required Frame Error Rate (FER) typically is less than 10^{-4} which corresponds to a Bit Error Rate (BER) of less than 10^{-7}. With an interleaving depth of 5 for the Reed-Solomon code, the FER of less than 10^{-4} is met when the bit signal to noise ratio is greater than 2.6 dB. Such code has a gain of about 9.5 dB with respect to the uncoded case but is still about 3.5 dB off the Shannon limit, therefore showing potential room for improvements in the coding area.

For the turbo code, several rates are selectable by the users. The lower the rate, the better the coding gain and therefore the lower the bit energy over noise density for the same FER. It can be seen from table 5, that the gain over the standard concatenated encoding (I = 5) at FER = 10^{-4} ranges from 1.7 dB with the turbo rate 1/2 code to 2.7 dB for the turbo rate 1/6 code. Computing the gain for FER = 10^{-6} with the simulation techniques used for FER = 10^{-4} requires years of processor time on the most powerful workstations. To date, therefore, it has only been possible to estimate with a conservative semi-analytical technique that gains ranging from 1.2 dB (rate 1/2) to 2.0 dB (rate 1/6) should be obtained with the proposed codes. Therefore, even high rate near-Earth missions with FER requirements of 10^{-6} or better can take advantage of the turbo codes proposed for deep space missions and operate closer to the Shannon limit than with the standard concatenated encoding. Description of the detailed analysis and simulation work performed along with the proposed codes can be found in a companion article (Ref. 8), addressing practical issues of quantisation, effect of phase noise on the carrier, etc.

Rate	Improvement [dB] @ FER = 10^{-4}
1/2	1.7
1/3	2.3
1/4	2.5
1/6	2.7

Table 5: *Estimated improvement against the concatenated coding scheme (Reed-Solomon and Convolutional code, interleave depth 5)*

4 THE SPACE SEGMENT

For the space segment, the development of the turbo encoder will follow the same approach that was taken by the Agency for the development of the radiation hard RESCUE device. The RESCUE design was based on Reed-Solomon and Convolutional encoder cores initially developed at the European Space Research and Technology Centre (ESTEC). By having in-house developed encoder cores that are technology independent, the Agency can act as a virtual second source to a foundry manufacturing a device incorporating them. Should it be required, the encoder cores can be rapidly targeted to another foundry, or be easily integrated in a system-on-a-chip.

To ensure that the planned turbo encoder core meets all user requirements, a baseline specification is presented in the next section. It covers areas such as transfer rates and interfaces.

The baseline is to implement the turbo encoder core in an FPGA for the Smart-1 mission. Due to the low complexity of the FPGA, an external memory will be required to hold the incoming frame during encoding. This first step in the overall development will allow early validation of the encoder core and provide an intermediate solution to spacecraft with schedules incompatible with an ASIC development.

The next step would be to integrate the encoder core together with the required memory in an ASIC. This will increase overall reliability and reduce power consumption and required board area. An ASIC development could be initiated provided there is sufficient interest from industry and projects.

A different approach has to be taken for the Rosetta mission as the procurement of onboard subsystems is already started. Since the data rates are low, the turbo encoding could be implemented in software and used when required achieving the necessary link margins. The uncoded frames would always be generated by the Virtual Channel Multiplexer (VCM) (Ref. 9) and the Virtual Channel Assembler (VCA) (Ref. 10), be encoded by software routines, augmented by the addition of the required synchronisation markers, and then sent to the transmitter. The only foreseen impact of turbo codes onto the Rosetta onboard

telecommunications system is that a different symbol rate would have to be accommodated by the modulator.

5 TURBO ENCODER CORE

The turbo encoder core should support the full CCSDS recommendation, including all frame lengths and code rates. All synchronisation markers should be implemented. It should implement pseudo-randomising and allow bypassing of the encoder. It should be compatible with existing telemetry encoders. The turbo encoder should be interchangeable with the RESCUE device to allow potential swaps late in the telemetry subsystem development. The data rates will depend on the technology used for implementing the encoder. However, the core will be targeted towards input data rates beyond 1 MHz when implemented in an FPGA with an external frame memory.

5.1 Interfaces

The input interfaces of the turbo encoder for present telemetry encoders could in a first stage be limited to only one interfacing component. The VCM is used on several commercial and scientific satellites and is an integral part of the modern packet telemetry encoder. The interface is simple; one bit clock, one data line and one line indicating when a frame is being sent. Although a simple interface, the communication protocol causes some problems. The VCM is designed to provide continuous and contiguous telemetry frames, only interrupted by the ASM or the optional Reed-Solomon check symbols. The turbo coding scheme requires however that four additional bits are inserted between the telemetry frame and the ASM. If the termination bits are not inserted, there is a loss of 0.1 to 0.2 dB only for an FER of 10^{-4}. This requires that the bit clock on the VCM is stopped for four clock periods while the tail bit are transmitted by the encoder. This constraint leads to one solution; to include the clock divider in the encoder itself.

5.2 Clock divider

The clock divider should as a baseline allow three implementation options; simple division with matching system clock frequency and code rate, possibility for a base rate and the double code rate (e.g. 1/4 and 1/2), and the more complex solution of supporting all code rates from a single system clock frequency. It should provide an input bit clock equaling the input rate, and an output symbol clock equaling the output rate. It should also provide a clock for interfacing devices such as the VCM, requiring special treatment of the code tail sequence.

5.3 Technology

The core has to be technology independent to allow implementation in various technologies, commercial amongst others. The Very High Speed Integrated Circuit Hardware Description Language (VHDL) will be used. To reduce the susceptibility against heavy ion effects, redundancy and voting mechanisms should be included. It will be possible to easily exclude such logic, should a near immune process be targeted.

5.4 Verification and validation

The turbo encoder core development should be completed in October 1998, after which verification with respect to the decoders developed for European Space Operations Centre (ESOC) can take place. It is foreseen to verify the turbo encoder core by providing encoded frames to those working on turbo decoders. The verification is foreseen to be based on encoded transfer frames generated through simulation of VHDL models. Models for the VCM and VCA devices are available and are suitable for this kind of boardlevel simulation. The advantage of performing boardlevel simulations already when verifying the encoder core is that the transfer frames will be formatted according to ESA and CCSDS recommendations, enabling verification of the interface between the turbo decoder and the ground station equipment. The verification of the encoder core should be completed by the end of 1998.

It is also the intention to exchange coded frames with other CCSDS partners. Ultimately, a reference data base of correctly encoded frames, covering all frame lengths and code rates, should be established and be made available via the net. The purpose of the data base is to support companies developing encoders and decoders. Experience from the telecommand decoder specification and development phase has shown that a reference data base alleviates many ambiguities and possible misinterpretations.

5.5 Distribution scheme

With with only a few foundries manufacturing radiation hard or tolerant components in Europe, it is not the intention to provide a core to industry intending to duplicate an existing product targeted to the space segment. For this reason has the Reed-Solomon core not yet been distributed to anyone. The same approach will be taken for the turbo encoder core. To protect the market for an envisaged single chip turbo encoder that is either radiation hard or tolerant, the distribution of the core will be limited to developments that do not compete with said device. The baseline is therefore to provide the core only to companies developing specific systems/devices for which a radiation hard encoder is not suited. An example could be a scaled down single-chip telemetry encoder for a commercial satellite constellation where cost is the major requirement driver.

In the spirit of industrial co-founding, the core will not be given away free of charge if it cannot be shown that the product to be developed brings significant benefits to European space industry or the Agency. This should not be interpreted as a limitation, but rather as a challenging encouragement.

6 FPGA IMPLEMENTATION FOR SMART-1

Turbo encoding is being proposed as part of an experimental transponder onboard the Smart-1 satellite. With the baseline being Reed-Solomon encoding on Smart-1, it is required that the turbo encoder is either implemented in the experimental transponder itself, or in the telemetry encoder. Since the experimental transponder is also foreseen to be used as the

redundant transponder onboard, it has to be able to accept nominal mission data from the telemetry encoder.

The Smart-1 encoder is foreseen to be based on the VCA/VCM/ RESCUE chip set. As discussed previously, the VCM bit clock has to be controlled by the turbo encoder to insert space for the code tail sequence. This constraint rules out the possibility of placing the turbo encoder far away from the VCM. The Smart-1 telemetry encoder will therefore possibly have to comprise both a RESCUE chip and a turbo encoder.

The main complication lays in the design of the clock divider in the telemetry encoder. When the Reed-Solomon coding is cascaded with Convolutional coding, the output bit rate of the combined encoder is twice the input rate. The RESCUE chip includes both encoders and the associated clock divider. Since this also has to be the case for the turbo encoder to allow selectable code rates, the selection between the source for the VCM input bit clock needs to be performed carefully not to induce timing problems in either encoder configuration. The baseline will be not to support dynamic encoder changes and a reset of the telemetry will be required after each such change.

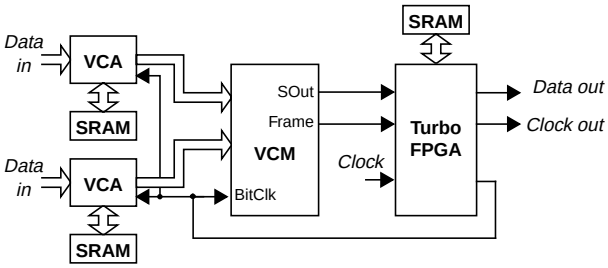

Figure 3: *Typical system using the turbo encoder FPGA*

As already mentioned, due to complexity reasons, the frame buffer memory cannot be implemented on the foreseen FPGA. It will instead by implemented with an external 4k-by-8 bit Static Random Access Memory (SRAM). The baseline will be to provide the encoder with a system clock with a frequency equaling the output data rate to minimise power consumption. This constraint requires that the read and write accesses to the external memory are tightly controlled. With an 8 bit wide memory interface, one write access is required per 8 input bits. The first component-encoder requires one read access per 8 bits, since all the bits can be used. For the second component-encoder, one read access is required for every input bit, since only one of eight bits is actually addressed. With a code rate of 1/2, there are only 16 clock periods available for the above accesses, and a properly performed write access requires at least three clock periods. This is however possible to implement when interfacing the VCM, since its interface complies to the strict data rate requirement.

A more flexible interface would require that the frame buffer can be randomly written to during the frame acquisition. Something that is easily accommodated in singe chip solution. The same approach could be taken when an off-chip memory is used. It comes however at a cost. To allow a write access to the frame memory that is not tightly synchronised with the read out accesses, the encoder needs to be operated at a higher clock frequency than what is required for the output data rate. The power consumption is likely to increase with a doubled system clock frequency compared to an implementation only interfacing the VCM. A trade off between power consumption and the need for a flexible interface is hence required.

The Smart-1 encoder will as a baseline be implemented in an Actel 14100 device, with flight parts procured in MIL-STD-883 quality level. Ongoing technology activities have shown that the selected device type has good radiation characteristics. Tests have shown it can sustain more than 50 krad total dose. It is however sensitive to Single Event Effects (SEU), which must be taken into account during the design. The frame buffer memory will be placed external to the FPGA and is planned to be implemented with an off-the-shelf radiation hard memory manufactured in Silicon On Insulator technology. The FPGA development should be finalised in June 1999 to meet the overall schedule of the transponder and the telemetry encoder.

For spacecraft with schedules not matching the development time required for implementing a turbo encoder in radiation hard ASIC technology, but, unlike Smart-1, have high requirements on radiation hardness, the design could be implemented in a radiation hard FPGA. The Actel RH1280 is similar to the 14100 device, but can withstand a total dose of at least 300 krad. The SEU sensitivity is however similar. The cost difference between the RH1280 and 14100 is in the order of one magnitude. The Smart-1 FPGA design will be compatible with the RH1280 in order to support demanding near-term missions.

An advantage of implementing the encoder in an FPGA is that it can be used in ground systems such as satellite simulators without incurring the high cost normally associated with parts provided by space foundries. The baseline is to provide any interested company with preprogrammed FPGAs. It will allow early use of the encoder, while protecting design information.

7 ASIC IMPLEMENTATION

For missions where power consumption and board area has to be minimised, and for missions with stringent radiation tolerance and reliability requirements, the next logical step is to develop a single chip turbo encoder in a radiation hard process with low SEU sensitivity. One possible candidate is the 1.25 µm SOS5 CMOS process from MITEL Semiconductor (S), which has also been used for the VCA/VCM/RESCUE chip set. Such a development could be initiated provided there is sufficient interest from industry and projects.

The main feature of a single chip encoder is the obvious inclusion of the frame buffer on-chip. The size of the buffer memory should be twice the largest frame size. A total of 32k bit memory is therefore required. The benefit of having the buffer on-chip is that the power consumption for the overall encoder can be reduced compared to a two chip alternative. Since the memory access can be made much faster on-chip, the duty cycle with respect to memory accesses can be reduced as well. The fast memory access also allows a relaxation of the input data requirements. The memory can therefore be used as a true buffer, allowing a varying input rate as long as the average

data rate equals the nominal rate. This enables the implementation of new type of interfaces.

Therefore, to further enhance the encoder versatility, some additional types of input and output interfaces could be envisaged. A parallel input interface supporting either an 8 or 16 bit data bus could allow a microprocessor to generate the telemetry frame. A 32 bit interface could also be considered, should an actual need arise. The nominal serial clock, data and frame input interface could be enhanced to support the traditional 16 bit memory load commands specified in the TTC-B-01 standard. A similar output interface could also be imagined. For test and evaluation purposes, the encoder could support bit serial asynchronous input and output interfaces being compatible with a Personal Computer (PC). This permits direct connection of the telemetry encoder to a ground station during development of the onboard data handling system etc. With the expanding use of commercial technologies, one can imagine that such an interface could actually be used in flight.

For future missions that will have even higher requirements on power and area consumption, the turbo encoder could be combined with the telemetry encoder and the telecommand decoder on a single chip. In such a device, one could imagine that the user would be free to select between turbo or Reed-Solomon encoding. The cores for developing this device will be ready by the end of this year, with the Reed-Solomon encoder core already finalised in 1997.

8 THE GROUND SEGMENT

Turbo encoding and decoding has been studied in several ESOC activities, with results confirming that the desired frame error rate can be obtained for deep space missions such as Rosetta. As the permuter size is normally large, maximum likelihood decoding is out of the question for complexity reasons. However, a suboptimal decoder implementing multiple iterations around a maximum a posteriori decoder is of the same level of complexity as for today's standard decoders and can be seen to operate very close to the theoretical bounds.

To properly validated the theoretical and simulation work of ESA and NASA, and to confirm the advantages of the selected turbo codes, a contract with Politecnico di Torino has been kicked off which foresees the development of the specified turbo decoders on a commercial Digital Signal Processor (DSP). This decoder will be first tested by the end of this year by implementing the turbo encoder on a fast PC platform. Later, the decoder will be placed into the ESA reference station at ESOC to be connected to the standard Earth station demodulator to evaluate the end-to-end performance. It is also expected that it will be sufficient for evaluating the coding performance at FER = 10^{-6}, for which only semi-analytical estimates of the coding gain are available today. Finally, the turbo decoder will be tested operationally in the year 2001 on Smart-1 since the turbo encoder is an experiment onboard this technology demonstration mission and therefore does not require a fully operational decoder at the Earth station. Development and deployment of operational decoders will follow in time for the Rosetta and the Mars Express missions (to be launched in 2003).

9 CONCLUSIONS

Turbo codes introduced in 1993 have been extensively studied by ESA, NASA and other space agencies to evaluate their applicability to space systems. The studies concentrated on the inter-agency CCSDS frame level service and came out with a set of proposed codes for adoption as CCSDS recommendations. Such codes, which are of the same complexity as for today's concatenated code or even less complex, have additional gains ranging from 1.7 to 2.7 dB depending on the selected code rate and the desired frame error rate. Pending final adoption at CCSDS level expected in late 1998, ESA is initiating the development of the required onboard chips and ground station equipment which are foreseen to be used for the first time with the Smart-1 mission in 2001.

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