CCSDS TELEMETRY CHANNEL CODING: THE TURBO CODING OPTION

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ABSTRACT

As of 1993 a new coding concept promising gains as close as 0.5 dB to the Shannon limit on Bit Error Rates was introduced by Berrou et al. The coding scheme called Turbo Coding [1] achieved immediately worldwide attention.

After the first discussions in the May 96 Meeting of the Consultative Committee for Space Data Systems (CCSDS), it was decided - in agreement with NASA and other national space agencies - to include a set of turbo codes in a new issue of the CCSDS telemetry channel coding recommendation. Turbo coding will be an add-on option to the recommendations without modifying the existing coding schemes and will retain compatibility with the CCSDS Packet Telemetry recommendation. *Pink sheets* updating the recommendation are currently being reviewed to formally establish turbo coding as an alternative to both Reed-Solomon and Convolutional coding for deep space and near-Earth missions.

This paper presents the turbo codes that are being proposed for the recommendation, and their expected higher coding gain with respect to the present encoding schemes.

1 Introduction

As of 1993 a new coding concept promising gains as close as 0.5 dB to the Shannon limit on Bit Error Rates was introduced [2] by Berrou et al. The coding scheme called Turbo Coding achieved immediately worldwide attention with both NASA and ESA playing a very active role in studying its application to space missions. For ESA the Turbo Coding option appeared very appealing in view of Rosetta, i.e. the most demanding ESA mission ever from the point of view of Earth station capabilities. For supporting the mission via ESA only facilities, the development of the first ESA Deep Space antenna to be located at Perth, Australia has been initiated. Notwithstanding the performance of such an antenna – with a diameter of 35 meters, cryogenically cooled Low Noise Amplifiers reaching a noise temperature of 10ºK, PLL receivers with bandwidth as narrow as 0.3 Hz, etc. – the return link margins are just met in nominal conditions with no extra margins to account for emergencies or performance degradation for a mission with a nominal lifetime of about 11 years, and Earth distances to some 6.25 AU.

After the first discussions in the May 96 Meeting when Turbo Codes were presented to CCSDS Sub Panels 1A and 1E for information, along with the main ESA-NASA coding activities, a study contract was let by ESA to the Communications Group of Politecnico di Torino that had already studied the emerging Turbo Codes [5] [6]. One starting point was the fact that the end product for CCSDS is the received frame instead of the received bit. In fact all the Turbo Codes papers available in literature at that time only dealt with bit error rates (BER). For this reason the investigation target of Frame Error Rates (FER) was specified hoping that the performance on FER could be as good as on BER. The aim of such study was to develop design criteria aimed at finding Turbo codes with a gain of about 1.5 dB at FER = $1*10^{-4}$ or lower, with respect to the CCSDS standard concatenated code [1] adopted as baseline for Rosetta.

[1] Turbo Code: license France Telecom & Telediffusion de France.

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In the October 96 Meeting, Turbo Codes were proposed to Sub Panel 1A as study item for potential adoption as CCSDS standard code(s) for inter-agency support. At Spring 1997 Meeting the White Book Issue 1 was officially presented and discussed jointly by Sub Panels 1A and 1E to establish the CCSDS baseline. The first FER curves were also presented and an algorithmic interleaver was proposed by Prof. Berrou to avoid the need of "big" on-board ROMs. In the 1997 Fall Meeting, White Book Issue 2 was discussed: the various attached Sync Markers were proposed and the CRC for the Frame Error Control Field made mandatory. During 1998 Meetings, the Channel Coding Pink Sheets have been reviewed by Sub Panel 1A. Today, a few small but essential questions for the best recommendation are about to be answered aiming at submission of the Pink Sheets to Member Agencies Review before the end of the year. This will formally establish turbo coding as an alternative to both Reed-Solomon and Convolutional coding for deep space and near-Earth missions demanding higher coding gains.

2 The coding options

The coding scheme recommended by CCSDS is the concatenated Reed-Solomon (255,223) and convolutional (rate 1/2, 64 states) code for which both ESA and NASA have coders and decoders available "off-the-shelf". With an interleaving depth of 5 of the R-S code, the Rosetta frame error rate is met when the bit signal-to-noise ratio (SNR) Eb/No is greater than 2.6 dB. The performance of this code is shown in fig. 1 where (indicated as VD+R-S) it is compared with the uncoded (PSK), the Reed-Solomon (R-S) and the convolutional (VD) performance.

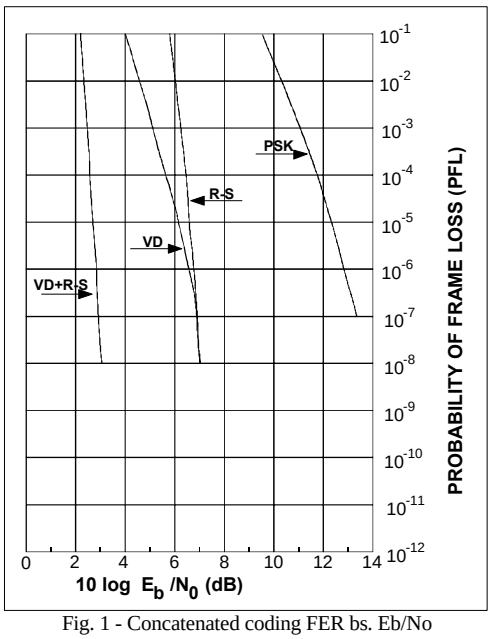


Fig. 1 - Concatenated coding FER bs. Eb/No

The Turbo codes are generated by parallel concatenations of two, or more, convolutional codes called the constituent codes. The input (telemetry) information bits are sent to the first encoder and, after being scrambled by an interleaver, to the second encoder. These codes can be decoded using iteratively soft-input soft-output algorithms working on the constituent codes, having a complexity comparable to that of the existing CCSDS-based decoders. Due to the interleaver size, Turbo codes have been shown to provide coding gains close to the theoretical Shannon limits on Bit Error Rate (BER) with improvement over the CCSDS codes of more than 2 dB [3], [4]. However, the performance of the codes on FER, and, with channel impairments other than additive white gaussian noise (AWGN) could not be found in literature.

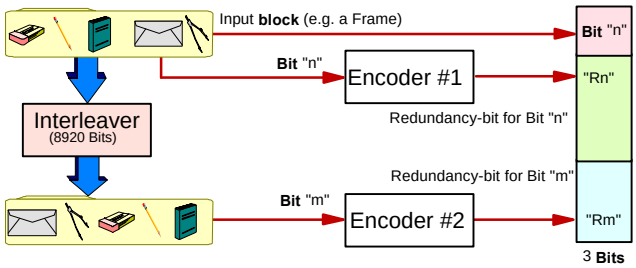


Fig. 2 - A Systematic Turbo Code Encoder

3 The Turbo codes theory

As mentioned above, "Turbo Codes" are parallel concatenation of two (or more) convolutional codes. Fig. 2 shows an example of a (systematic) Turbo code encoder made up of two recursive convolutional encoders. The first encoder operates on the information (telemetry) bit sequence directly whereas the second encoder receives the information sequence in a re-ordered manner via the interleaver (sometimes called also "permuter") which is basically a pseudo-random scrambling device. A complete block is read bit-by-bit into the interleaver and read out in a specified random order. Generalization of this concept to several convolutional encoders with different constraint lengths and rates is possible. As the interleaver is part of the whole encoder, increasing its size leads to a larger code memory and hence, in general, to better bit error rate performance. However, for the same reason, the analytical evaluation of the Maximum Likelihood (ML) performance of Turbo codes using a given interleaver becomes an exceptionally hard task for large interleaver sizes (N). As explained in [5], [6], a bound on BER performance can be found by introducing the concept of a *uniform interleaver,* a device that maps an input word of weight w into all its $\binom{k}{w}$ distinct permutations, each with probability $1/\binom{k}{w}$. For recursive constituent codes, and with N significantly larger than the constituent code memory, the interleaver gain is a reduction of the BER by a factor 1/N [6]. The penalty of large N is the decoding delay (latency) which is not important for Rosetta. Furthermore, performance improvements can be obtained at low BER by increasing the complexity of the constituent codes [5] (higher number of states.)

As the interleaving size is normally large, maximum likelihood decoding is out of the question for complexity reasons. However, a suboptimal decoder implementing multiple iterations around a maximum a posteriori (MAP) decoder as proposed in [2] is of the same level of complexity of today's standard decoders and can be seen to operate very close to the theoretical bounds. The following sections show the results obtained on FER by Politecnico di Torino, Italy [7].

3.1 Determining performance bounds

The initial activities were based on the concept of uniform interleaver and started with optimization of the constituent codes according to the union bounding technique (maximum likelihood performance), thereby determining the upper limits of the code performance. Examination of the literature on Turbo codes helped reducing the search domain to systematic codes made up by only two constituent codes, both recursive convolutional with 8, 16 and 32 states. For this case, it can be seen [7] that the frame error rate can be approximated by the following equation:

$$P(e) \approx \sum_{z=d_{fP}}^{\infty} C_z \, N^{a(z)} \, erfc\left(\sqrt{\frac{z \, Rc \, Eb}{No}}\right) \quad (1)$$

where the constant C_z depends on the constituent codes, N is the interleaver length, Eb/No is the bit SNR, Rc is the code rate. $\alpha(z)$ is the most important parameter for selecting the constituent codes.

Two particular values of $\alpha(z)$ are of importance in the code design: $\alpha(d_{fP})$ where d_{fP} is the free distance of the code which determines the performance at medium-high SNR, and $\max_z \alpha(z)$ which gives the dominant term for an arbitrary large interleaver ($N \rightarrow \infty$.) The corresponding value of z is called effective free distance $d_{fP,\,eff}$, the distance produced by errors of weight 2 which are the most probable errors after the interleaver. It can be seen from the approximation of P(e) for $N \rightarrow \infty$:

$$P(e) \approx \tfrac{1}{4} \, N_{f1,eff} \, N_{f2,eff} \, erfc\left(\sqrt{\frac{d_{fP,eff} \, Rc \, Eb}{No}}\right) \quad (2)$$

where $d_{fP,eff} = d_{f1,eff} + d_{f2,eff}$ that the choice of the constituent codes has to be based on maximizing the effective free distance while minimizing the multiplicity of the error events by input sequences of weight 2.

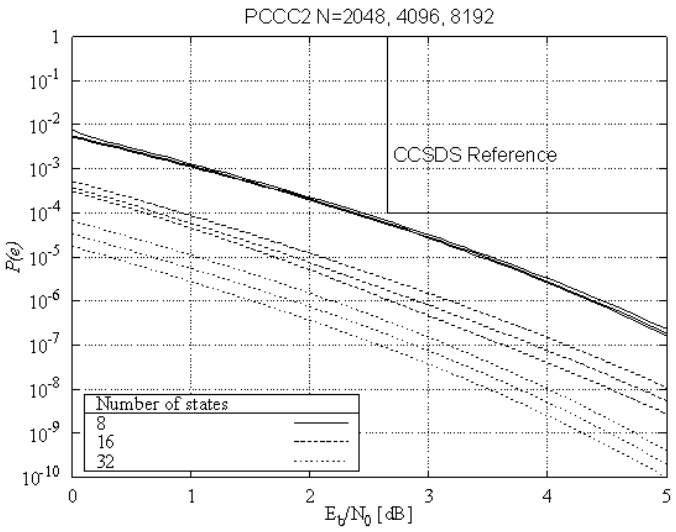
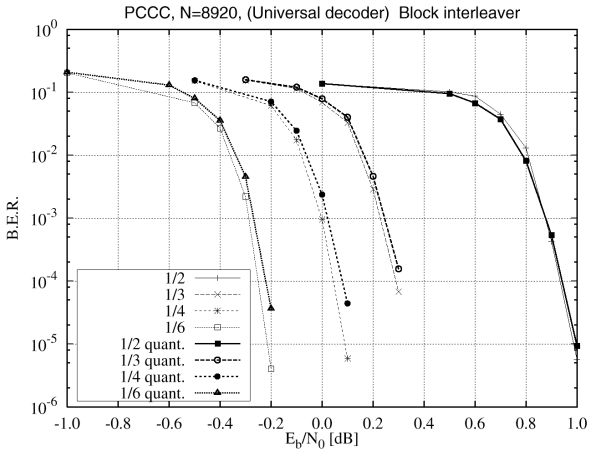


Fig. 3 - FER vs. Eb/No bounds for proposed rate 1/2 Turbo codes

Based on such criteria, a set of candidate codes was found. A simple rate 1/2 code can be generated by concatenation of a rate 2/3 16-state systematic recursive convolutional code with a rate 2/1 code generated from the first one by elimination of the two systematic symbols. The FER maximum likelihood bound of the resulting rate 1/2 code can be seen in figure 3 where also the effect of different interleaver lengths and number of states is shown. At the required FER of 10^{-4} the 16-state code showed a theoretical gain of about 1.6 dB over the CCSDS reference, just what is needed for Rosetta. Since theoretical bounds are based on maximum likelihood decoding whereas any practical implementation of Turbo decoder is based on the MAP algorithm, the actual performance may diverge from the bound. Therefore, a series of more performing lower rate codes (1/3, 1/4 and 1/6) was also investigated. A rate 1/6 code can be obtained by using a rate 1/4 recursive 16-state systematic encoder in parallel with a rate 1/2 encoder. The FER bounds for an interleaver size of 8192 bits the bound of the proposed rate 1/6 code showed a gain of about 2.7 dB over the CCSDS code.

3.2 Validating bounds by simulations

Having selected a series of potential codes and determined the performance bounds analytically, the second step consisted in simulating the iterative decoding algorithm of such codes and comparing the resulting performance with the theoretical bounds.



Code Rate	Improvement [dB] @ FER = 10^{-4}	Improvement [dB] @ FER = 10^{-6}
1/2	**1.7**	**≈ 1.2**
2/5	**2.0**	**≈ 1.6**
1/3	**2.3**	**≈ 2.0**
1/4	**2.5**	**≈ 2.0**
1/6	**2.7**	**≈ 2.0**

Fig.4 - Summary of BER Simulation Results and estimated FER improvement against current CCSDS concatenated coding scheme

With the actual spread interleaver of length *N*=8920 the decoder was simulated using the iterative decoding scheme that makes use of two *a-posteriori probability* algorithms, one for each convolutional code, obtaining the true coding gain at FER=10^{-4} through the simulation of 200 million bits per signal-to-noise ratio point. In the practical impossibility of estimating FERs as low as 10^{-6}, a new extrapolation technique was devised which is based on the evaluation of the distance spectrum of the PCCCs, yielding reasonably accurate estimate of the coding gains at FER=10^{-6}. The BER results are shown in Fig. 4 together with the estimated FER improvement against current CCSDS concatenated coding scheme.

4 The CCSDS Recommendation

The first obvious target given to CCSDS members has been the search for good constituent codes for the definition of a CCSDS

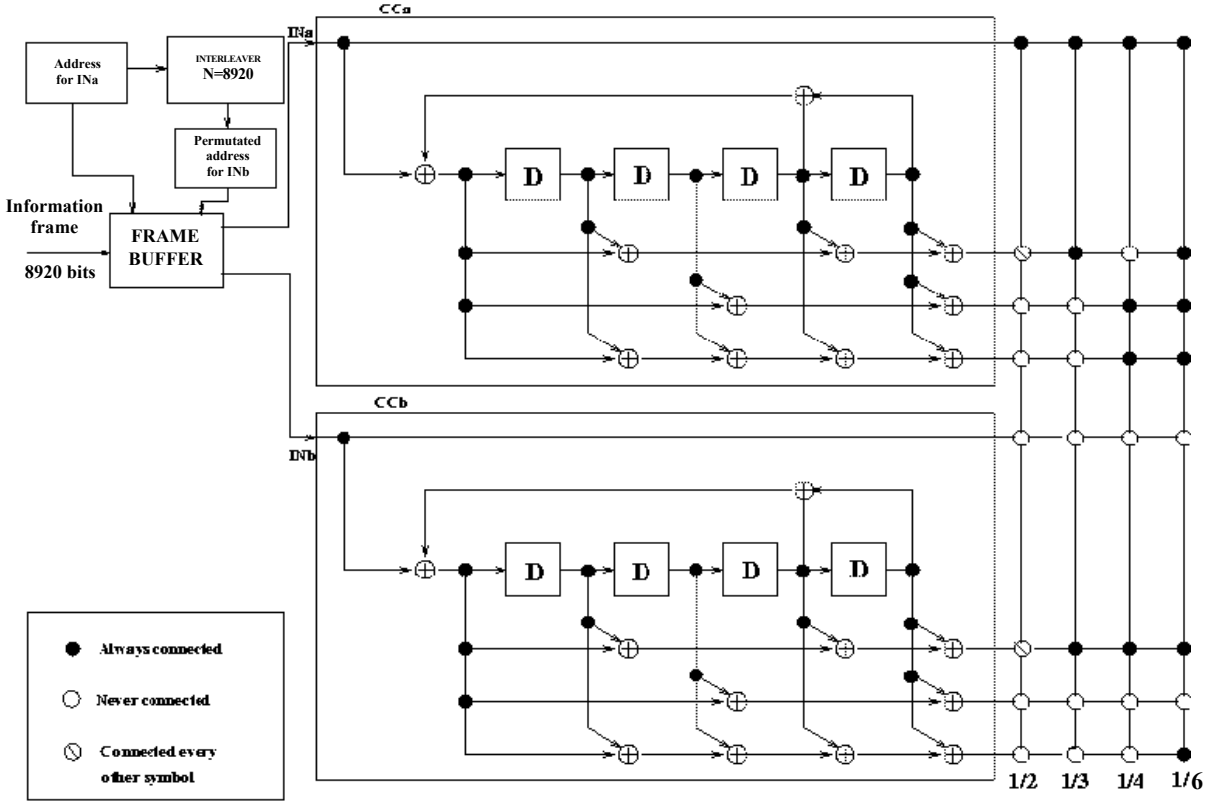


Fig. 5 - One of the proposed CCSDS Turbo Code Encoders

encoder capable of supporting different code rates; i.e. 1/2, 1/3, 1/4 and 1/6. Today agreement about the codes for rates 1/2, 1/3 and 1/4 has been reached while for the rate 1/6 some investigations are still to be performed to finally select one of two proposed choices. Fig. 5 shows one of the two proposed CCSDS Turbo Encoders. It differs from the other alternative only with respect to the rate 1/6 code and, as the other one, can generate all the required rates according to the selected puncturing.

In addition to the search for good constituent codes, a big effort has been made to assure compatibility with pre-existing devices and choices. For this reason, the five possible values for the Frame length shown in Table 1 have been allowed. While the last one has been selected for highest coding gain being the biggest supported by the current Packet Telemetry Frame format, the first four values are fully compatible with Frame Length values selected for e.g. Reed-Solomon encoding. Table 2 shows the various possible Codeblock lengths (i.e. the transmitted number of bits).

5 The Ground Segment

Information block length k, bits	Corresponding Reed-Solomon interleaving depth I	Notes
1784 (=223 × 1 octets)	1	For very low data rates or low latency
3568 (=223 × 2 octets)	2	
7136 (=223 × 4 octets)	4	
8920 (=223 × 5 octets)	5	
16384		For highest coding gain

Table 1: Specified information block lengths

Information block length k, bits	Codeblock length n, bits			
	rate 1/2	rate 1/3	rate 1/4	rate 1/6
1784	3576	5352	7152	10704
3568	7144	10704	14288	21408
7136	14280	21420	28560	42840
8920	17848	26772	35696	53544
16384	32776	49164	65552	98328

Table 2: Codeblock lengths for supported code rates

Politecnico of Torino on behalf of ESA is currently implementing a proof-of-concept Digital Signal Processor (DSP) Turbo Codes Decoder [10] and is quite close to its finalization. After a comparison of the DSP's available off-the-shelf on the basis of their suitability to the specific requirements of a Turbo Decoder implementation, the Texas Instruments "TMS320C6201" - a DSP chip allowing high level of parallel processing - has been selected. The software has been written in two versions: both in C and in the DSP assembler language. The latter has then been optimized with respect to both memory usage and parallel processing. The system embedding the DSP board implementing the ESA-CCSDS Turbo decoder was demonstrated to ESA in September 1998 and it is already heavily used to obtain fast and reliable results about the remaining CCSDS open questions.

The initial 160-MHz chip allowed, for all the code rates 1/2, 1/3, 1/4 and 1/6, decoding up to about 40 kbps information rate. The 200-MHz chip, just arrived at the end of October, has extended the supported information rate to almost 60 kbps. One of the reasons for such a high speed (compared to previous similar recent implementation) is also due to the very symmetrical nature of the Turbo Encoder that allowed the design of a so called "Universal Decoder" applicable to all the code rates without penalties in efficiency and performances.

6 The Space Segment

The development of the turbo encoder for the space segment follows the same approach that was taken by the Agency for the development of the radiation hard MS13544 device [9]. That design was based on Reed-Solomon and Convolutional encoder cores initially developed at the European Space Research and Technology Centre (ESTEC). By having in-house developed encoder cores that are technology independent, the Agency can act as a virtual second source to a foundry manufacturing a device incorporating them. The following sections address the development of the turbo encoder core, the Smart-1 implementation and future system-on-a-chip integration.

6.1 Turbo Encoder Core

The turbo encoder core supports the full CCSDS recommendation, including all frame lengths and code rates. The on-chip algorithmic interleaver is implemented in accordance with Prof. Berrou. The encoder core is technology independent to allow implementation in various technologies, commercial amongst others. The Very High Speed Integrated Circuit Hardware Description Language (VHDL) has been used. The supported data rates depend on the technology used for implementing the encoder. However, the core is targeted towards output data rates beyond 5MHz when implemented in an Field Programmable Gate Array (FPGA) with an external frame memory. The encoder core development was completed in October 1998.

It is foreseen to validate the turbo encoder core by exchanging coded frames with the developers of the turbo decoders. The validation is foreseen to be based on CCSDS transfer frames generated through simulation of existing VHDL models. This enables end-to-end validation, including the interface between the turbo decoder and the ground station equipment. It is also the intention to exchange coded frames with other CCSDS members. Ultimately, a reference data base of correctly coded frames will be established. The purpose of the data base is to support companies developing encoders and decoders.

6.2 FPGA Implementation for SMART-1

Turbo encoding is being proposed as part of an experimental transponder onboard the Smart-1 satellite. With the baseline being Reed-Solomon encoding on Smart-1, it is required that the turbo encoder is either implemented in the experimental transponder itself or in the telemetry encoder.

The Smart-1 turbo encoder will as a baseline be implemented in an Actel 14100 FPGA. Ongoing technology activities have shown that the selected device type has good radiation characteristics. The frame buffer memory will be placed external to the FPGA and is planned to be implemented with an off-the-shelf radiation tolerant memory. The development should be finalised in June 1999 to meet the overall schedule of the transponder and the telemetry encoder.

6.3 ASIC Implementations

The next step might be to integrate the encoder core together with the required frame buffer memory in an ASIC. This would increase overall reliability and reduce power consumption and required board area. An ASIC development will be initiated provided there is sufficient interest from industry and projects.

For future missions with even higher requirements on power and area consumption, the turbo encoder could be combined with the telemetry encoder and the telecommand decoder on a single chip. With such a device, that the user would be free to select between turbo or Reed-Solomon encoding. The channel coding cores for this type of development are already in place.

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