ASIC 121
Practical VHDL Digital Design for FPGAs
Fall 2006

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Resources

Website:	http://asic.uwaterloo.ca Check the Resources tab
Location:	Wednesdays 6-7pm, RCH 109 *Note: This is subject to change, check the ASIC website.*

Course Outline

The goal of this tutorial series will be to provide ASIC members with practical knowledge of digital hardware design. Very little emphasis will be placed on theory, only the basics will be taught and the rest left to courses such as ECE 222, 223, 324, and 427.

All focus will be placed on practical examples that will be useful in industry. VHDL will be used as the hardware description language in all exercises. We will assume that the VHDL will be targeted for synthesis on an FPGA.

Each tutorial will have an assignment that members must perform at home. This will allow members to get familiar with the tools used in industry and to experiment on their own.

The main project of the tutorial series will be the implementation of a simple 16-bit processor in VHDL. The design work will be done in tutorials but most of the implementation will be performed independently.

Topics

1. Basics of Digital Design: Logic Gates, Flip Flops, Basic Structures (MUX, Adders)
2. VHDL: Basic Syntax, State Machines, Simple Example: Full Adder
3. FPGA Basics: Structure, Features, Recap of Design tools. Using FIFOs.
4. Processor Design: Design of an ALU. Bus. Simple instruction decoder.
5. Processor Design: Simple Testbenches.
6. Processor Design: Memory Blocks. Instruction Set.
7. Processor Design: Writing an Assembler. (If time permits)
8. Processor Design: Retargetting a Compiler. (If time permits)

Contributions

I would like to thank Jeff Wentworth for his fantastic ASIC 120 tutorial series. Some of the material used in this series is based on his tutorials.