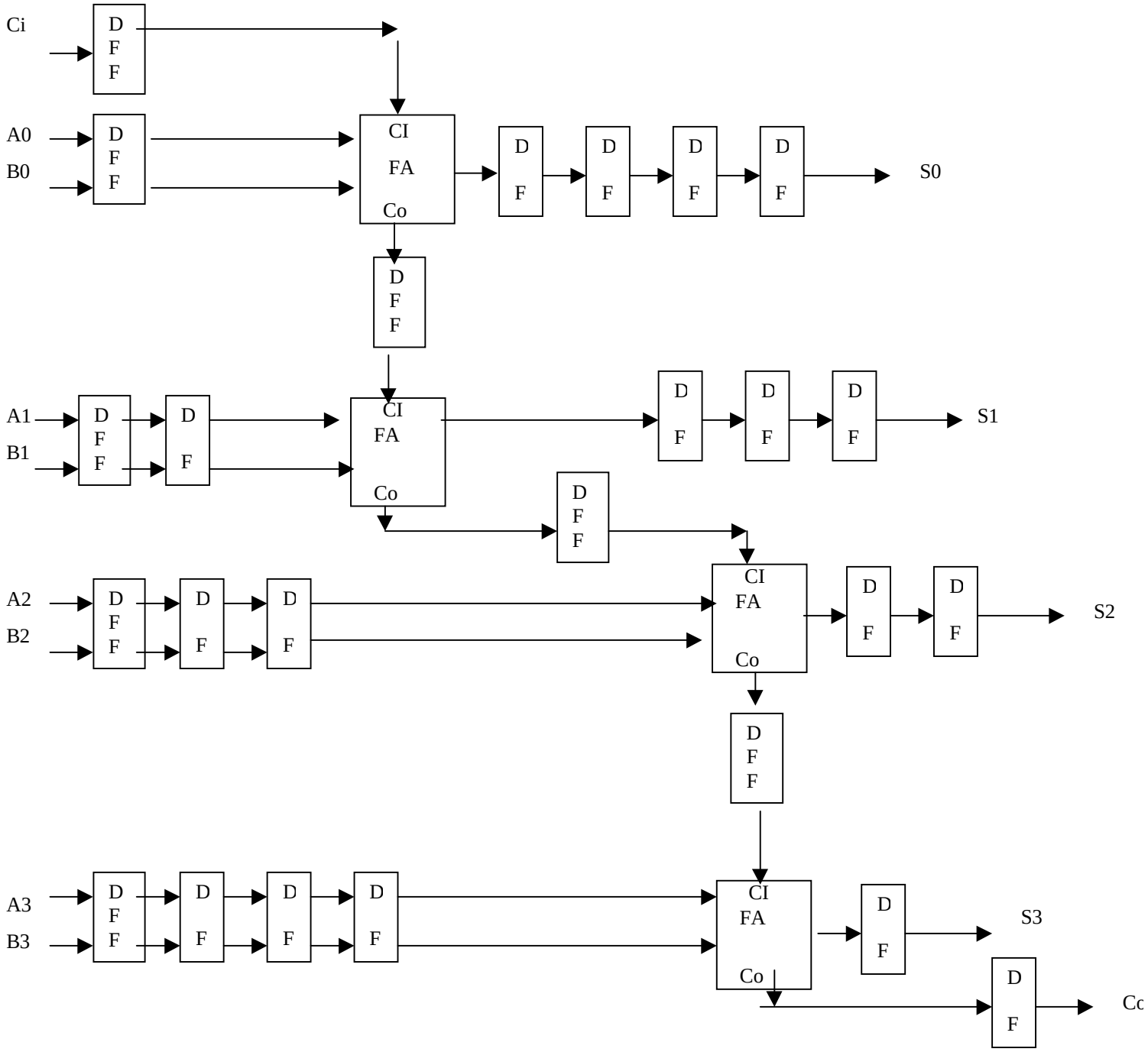
EE 4743 Test 1 Solutions - Spring 2000 – Reese

1. (15ts) Figure #1 shows a ripple carry adder. I want you to pipeline the ripple carry adder so that there is a DFF between every Full Adder and all inputs/outputs are registered through DFFs. You **must maintain data synchronization** inside of your design. Draw a schematic showing your work.



2. (15 pts) Give the equations for computing the following timing characteristics within a design (be sure to use words like “maximum”, “minimum” where appropriate). Also draw a block diagram that illustrates your timing components**. SEE NOTES**

3. (15 pts) The diagram in Figure 2 shows two ASICs connected together and also gives datasheets for each ASIC. The internal CLOCK of each ASIC is the same as the external clock (there is no clock multiplication or division of the clock in the ASIC.

Show work for partial credit

FOR THIS SYSTEM compute:

a. The maximum external clock speed (in Mhz) for the datasheet TABLES labeled as PART A.

Paths: Reg-Reg ASIC #1 = 1/10ns = 100 Mhz
Reg-Reg ASIC #2 = 1/15 ns = **67 Mhz**
ASIC #1 to ASIC #2 = 7 (clk to out #1) + 4 (setup #2) = 11ns = 1/11ns = 91 Mhz
ASIC #2 to ASIC #1 = 5 (clk to out #2) + 3 (setup #1) = 8 ns = 1/8 ns = 125 Mhz

MAXIMUM clock speed will 67 Mhz (slowest path)

b. The maximum external clock speed (in Mhz) for the datasheet TABLES labeled as PART B

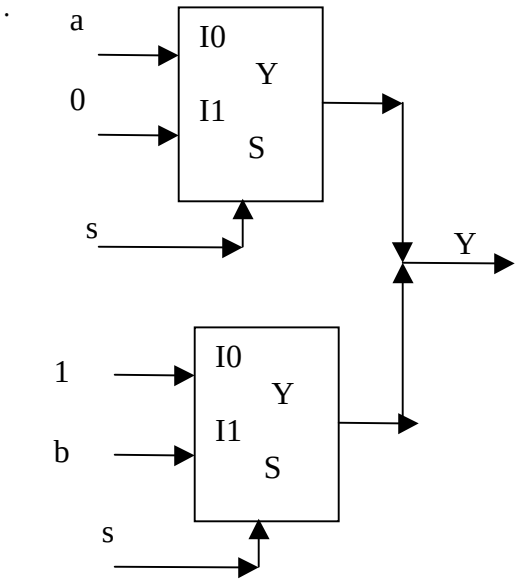
Paths: Reg-Reg ASIC #1 = 1/10ns = 100 Mhz
Reg-Reg ASIC #2 = 1/11 ns = 91 Mhz
ASIC #1 to ASIC #2 = 7 (clk to out #1) + 4 (setup #2) = 11ns = 1/11ns = 91 Mhz
ASIC #2 to ASIC #1 = 10 (clk to out #2) + 3 (setup #1) = 13 ns = 1/13 ns = **77 Mhz**

MAXIMUM clock speed will 77 Mhz (slowest path)

4. (10 pts) A poor attempt at a VHDL architecture for a 2-to-1 mux is shown below.:

```
Architecture a of mux2to1 is
   Begin
        Y <= a when (s = '0') else '0';
        Y <= b when (s= '1') else '1';
End a;
```

This obviously does not synthesize a 2to1 mux. Show the logic that is actually synthesized.



5. (20 pts)The entity declaration for a 4 bit combinational shifter block is shown below:

```
Entity  myshift is
        Port (    din:  in std_logic_vector(3 downto 0);
                  sl:   in std_logic;
                  sr:  in std_logic;
                  sl_in  :   in std_logic;
                 sr_in  : in std_logic;
                dout:   out std_logic_vector(3 downto 0)
              )
 End myshift;
```

The shifter has the following functionality:

sl=0, sr= 0	:	dout equals to din
sl=1, sr=0		dout is din shifted left by 1 position, new LSB of dout is sl_in
sl=0, sr=1		dout is din shifted right by 1 position, new MSB of dout is sr_in
sl=1, sr =1		dout equals to 1's complement of din (NOT of din)

Write the VHDL architecture for this block.

```
Process (din, sl, sr, sl_in, sr_in)
   Begin
      Din <= dout;
     If (sl = '1' and sr = '0') then
       Dout(0) <= sl_in;
       Dout(3 downto 1) <= din(2 downto 0);
    End if;
 If (sr = '1' and sl = '0') then
       Dout(3) <= sr_in;
       Dout(2 downto 0) <= din(3 downto 1);
    End if;
If (sr = '1' and sl = '1') then
    Dout <= not din;
   End if;
End process;
```

6. (25 pts) Short Answer (answer 5 out of 6)

a. List the three ASIC implementation technologies we discussed.
Full Custom, Gate Array, Standard cell

b. One of these ASIC technologies has a distinct advantage over the others in terms of manufacturing time - which one is it? Gate Array

c. List the three programmable logic implementation technologies we discussed.
PLDs, CPLDs, FPGA

d. What is NRE and what type of implementation technology (ASIC or programmable) has a higher NRE???
Non Recoverable Engineering Costs, ASIC has highest since chip has to be fabricated.

e. Why are monolithic SRAM blocks included on most high density programmable logic devices these days? Need DATA close to gates, faster to access data on chip than off chip.

f. What is an architectural design technique for reducing register-to-register delay within a design?
Pipelining

Figure 1: Ripple Carry

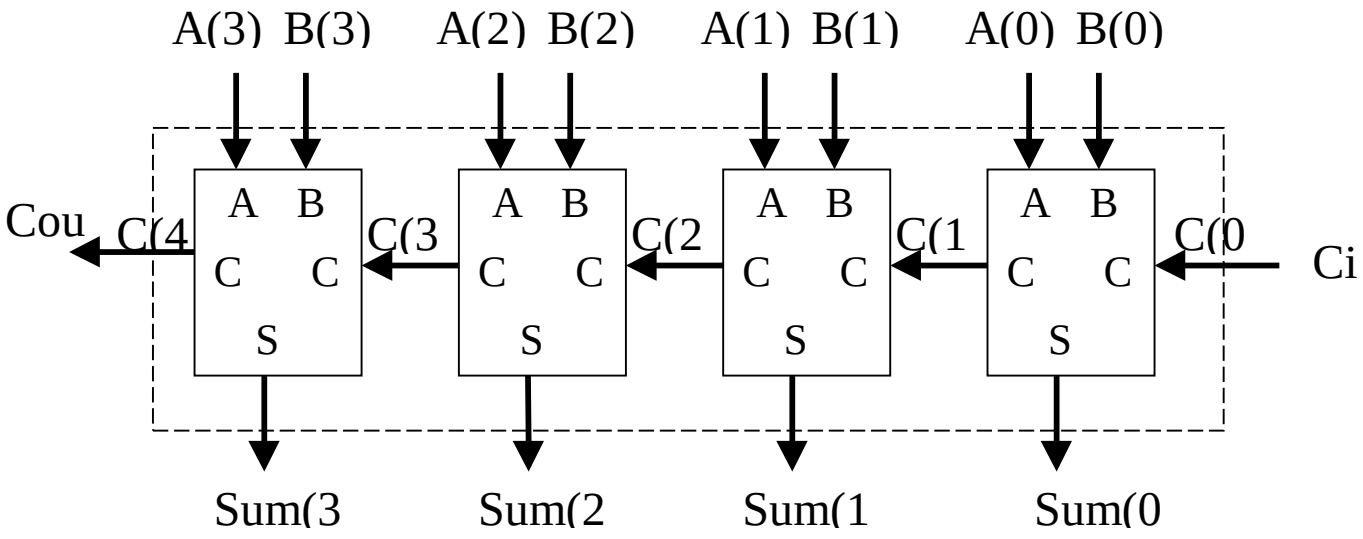
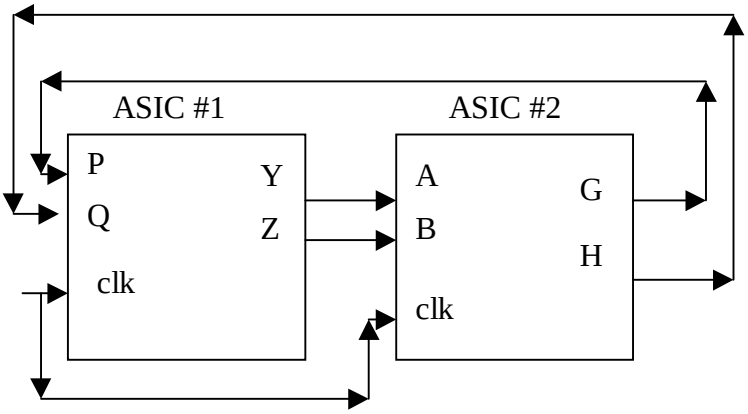


Figure #2



PART A:

ASIC #1

Parameter	Value
Reg to Reg Delay	10 ns
Clk to Any output	7 ns
Setup time (any input)	3 ns
Hold Time (any input)	2 ns

ASIC #2

Parameter	Value
Reg to Reg Delay	15 ns
Clk to Any output	5 ns
Setup time (any input)	4 ns
Hold Time (any input)	3 ns

PART B:

Table for ASIC #1 is the same.

ASIC #2

Parameter	Value
Reg to Reg Delay	11 ns
Clk to Any output	10 ns
Setup time (any input)	4 ns
Hold Time (any input)	3 ns