For:reese
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Test #1 – EE 4743 – Fall 1998 My Name is: _____

You have **50 minutes** to complete this test. Good luck!

1. (20 pts.) Answer the following questions.

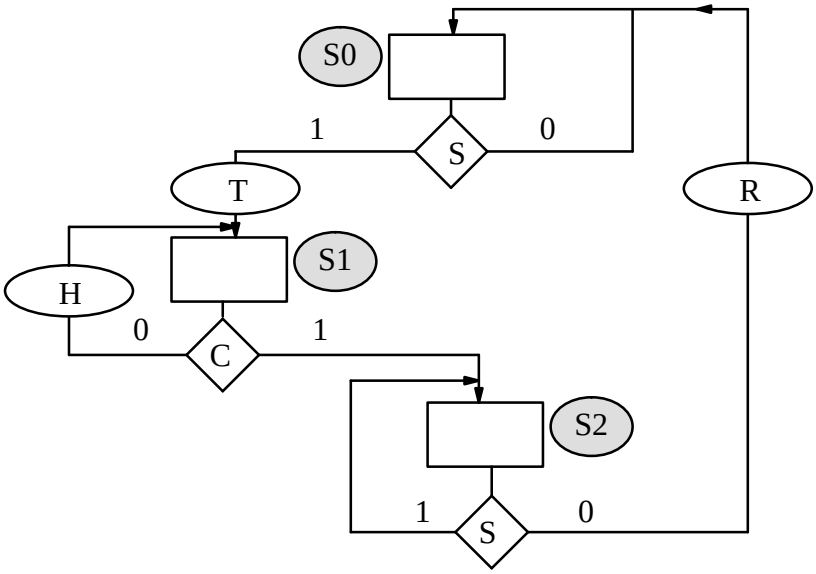
a. Which is smaller—a one–time–programmable logic interconnection or a reprogrammable logic interconnection? For example, would you expect a one–time–programmable logic part to be "small and fast" or "large and slow" compared to a repogrammable one?

b. Which implementation technology consists of a prefabricated array of transistors in which the last few metal layers are left blank, so that they can be customized to wire up the transistors?

c. Full custom and standard cell have the highest initial cost. (That is, they have the highest cost at very low levels of production.) Why?

d. Which state encoding strategy attempts to reduce glitches? Name one.

2. (50 pts) Consider the following ASM chart.



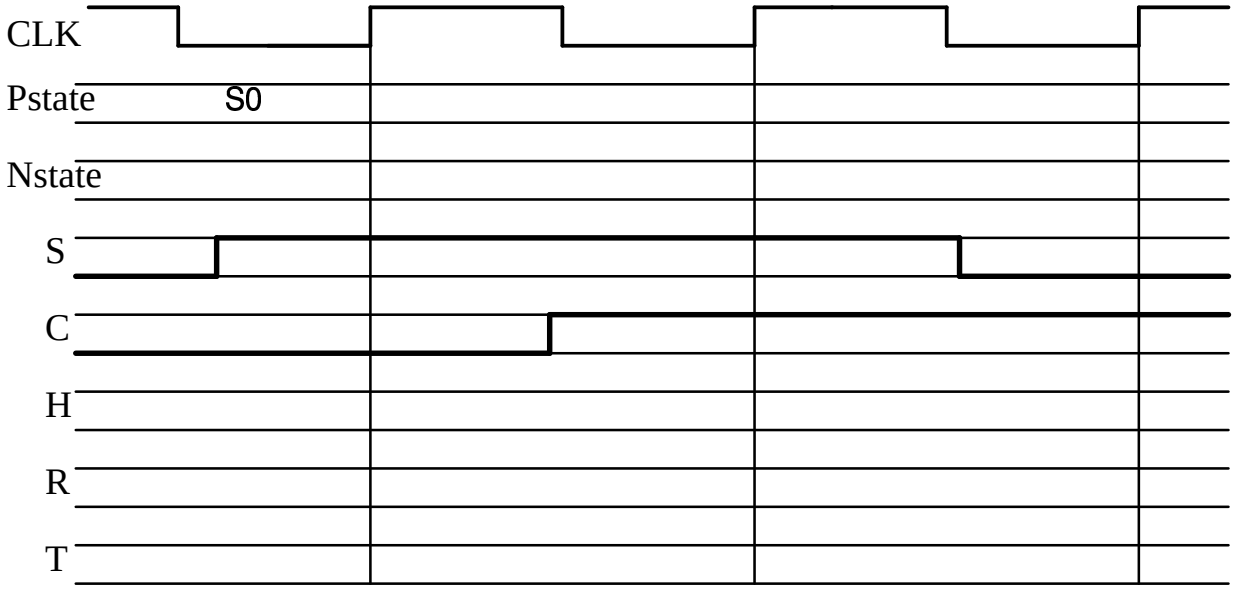
a. Write a VHDL code that implements it. You can ignore the reset logic. *Use conventional state encoding.*

```
entity asm is port(
   signal s,c,clk: in std_logic;

   signal ____________________: out std_logic
);
end asm;

architecture behavior of asm is

-- put constants here
-- example of syntax: constant S0: std_logic_vector(X downto 0) := B"0...0";




signal pstate,nstate: std_logic_vector(1 downto 0); -- present and next state

begin

dffs:process (                                                    )
begin
-- dff logic here




end process;

c_logic:process(                                                  )
begin
-- state logic here
-- Don't forget to assign default values to all outputs
```

```
--Case syntax: case <name> is ... when <value> =>
```

```
end process c_logic;
end behavior;
```

b. Complete the following timing diagram for the code and chart. Assume all flip–flops are rising–edge triggered.



c. Complete the following table about state encoding methods. First, answer whether it is possible to use the indicated method for the ASM chart shown above. Second, if it is possible, answer how many state bits would be needed to use that method.

Method	Possible?	No. of State Bits Needed
Conventional		
Gray–Code		
1–Hot		
One–Cycle–Early		
Output Encoding		

3. (30 pts) Consider the following VHDL code.

```
library ieee;
use ieee.std_logic_1164.all;

entity pulsedet is port(
   signal clk,reset,pulse_in: in std_logic;
   signal pulse_out: out std_logic
);
end pulsedet;

architecture behavior of pulsedet is

signal dffout : std_logic_vector(2 downto 0);

begin

dffs: process(clk,reset)
begin
if (reset = '1') then
   dffout <= "000";
elsif (clk'event and clk='1') then
   dffout(2) <= dffout(1);
   dffout(1) <= dffout(0);
   dffout(0) <= pulse_in;
end if;
end process;

pulse_out <= dffout(2) and not dffout(1);

end behavior;
```

Draw a diagram of logic that implements the VHDL code. (I want to see logic gates and D flip–flops.)