EE 4743 Test #1 - Spring 1999 – Reese

SSN: _____ (no names please)

PART 1: Answer   17 questions out of questions 1-20. MARK out the three questions that you DO NOT want me to grade.

Bonus: Answer either question 21 or question 22.

1.   What is the common combinational function implemented by the VHDL process block below? You may draw a symbol, gating, truth table, etc to give me your answer. Signals A,B,S are inputs, Y is an output.

    process (A,B,S)
    begin
        Y <= A;
        If (S = '1') then
        Y <= B;
        end if;
     end process;

2.   How do I declare an 8-bit bus port in VHDL?   Give me an example (either input or output port).

3.   Draw the structure for a 4-bit ripple carry adder. The inputs are A[3..0], B[3..0], Cin. The outputs are Sum[3..0], Cout.

4.   If I have an FPGA that uses LUTs to implement logic, then will this FPGA require configuration on power up? EXPLAIN WHY!!!!!!!

5.   On FPGAs that use LUTs, I can build larger SRAMs out of individual LUTs. However, most FPGAs include monolithic blocks of SRAMs. What are the advantages of a monolithic SRAM block over a SRAM built from LUTs and why do these advantages occur?

6. When would I choose a gate array implementation technology over an FPGA implementation technology?

7. Most FPGAs have a few dedicated low-skew, high-drive nets called global nets. What are these nets used for? Be explicit.

8. The Actel FPGA is a one-time programmable FPGA. It is not LUT-based, and has considerably less density than the Altera or Xilinx FPGAs. When might I consider using the Actel FPGA over the Altera or Xilinx FPGAs?

9. I have an 8-bit hex number of the value $A0 (binary = 1010 0000). Write the decimal equivalent for
    a) An unsigned integer (8.0 fixed point format) _____

    b) decimal point all the way to the left (0.8 fixed point format) _____

    c) xx.xxxxxx format (2.6 fixed point format) _____

10. What is the benefit of a saturating adder over a normal binary adder? Draw a block diagram of a saturating adder for unsigned numbers.

11. In Lab exercise #2, we had an 8-bit X 8 bit multiplier that produced a 8-bit result. Normally, a 8x8 multiply will produce a 16 bit result. Which bits of the final product did we throw away? Why could we throw these bits away?

12. What is the cascade chain used for in the Altera Flex 10K family? Explain any advantages that arise from using the cascade chain.

13. What is the carry chain used for in the Altera Flex 10K family? Explain any advantages that arise from using the carry chain.

14. We looked at some low voltage, high speed IO interfaces supported the Xilinx Virtex family. These make references to a 'Vt' and a 'Vref'. What do these mean? Explain.

15. What is the advantage(s) of a gate array implementation over a standard cell or full custom implementation?

16. When you did combinational delay analysis in the Maxplus tool, it would present a matrix of delays. What was along the left edge of the matrix and what was along the top of matrix? What values were contained in the matrix entries? Show an example.

17. Many FPGA families offer 3.3v power supply versions of their families in addition to 5v power supply versions. What is driving the trend to lower power supply voltages?

18. Many FPGA vendors include a Phase Locked Loop or Delay Locked Loop capability. What is the function of a PLL or DLL?

19. The Actel FPGA used a logic element that consisted of three 2/1 muxes plus a 2-input AND gate. On the 2-1 mux shown below, how would I connect the inputs to implement Y = A + B (the mux inputs can be connected to 'A', 'B', '1', '0')

20. In class and in the notes, I mentioned a problem about output signals inside of a process block. If there is a path through the process block, such that a value does not get assigned to the output signal, then something extra gets generated in the synthesized logic. As an example, the 'good process' below implements a 2-input AND gate. The 'bad' process below implements a 2-input AND gate plus some extra logic. What is this extra logic?

```
Bad: Process                          Good: Process
Begin                                 Begin
If (A = '1' and B = '1') then            Y <= 0;
    Y <= '1';                            if (A = '1' and B = '1') then
End if;                                      Y <= '1';
End process                           end if;
                                       End process;
```

Bonus: ANSWER EITHER Question 21 OR Question 22.

21. Draw a block diagram for a saturating adder for 8-bit 2's complement numbers.
22. Give me a VHDL model that will implement the logic below. YOU DO NOT have to write the entity declaration.
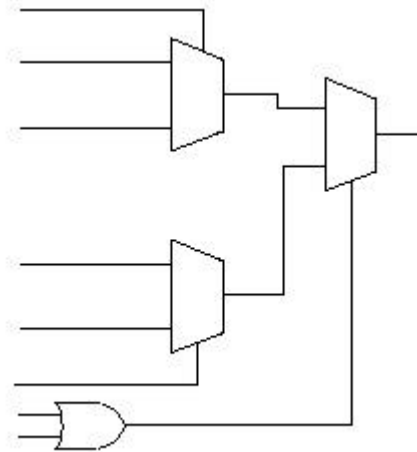
Can show work on next page.

Work for either problem 21 or 22.