EE 4743 Test #2 - Spring 1999 – Reese

SSN: _____ (no names please)

Answer questions 1-4. Answer 8 questions from questions 5-14 (cross out the questions that you do NOT want me to grade).

1. Figure 1 shows a 32-bit ripple carry adder. Show how you would modify this design to double its speed via pipelining.

2. On the FSM diagram for the vending machine, assume the state encoding is one-hot encoded (ZERO = "0001", FIVE = "0010", TEN="0100", FIFTEEN="1000").
   a. Write BY INSPECTION the boolean equation for State TEN.
   b. Write by inspection the equation for output "paper".

3. For the ASM chart shown in Figure 2, write the VHDL architecture block that will implement this ASM.

   ARCHITECTURE a OF detector is

4. For the logic diagram shown in Figure 3, give the delays of the following paths
   a. Longest Clock to Out

   b. Longest Register to Register Delay

   c. Longest Pin to Pin delay (combinational delay path).

Answer 8 of the following 10 questions

5. If I have a two chip design (two FPGAs), what timing characteristics of each chip would I need to know in order to compute the maximum operating frequency at which data can be transferred between the two chips?

6. How can I minimize the required external setup time of an input pin?

7. What is Latency in a digital system? Define it.

8. Give a 3-bit Grey code sequence (show all 8 states).

9. How do I ensure that an output from a FSM will be glitch free?

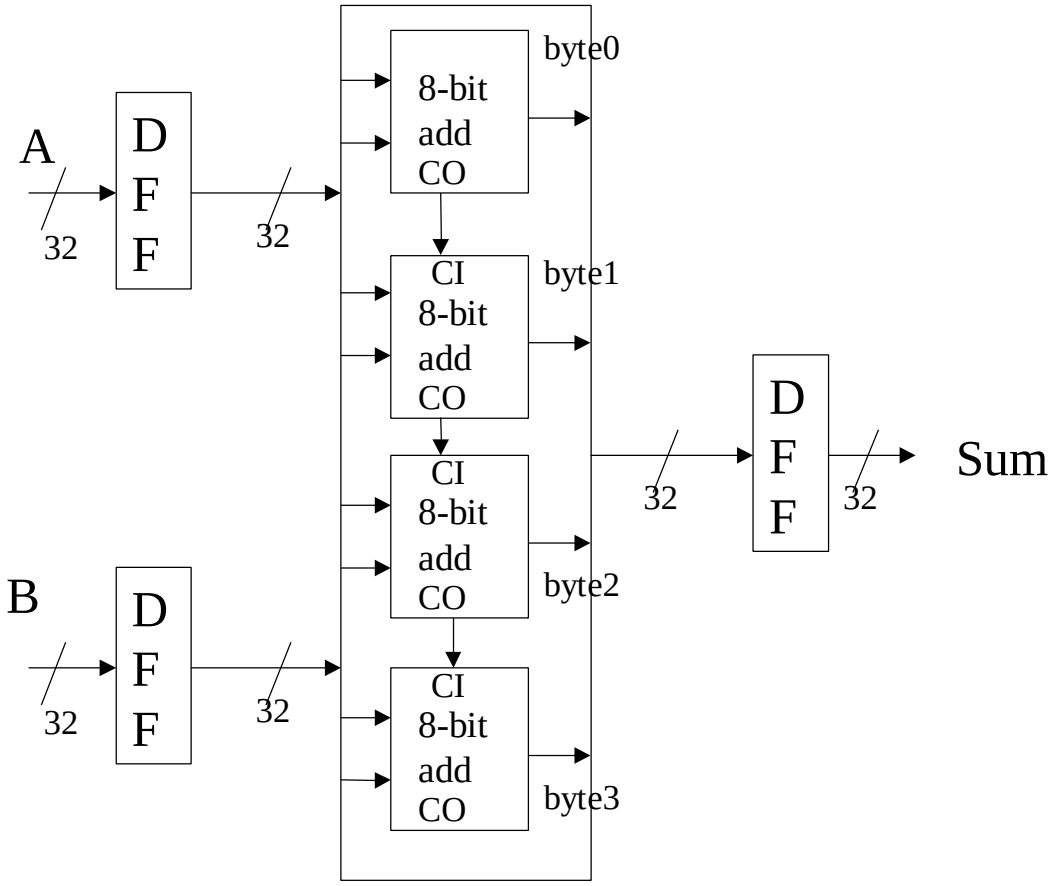
10. Write a VHDL process that will implement a J-K flip-flop.

11. What is the difference between a synchronous RAM and an asynchronous RAM? BE specific!

12. Joe Billy-Bob Schmo from Univ of Texas (or maybe Ole Miss, I forget), tied a conditional output from his FSM to the ACLR line of his LPM counter and he is getting erratic results during simulation. What could be the problem?

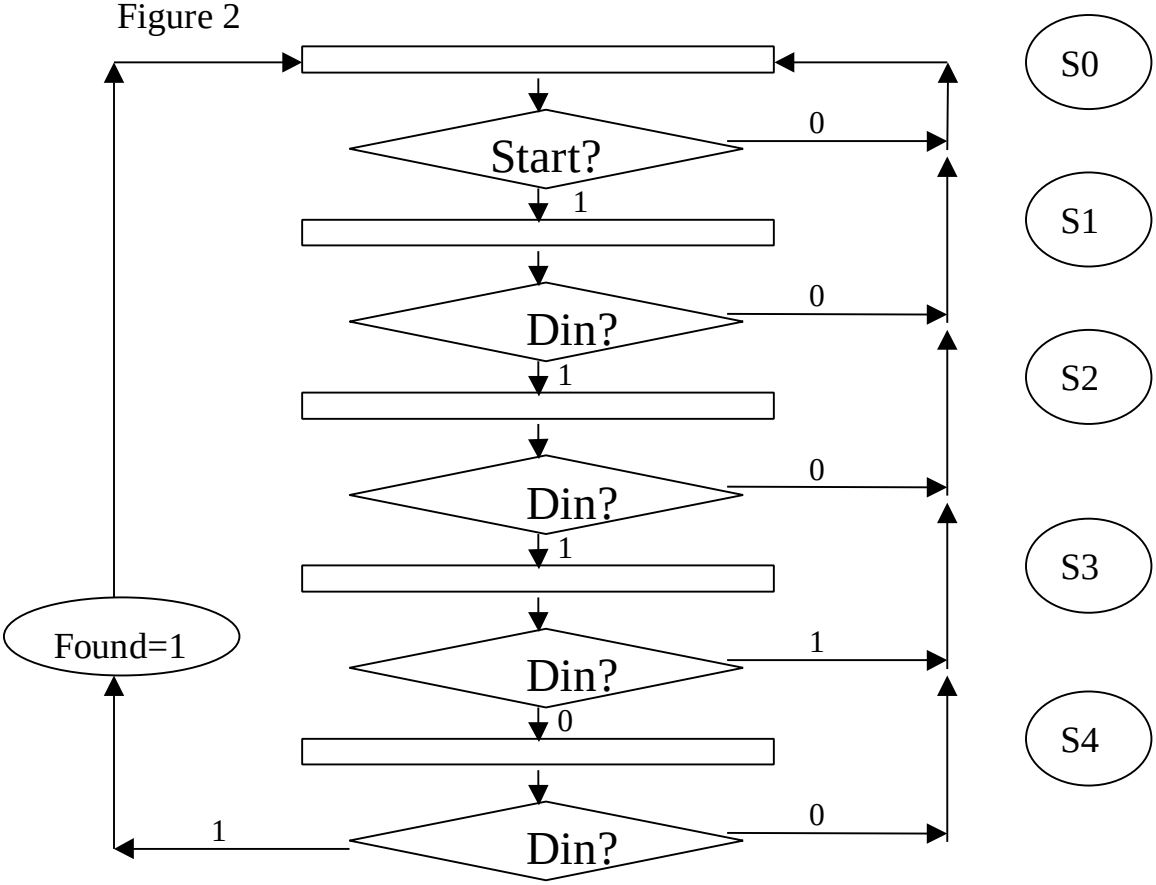
13. What is an FPGA timing model? What does it allow a designer to do?

14. What timing constraint am I checking if I compute the minimum path delay from an external input to the input of register?



32 Bit Ripple Carry Adder - Figure 1

Figure 2



Start, *Din* single bit inputs. Detects a serial bit sequence "1101".

Figure 3