Input Output Buffer Information Specification (IBIS)

- Problem: Want to model transmission line effects and other signal integrity issues on boards for different packages/buffer combinations
- Need models for packages/buffer structures
  - Want models to keep underlying implementation details hidden because of proprietary nature of I/O drivers
  - Need models to be usable by a variety of simulators and freely interchangeable
- Need simulator that understands IBIS models or else a translation mechanism that converts an IBSI model to my simulator model format.

IBIS Standard

- V1.0 – 1993, V3.2 – Sept. 1999, V4.0 July 2002
- Table driven format using V/I curves for buffers, key specs like R/L/C of package pins
- Offers Fast, Accurate Signal Integrity simulation
- Standalone signal integrity products from Cadence, Mentor Graphics (HyperLynx) can read IBIS models directly
- HSPICE (Synopsys) can read IBIS models directly

Model Types

- Input, Output, I/O, 3-state, Open_drain, I/O_open_drain,
- Open_sink, I/O_open_sink, Open_source, I/O_open_source,
- Input_ECL, Output_ECL, I/O_ECL, 3-state_ECL, Terminator,
- Series, and Series_switch.

Behavioral Diagram of IBIS Model

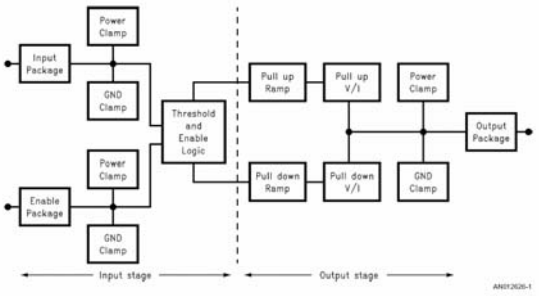


FIGURE 1. Behavioral Diagram of IBIS

From National Semiconductor App note 1111, Syed Huq Je '98

Input/Enable Structure

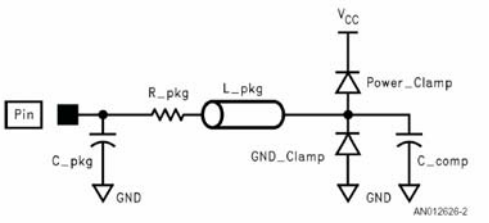


FIGURE 2. Input/Enable Structure Model

Output Structure

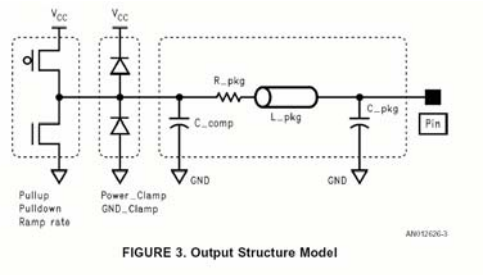
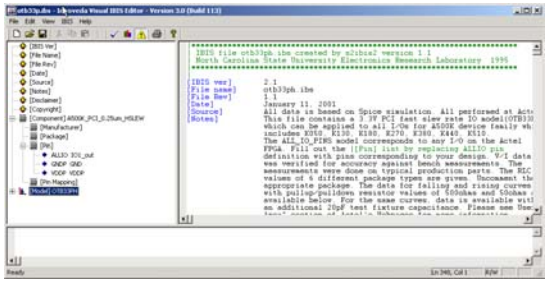


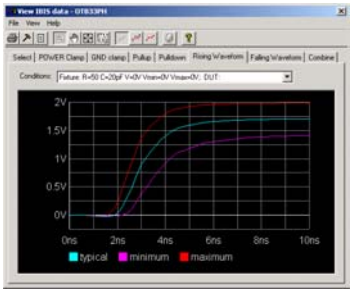
FIGURE 3. Output Structure Model

Visual IBIS Editor

Allows viewing/editing of IBIS Models – free download from Mentor. Can also view waveform data present in model.



IBIS Waveform Viewing (Rising)

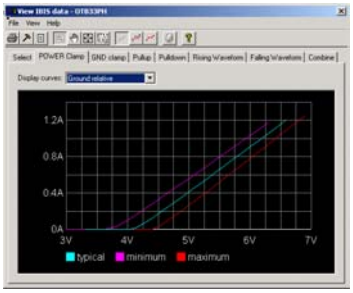


Rising Waveform

Model is for I/O buffer for ProASIC FPGA family from Actel Corporation.

Note conditions are typical output loads defined in data book R=50, C=20pF

Power Clamping



Shows current draw for power clamping on overshoot.

Other IBIS Sites

- Look at IBIS links on the class WWW page, they point to more information.