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Routing Results For:

Silicore SLC1657 Evaluation Board for Xilinx Spartan 2 FPGA

May 24, 2001

Test conditions:

Project:	CALCDEMO
Device:	Xilinx: XC2S50-5-PQ208
Synthesis tool:	Altium Accolade PeakFPGA 5.30a
Router:	Xilinx Alliance series 3.3.06I_V2_SE2

For more information, please refer to the SLC1657 Technical Reference Manual.

Timing Results (as reported by router):

Timing constraint (MIN):	5.000 MHz (MIPS)
Actual speed (MAX):	20.986 MHz (MIPS)

Device Utilization Results (as reported by router):

Device utilization summary:

Number of External GCLKIOBs	1 out of	4	25%
Number of External IOBs	34 out of	140	24%
Number of BLOCKRAMs	6 out of	8	75%
Number of SLICEs	370 out of	768	48%

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