

HD-6402

CMOS Universal Asynchronous Receiver Transmitter (UART)

March 1997

Features

- 8.0MHz Operating Frequency (HD-6402B)
- 2.0MHz Operating Frequency (HD-6402R)
- Low Power CMOS Design
- Programmable Word Length, Stop Bits and Parity
- · Automatic Data Formatting and Status Generation
- **Compatible with Industry Standard UARTs**
- Single +5V Power Supply
- CMOS/TTL Compatible Inputs

Description

The HD-6402 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Intersil advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Ordering Information

PACKAGE	TEMPERATURE RANGE	2MHz = 125K BAUD	8MHz = 500K BAUD	PKG. NO.
Plastic DIP	-40 ⁰ C to +85 ⁰ C	HD3-6402R-9	HD3-6402B-9	E40.6
CERDIP	-40 ⁰ C to +85 ⁰ C	HD1-6402R-9	HD1-6402B-9	F40.6
SMD#	-55 ^o C to +125 ^o C	5962-9052501MQA	5962-9052502MQA	F40.6

Pinout



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. http://www.intersil.com or 407-727-9207 | Copyright © Intersil Corporation 1999



Control Definition

CONTROL WORD				CHARACTER FORMAT					
CLS 2	CLS 1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS	
0	0	0	0	0	1	5	ODD	1	
0	0	0	0	1	1	5	ODD	1.5	
0	0	0	1	0	1	5	EVEN	1	
0	0	0	1	1	1	5	EVEN	1.5	
0	0	1	Х	0	1	5	NONE	1	
0	0	1	Х	1	1	5	NONE	1.5	
0	1	0	0	0	1	6	ODD	1	
0	1	0	0	1	1	6	ODD	2	
0	1	0	1	0	1	6	EVEN	1	
0	1	0	1	1	1	6	EVEN	2	
0	1	1	Х	0	1	6	NONE	1	
0	1	1	х	1	1	6	NONE	2	
1	0	0	0	0	1	7	ODD	1	
1	0	0	0	1	1	7	ODD	2	
1	0	0	1	0	1	7	EVEN	1	
1	0	0	1	1	1	7	EVEN	2	
1	0	1	Х	0	1	7	NONE	1	
1	0	1	х	1	1	7	NONE	2	
1	1	0	0	0	1	8	ODD	1	
1	1	0	0	1	1	8	ODD	2	
1	1	0	1	0	1	8	EVEN	1	
1	1	0	1	1	1	8	EVEN	2	
1	1	1	Х	0	1	8	NONE	1	
1	1	1	Х	1	1	8	NONE	2	

Pin Description

1 V _{CC} + Positive Voltage Supply 22 0 TBRE A high level on TRANSMITTER 2 0 TBRE A high level on RECEIVER REGISTER DISABLE to right register bidding out-puts RBR1-RBR8 to high inpedance state. 23 1 TBRE A high level on TRANSMITTER TER LOWD random state state of the RECEIVER REGISTER DISABLE to right register. 23 1 TBRE A high level on TRANSMITTER TER LOWD random state state of the RECEIVER REGISTER DISABLE to resist the ready for new data. 5 0 RBR8 The contents of the RECEIVER REGISTER DISABLE to RER State state a character state of the receiver data state state and is ready for new data. 23 1 TBRE A high level on TRANSMITTER TER LOWD random state state and is ready for new data. 5 0 RBR8 TBRE on the RECEIVER REGISTER DISABLE to RER State state and state state and is ready for new data. 23 1 TTBRE inhot the transmitter buff high transmitter buff register. 24 0 TTRE A high level on TRANSMITTER REGISTER Na high level on TRANSMITTER REGISTER Na high level on FRANSMITTER REGISTER Na high level on TRANSMITTER REGISTER Na high level on FARMSMIS REGISTER	ON
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3 GND Ground and is ready for new data. 4 1 RDD A high level on RECIVER REGISTER DISABLE forces the receiver holding out-puts RR1-RBR8 in bigh impedance state. 23 1 TBR A low level on TRANSMITTER TER LOAD transmitter buff high transition on TBRL initiate the transmitter register. 5 0 RBR8 The contents of the RECIVER BUFFER REGIS- TER appear on these three-state outputs. Word for- mats less than 8 characters are right justified to RBR1. TBR A low level on TRANSMITTER Triansmitter register. 6 0 RBR7 See Pin 5-RBR8 25 0 TRC Character data site added into till approved correspond grammed word length. 10 0 RBR3 See Pin 5-RBR8 25 0 TRC Character data site added into till BUFFER REGISTER via input register. 11 0 RBR2 See Pin 5-RBR8 26 1 TBR1 Character data site added into till BUFFER REGISTER via input register. 12 0 RBR1 See Pin 5-RBR8 26 1 TBR1 See Pin 26-TBR1. 13 0 PE A high level on PARITY ERROR indicates received fig was not cleared before the last the ratare was transferred t	•
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 17 I RRC The Receiver register clock is 16X the receiver data rate. 18 I DRR A low level on DATA RECEIVED RESET clears the data received output DR to a low level. 19 O DR A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register. 20 I RRI Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register. 21 I MR A high level on MASTER RESET clears PE, FE, OE and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up. The HD-6402 must be master reset after power up. The reset pulse should meet V_{IH} and t_{MR}. Wait 18 clock cycles after the falling edge. MR does not clear the falling edge. After the falli	he control word. The
 18 I DRR A low level on DATA RECEIVED RESET clears the data received output DR to a low level. 19 O DR A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register. 20 I RRI Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register. 21 I MR A high level on MASTER RESET clears PE, FE, OE and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up. The HD-6402 must be master reset after power up. The reset pulse should meet V_{IH} and t_{MR}. Wait 18 clock cycles after the falling edge. MR does not clear the falling edge. After the falling ed	
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reset after power up. The reset pulse should meet V _{IH} and t _{MR} . Wait 18 clock cycles after the falling	
I I I I I I I I I I I I I I I I I I I	ER CLOCK is 16X
edge of MR before beginning operation. † A 0.1μF decoupling capacitor from the V _{CC} pin	to the GND is rec-
ommended.	



Transmitter Operation

The transmitter section accepts parallel data, formats the data and transmits the data in serial form on the Transmitter Register Output (TRO) terminal (See serial data format). Data is loaded from the inputs TBR1-TBR8 into the Transmitter Buffer Register by applying a logic low on the Transmitter Buffer Register Load (TBRL) input (A). Valid data must be present at least t_{set} prior to and t_{hold} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are transmitted. The character is right justified, so the least significant bit corresponds to TBR1 (B).

The rising edge of TBRL clears Transmitter Buffer Register Empty (TBRE). 0 to 1 Clock cycles later, data is transferred to the transmitter register, the Transmitter Register Empty (TRE) pin goes to a low state, TBRE is set high and serial data information is transmitted. The output data is clocked by Transmitter Register Clock (TRC) at a clock rate 16 times the data rate. A second low level pulse on TBRL loads data into the Transmitter Buffer Register (C). Data transfer to the transmitter register is delayed until transmission of the current data is complete (D). Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



FIGURE 1. TRANSMITTER TIMING (NOT TO SCALE)

Receiver Operation

Data is received in serial form at the Receiver Register Input (RRI). When no data is being received, RRI must remain high. The data is clocked through the Receiver Register Clock (RRC). The clock rate is 16 times the data rate. A low level on Data Received Reset (DRR) clears the Data Receiver (DR) line (A). During the first stop bit data is transferred from the Receiver Register to the Receiver Buffer Register (RBR) (B). If the word is less than 8 bits, the unused most significant bits will be a logic low. The output

character is right justified to the least significant bit RBR1. A logic high on Overrun Error (OE) indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. One clock cycle later DR is reset to a logic high, and Framing Error (FE) is evaluated (C). A logic high on FE indicates an invalid stop bit was received, a framing error. A logic high on Parity Error (PE) indicates a parity error.





HD-6402

Absolute Maximum Ratings	Thermal Information		
Supply Voltage +8.0V Input, Output or I/O Voltage Applied. GND -0.5V to V _{CC} +0.5V Storage Temperature Range -65°C to +150°C Junction Temperature +175°C Lead Temperature (Soldering 10s) +300°C ESD Classification Class 1 Typical Derating Factor 1mA/MHz Increase in ICCOP	Thermal Resistance (Typical) CERDIP Package PDIP Package Gate Count	50 ^o C/W	θ _{JC} 12 ^o C/W N/A 1643 Gates
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may can of the device at these or any other conditions above those indicated in the opera		ress only ratin	g and operation

Operating Conditions

DC Electrical Specifications V_{CC} = $5.0V \pm 10\%$, T_A = -40° C to $+85^{\circ}$ C (HD-6402R-9, HD-6402B-9)

		LIMITS					
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS		
V _{IH}	Logical "1" Input Voltage	2.0	-	V	V _{CC} = 5.5V		
V _{IL}	Logical "0" Input Voltage	-	0.8	V	$V_{CC} = 4.5V$		
II	Input Leakage Current	-1.0	1.0	μΑ	$V_{IN} = GND \text{ or } V_{CC}, V_{CC} = 5.5V$		
V _{OH}	Logical "1" Output Voltage	3.0 V _{CC} -0.4	-	V	I _{OH} = -2.5mA, V _{CC} = 4.5V I _{OH} = -100μA		
V _{OL}	Logical "0" Output Voltage	-	0.4	V	I_{OL} = +2.5mA, V_{CC} = 4.5V		
Ι _Ο	Output Leakage Current	-1.0	1.0	μΑ	$V_{O} = GND \text{ or } V_{CC}, V_{CC} = 5.5V$		
ICCSB	Standby Supply Current	-	100	μΑ	$V_{IN} = GND \text{ or } V_{CC}; V_{CC} = 5.5V,$ Output Open		
ICCOP	Operating Supply Current (See Note)	-	2.0	mA	V_{CC} = 5.5V, Clock Freq. = 2MHz, V_{IN} = V_{CC} or GND, Outputs Open		

NOTE: Guaranteed, but not 100% tested

Capacitance T_A = +25^oC

			LIMIT	
PARAMETER	SYMBOL	CONDITIONS	TYPICAL	UNITS
Input Capacitance	CIN	Freq. = 1MHz, all measurements are referenced to de- vice GND	25	pF
Output Capacitance	COUT		25	pF

AC Electrical Specifications $~V_{CC}$ = 5.0V \pm 10%, T_{A} = -40 ^{o}C to +85 ^{o}C (HD-6402R-9, HD6402B-9)

		LIMITS HD-6402R		LIMITS HD-6402B				
SYMBOL	PARAMETER	MIN	МАХ	MIN	MAX	UNITS	CONDITIONS	
(1) fCLOCK	Clock Frequency	D.C.	2.0	D.C.	8.0	MHz	$C_L = 50 pF$	
(2) t _{PW}	Pulse Widths, CRL, DRR, TBRL	150	-	75	-	ns	See Switching Waveform	
(3) t _{MR}	Pulse Width MR	150	-	150	-	ns		
(4) t _{SET}	Input Data Setup Time	50	-	20	-	ns		
(5) t _{HOLD}	Input Data Hold Time	60	-	20	-	ns		
(6) t _{EN}	Output Enable Time	-	160	-	35	ns		



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