ELEC372
Computer Aided Logic Design and Computer Architecture
1997

Course Components

First Semester (Digital Logic Design, Lecturer: Bob Betz)

- Introduction to computer aided logic design (CALD).
- Details of the internal workings of modern EPLD devices and how this impacts on design.
- How to use the Altera logic design suite.
- Introduction to hardware description languages (HDLs).
- Details of the Altera Hardware Description Language (AHDL).
- Introduction to the Very High Speed Integrated Circuit Hardware Description Language (VHDL).
- Project involving the design of a standard UART (16450).

Second Semester (Computer Architecture, Lecturer: Hossam Elgindy)

- See Hossam.

First Semester Lecturer

Bob Betz, Room EAG29 (NB. there are two rooms marked as EAG29 - they are next to each other. I am in the room at the extreme eastern end of the building).

Lectures/Tutorials (1st Semester)

Friday, 2-4pm, room ES206. Tutorials, Friday 4-5pm, room ES206.

References

- M. Morris Mano, *Digital Design, 2nd Edition*, Prentice Hall, Englewood Cliffs, New Jersey, ISBN 0-13-212994-9, 1991
- John F. Wakerly, *Digital Design, Principles and Practices, 2nd Edition*, Prentice Hall, Englewood Cliffs, New Jersey, ISBN 0-13-059973-5, 1994.
- John P. Hayes, *Introduction to Digital Logic Design,* Addison-Wesley, ISBN 0-201-15461-7, 1993.
- *Max+Plus II Programmable Logic Development System, Getting Started*, Altera Corporation, November, 1995.
- *Max+Plus II Programmable Logic Development System, Text Editor & AHDL*, Altera Corporation, April, 1991.
- There are numerous books in the library on VHDL.
- The on-line help system in the Altera software system is very extensive and well worth consulting.

Course Assessment (First Semester)

See the generic handout for the general rules about all EE&CE subjects. There will one quiz in both the first and second semester. It should be emphasized that the ***minimum mark in the quizes to pass the subject is 40%***. If you fail to meet the 40% requirement for the 1st semester quiz then you should withdraw from the 2nd semester of the course. Failure to do so will incur HECS charges for the 2nd semester. Furthermore you will have a failure recorded against your name.

First semester contribution to final mark: Quiz 20%; Assignment 30%.

Course Objectives (1st Semester)

It is the objective of this course to leave students with the following competencies:

- To be able to carry out a significant digital logic design with modern CAD tool using the digital logic design theory established in previous courses.
- To understand the limitations on the speed performance of EPLDs caused by their internal architecture.
- Having working knowledge of Hardware Description Languages (HDLs), especially AHDL and VHDL.

In order the achieve these course objectives a “hands-on” approach is taken.

A Note About the First Semester Assignment

From the above course assessment one will notice that there is a high emphasis on the assignment in first semester. The assignment will consist of a major design project which will be undertaken in groups of two. The design will be assessed by a demonstration of the design. In addition a report on the design will be handed in.

The design can be broken up into blocks so that one can proceed through a set of steps, each step producing a new working version of the design. The more steps completed the more elaborate the design will be (and the higher the mark that will be attained). Using this process every group should be able to produce a working design of some description.

In order to prepare for the assignment students should do the tutorials in the Altera “Getting Started” book. This is available from my Web Site at URL *http://www.ee.newcastle.edu.au/users/staff/reb/Betz.html* (this can also be located via the main University page). Copies of the slides presented in the lectures are also available at the same site. One can also obtain a lot of information about Altera components via anonymous ftp to *murray.newcastle.edu.au*, and go to the directory */pub/reb/Elec372_material/Altera_data*.