LABORATORY MANUAL

FOR

DIGITAL SYSTEM DESIGN I

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REVISION HISTORY

- Experiment 4 updated. August 2009. T. Obuchowicz
- "The Report" section update. July 2010. T. Obuchowicz

EMERGENCY PROCEDURES

1. **Emergency Evacuation during a Fire Alarm**
   - Stop your work and secure your area
   - **Proceed to the nearest Fire Exit**
     Don't Use Elevators or Escalators – Chimney effect
   - **General Alarm** – Bells ring continuously
     Message will be given through the Public Address System, if available
   - **Follow the directives** from the Fire Monitors (wearing armbands)
   - **Once outside move away from the building** to the gathering location

You must evacuate

2. **Emergency Procedures in the Event of Fire Discovery**
   - **Sound the alarm** by activating the nearest Pull Station
   - **Call Security** to confirm using:
     - **Fire or Emergency telephones** located near exit stairwells no dialing necessary, or
     - **Public phones** by dialing 848-3717 (no charge), or
     - **Office phones** by dialing 811, or
     - **Cellular phones** by dialing 848-3717
   - ***Give your Name, Location, and Nature of the problem***
   - Once informed of the situation **Security will call 911**

You must evacuate

3. **What to do in case of Medical Emergency**

Serious/Life-Threatening Emergency
   - **Call 9-911 to alert Urgences Santé**
     Give your Name, Location and Nature of the problem
   - **You must call Security** using (see above instructions)
   - Give your Name, Location, and Nature of the problem and tell them that you have called the 911
   - **Provide first-aid assistance if you can** or call 4181 to request an Emergency Responder
   - **Security will send an agent to assist you**
     Agents have been trained to provide first-aid assistance

You must always contact Security

Non Life-threatening Situation (not requiring Urgences Santé)
   - **Call Security** (see above instructions)
   - **Provide first-aid assistance if you can** or call 4181 to request an Emergency Responder

October 14th, 2004

CONTENTS

THE REPORT

For each experiment performed a report must be submitted. This report should present the relative theory used to accomplish the experiment including a discussion of the analysis and design of all circuits. The results obtained from the experiment should be presented in a clear and concise manner. The experimental results should be discussed and compared to the theoretical results.

The format for the report is as follows:

OBJECTIVES
INTRODUCTION
RESULTS
DISCUSSION
CONCLUSION
PRE-LAB

OBJECTIVES - Describe **IN YOUR OWN WORDS** the goals of the experiment.

INTRODUCTION - Present any relevant theory used in the experiment using words, diagrams, tables, charts, schematics, etc.

RESULTS - Describe the procedure that was performed to obtain the results. Present the results in a clear and concise manner. Use tables, graphs, diagrams, etc. to aid in the presentation.

DISCUSSION - Discuss the results obtained. If the results are poor (i.e. the circuit did not function as expected) give possible reasons to explain the incorrect results. NOTE: A portion of the lab grade is allotted to correct circuit operation - you should strive to design and build a properly working circuit.

CONCLUSION - Explain what was learned from the experiment and summarize the salient theoretical aspects of the lab.

PRE-LAB - This is to be included as an appendix to the lab report. Any relevant material from the pre-lab used in the Introduction or Discussion sections should be reproduced in the section (i.e. do not simply include the pre-lab in the Introduction or Discussion sections).

Some tips about writing good reports:

- Label diagrams and tables with numbers and captions.
- Reference figures and tables by number in the text. If a figure or table is not referred to in body of the text then it should not be included in the report.
- Do not draw figures with pencil. Everything hand written should be in ink.
- Use your own words to describe everything. You may use referenced material when appropriate... **BUT IT MUST BE REFERENCED!!!!!**
- All text must be type written, preferably using a word-processing package such as MS Word™ or FrameMaker™.
- Proof-read the report for spelling and grammar mistakes. (Do not rely on "spell check" and "grammar check" software... it is good, but it does make mistakes!)
- Use a font size of 10-point or greater.
- Do not refer to figures or tables from the lab manual. Rather, they should be redrawn in the report.

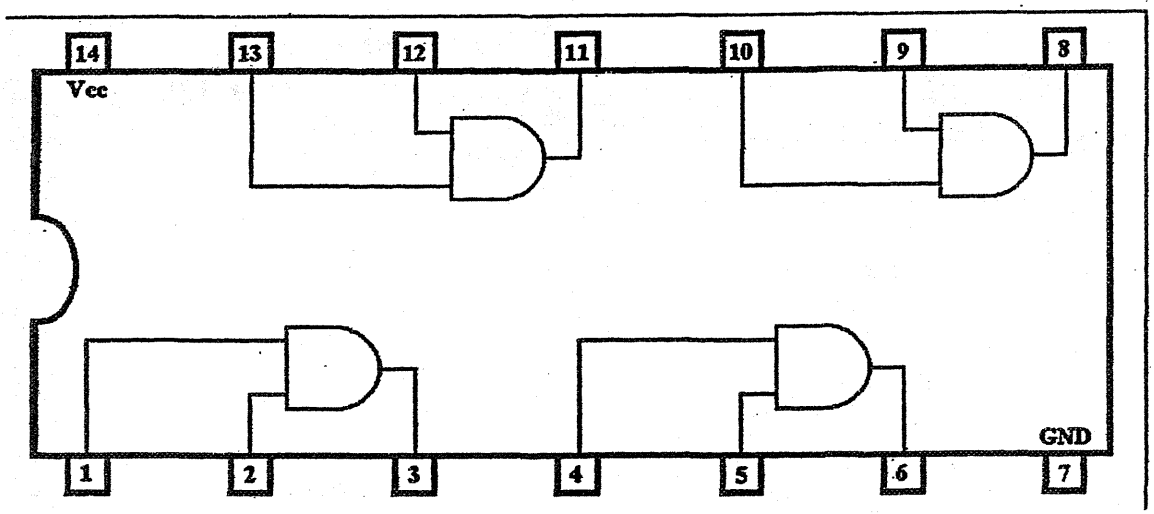
Remember, a report is a means to document what you have done in an experiment. It should comprehensive enough such that anyone reading the report could reproduce your experiment to achieve the same results!

HOW TO DRAW A LOGIC CIRCUIT DIAGRAM

A logic circuit diagram is a block level diagram consisting of the inputs and outputs, the logic gates (e.g. AND, NOR, inverters, etc.), black box circuits, and the interconnectivity between all of them. Every logic gate in the diagram should contain a part number, an instance name, and the physical pin numbers that the wires would connect to the integrated circuit of that instance.

A part number is code that uniquely identifies the type of IC that is used. As each gate is shown using its logic diagram, it should be written on the gate what type of IC is implementing it. For example, a two input AND gate could be implemented using a 74x08 IC.

An instance number is any logic gate label that indicates from which IC the gate is being used. In other words, it is an identifier of the IC itself. It should be noted that many ICs have several gates inside. For example, the 74x08 Quad 2-Input AND gate IC has four 2-input and gates inside it. The figure below shows the arrangement of the AND gates inside the IC and which pins are used.



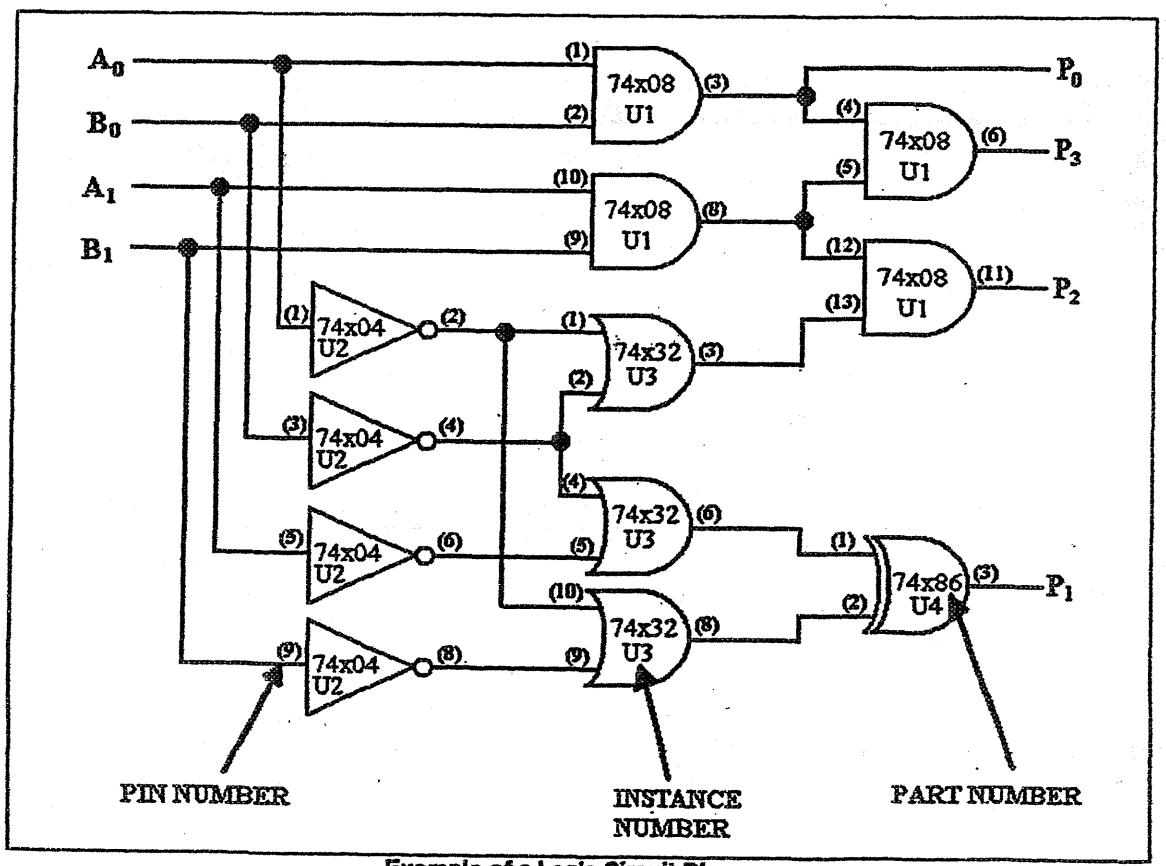
74x08 Quad 2-Input AND Integrated Circuit Pinout

Pin numbers are the labels that indicate from which pin of a particular IC is being connected through a wire. (I.e. pin numbers are the numbers shown in the figure above from the actual IC pins.)

Some helpful tips to drawing good circuit diagrams are as follows:

- Wires should always be drawn vertically and horizontally, not diagonally. (Note that it is sometimes acceptable to draw diagonal lines when representing latches.)
- A dot should be put any place where two wires intersect and belong to the same node.
- Whenever possible, draw the inputs entering the circuit from the left side, and the outputs leaving from the right side.
- Label long wires at all its end-points throughout a diagram to help readability.
- Label internal wire nodes to help readability.
- Do not route ground and V_{DD} wires throughout a circuit diagram unless they connect to a gate input.

The figure below is an example of what a logic circuit diagram should look like. Note that the AND gates are labeled with their part number (74x08), an instance number (U1) and the IC pin numbers inside brackets. The OR gates are labeled with their part number (74x32), an instance number (U3), and the associated IC pin numbers. The outputs are P_0, P_1, P_2, and P_3. The inputs are labeled A_0, A_1, B_0, and B_1.



Example of a Logic Circuit Diagram

EXPERIMENT 1

INTRODUCTION TO THE PROTO-BOARD®, LOGIC GATES, AND DEBUGGING TECHNIQUES

OBJECTIVES

- To introduce the Proto-Board® facilities.
- To gain experience using breadboards and wiring digital circuits.
- To learn techniques for debugging circuits.

INTRODUCTION

The Breadboard:

A breadboard is a device used to interconnect electronic circuits. As shown in Figure 1.1, the breadboard consists of many holes in which circuit components (i.e. ICs, resistors, capacitors, etc.) are inserted. A breadboard is connected internally via strips of metal. This facilitates the connection between components and permits the use of data and power buses. Figure 1.1 illustrates the internal connectivity of the holes.

Dual Inline Package (DIP) Integrated circuit (IC) components are inserted into the breadboard holes as shown in Figure 1.1. Note that the vertical connections do not cross the horizontal gap in the center of the breadboard.

Power and ground buses are usually constructed using the horizontally connected holes on the top and bottom of the breadboard.

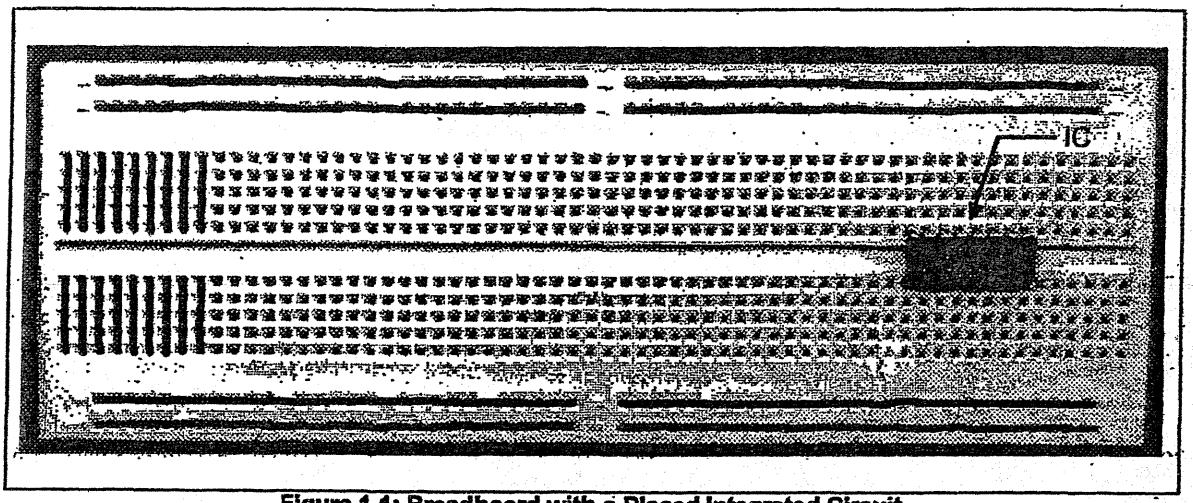


Figure 1.1: Breadboard with a Placed Integrated Circuit

The Proto-Board®:

The Proto-Board® is a complete mixed-signal test-bench from Global Specialties equipped with regulated and variable power supplies, breadboards, switches, light emitting diodes (LEDs), pushbuttons, signal generators, potentiometers (POTs), pin-to-BNC connectors, and an 8Ω speaker.

The "ON" Button:

The Proto-Board® may be turned on using the big red switch at the top, left corner of the kit (next to the power cord). When the kit is turned on, the button should illuminate.

Power Supply:

The regulated power supply is located at the top, right side of the kit. There are four connectors with the colors of red, yellow, blue and black. The red connector is a 5V supply and the black connector is the ground (i.e. 0V).

Logic Indicators:

Under the power supply are the logic indictors. These are a set of LEDs. When +5V is placed on a pin, the corresponding red LED will be illuminated. Conversely, when 0V is placed on a pin, the green LED will light up. These LEDs will be used as the output display for the majority of the experiments.

Note the two selector switches associated with the logic indicators. The top switch should be set to "+5V" and the lower switch should be set to "TTL".

Logic Switches:

On the bottom, left side of the kit are the logic switches. These will emulate digital inputs. When the switch is down the output is 0V or logic low. When the switch is up the output is logic high.

Note the selector switch associated with logic switches. It should be set to "+5V".

Frequency Generator:

Under the "ON" switch is a frequency and signal generator. This feature allows the generation of sinusoids, ramps, and square waveforms at frequencies in the range of 0.1Hz to 100kHz. For Experiments 4 and 5 the square waveform may be used as a clock for sequential circuits.

Pushbuttons:

Two pushbuttons are available for use with edge-triggered devices (e.g. 74LS74 Delay Flip-Flop). These are the two blue buttons located below the Frequency Generator.

NOTE: Do not use +V power supply with any of the circuitry in these experiment!!!

Logic Gates, Flip-Flops, Decoders, Multiplexers:

In general, any type of integrated circuit (IC) devices may be used. However, only transistor-transistor logic (a.k.a. TTL) will be used in these experiments. Table 1.1 lists the devices that will be used in this experiment. See Appendix A for the data sheets for each device. Note that each of these devices contains several gates inside. (I.e. don't use one IC for one gate!)

Table 1.1: TTL Gates

Device Number	Function
7400	Quad 2-input NAND gate
7402	Quad 2-input NOR gate
7404	Hex Inverter
7408	Quad 2-input AND gate
7410	Triple 3-input NAND gate
7432	Quad 2-input OR gate

Debugging Circuits:

Debugging a circuit implies determining where, if anything, something is not functioning. There are many common mistakes made that lead people to believe that their circuit is non-functional. Some of these common mistakes are:

- Forgetting to turn on the power switch! ☺
- Forgetting to connect to the ground and +5V supplies to <u>each</u> IC.
- Connecting the power and ground incorrectly.
- Improperly wiring a circuit.
- Connecting two outputs together.
- Using the wrong IC.
- Using an IC with broken pins such that no connection is made into the holes of a breadboard.
- Using an IC that is damaged internally. ICs may be damaged by applying an excessive voltage to any pin, by grounding output pins, connecting two outputs together, or by reversing the power and ground connections.

Due to these possible errors, you should follow these steps when debugging a circuit.

1. Check all connections carefully to ensure that the power and grounds are connected to each IC correctly and that no TTL gate outputs are connected together or grounded.
2. Check each IC to ensure that all the pins are not broken. Be very careful when placing and removing the IC from the breadboard. The pins are very delicate.
3. Turn the power supply on. Touch each IC with your finger. If the IC is hot, then it is possible that that IC is destroyed. Turn the power off immediately!!! Check the connection leading to that IC. If the connections are correct then test the "Burned" IC independently (i.e. take it out of the circuit and connect it by itself to determined if it is broken).
4. With the power supply turned on, check each internal circuit node to determine if the functionality is as expected. Always start from the node closest to the inputs. Use the LED arrays and a single wire to probe the nodes. Use a truth table to compare the expected results.

WARNINGS

1) **TTL gate outputs should not be connected to other TTL gate outputs.**

2) **TTL gate outputs must never be shorted to ground. Check your connections carefully!**

3) **Always connect unused TTL inputs to logic HIGH (+5V) or logic LOW (0V), whichever is appropriate. This reduces undesirable effects due to electrical noise.**

4) **Always connect the ground and +5V to the integrated circuits before wiring the circuit. Forgetting to connect the power supplies is one of the most common mistakes made.**

5) **Never apply more than +5V to any pin of a TTL gate.**

6) **When modifying a circuit ensure that the power is turned off!**

PRE-LAB

1) Read all of Experiment 1 (pages 5-13) to become familiar with the Proto-Board and Procedures for completing this experiment.

2) Analyze the logic circuits shown in figures 1.2, 1.3, and 1.4 to determine their Boolean logic function.

3) Analyze the circuit given in Figure 1.5. Provide your analysis in a truth table. Include in your truth table all the internal nodes (x, y, and z).

PROCEDURE

Part 1

Connect the circuits shown below on a breadboard. Note that the circuits (a) and (b) may be connected using the same IC. Test each circuit by connect the inputs (A, B, C, and D) to the switches on the Proto-Board®. Connect each output to one LED. Record your results in a Truth Table.

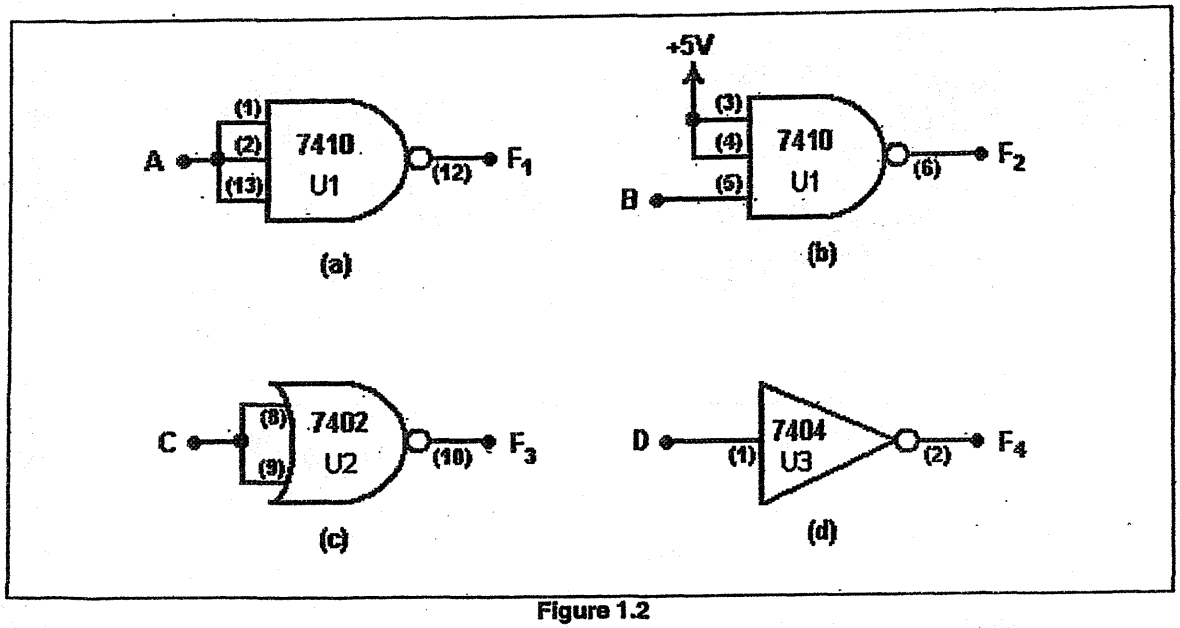


Figure 1.2

Demonstrate your circuits to the lab instructor before disconnecting them!

Part 2

Connect the circuit shown in Figure 1.3. Test all possible combinations to obtain a Truth Table.

Questions:

1) From your results, what Boolean function does this circuit produce?
2) Do your results agree with your analysis of this circuit? Why or why not?
3) Draw another circuit that would produce the same Boolean function using only NOR gates.

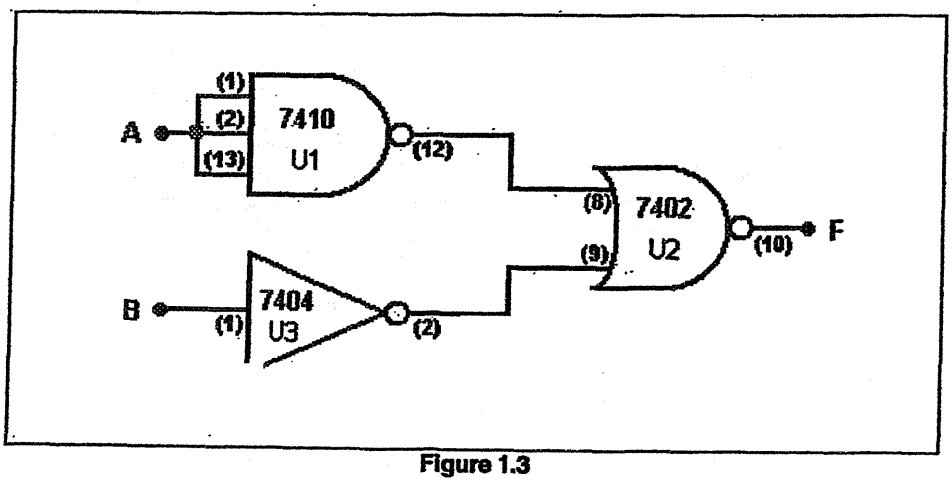


Figure 1.3

PART 3

Connect the circuit shown in Figure 1.4. Test all possible combinations to obtain a Truth Table. Note: You need only one IC to for this circuit!

Questions:

4) From your results, what Boolean function does this circuit produce?
5) Do your results agree with your analysis of this circuit? Why or why not?
6) What are the benefits of designing digital circuits using only NAND gates?

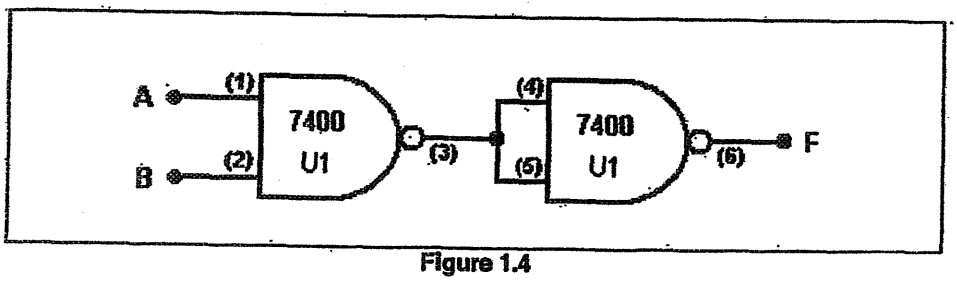


Figure 1.4

PART 4

Connect the circuit shown in Figure 1.5. Using an LED, probe each internal node (x, y, and z) and record your results in a truth table. If there are any problems with your circuit record what was wrong and how you were able to fix it.

If you determine that an IC is broken, then demonstrate it to the lab instructor.

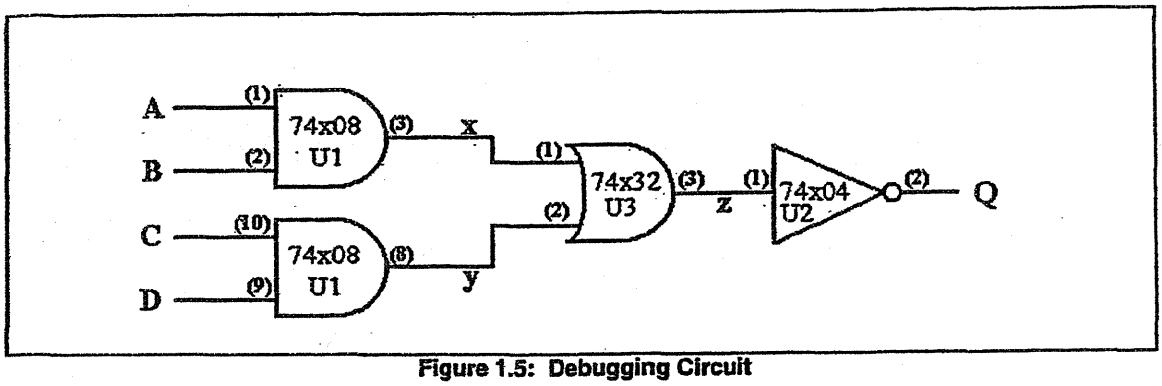


Figure 1.5: Debugging Circuit

Questions:

7) Reiterate in your own words the procedure for debugging circuits. List the most common problems with digital circuits. Are there any other possible problems that could arise?

EXPERIMENT 2

COMBINATIONAL LOGIC CIRCUIT DESIGN

OBJECTIVE

- To gain experience in connecting digital circuits on a breadboard.
- To construct and verify the operation of a 2-bit multiplier.
- To obtain an appreciation for modular design.

INTRODUCTION

2-Bit Multiplier

A 2-bit multiplier is a circuit that multiplies two 2-bit binary numbers (A and B) to produce a 4-bit binary output (P). The truth table describing the system behavior is given in Table 2.1.

Table 2.1: Truth Table for a 2-Bit Multiplier with Inputs A and B and Output P

INPUTS				OUTPUTS				
A_1	A_0	B_1	B_0	P_3	P_2	P_1	P_0	Decimal
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	1	1
0	1	1	0	0	0	1	0	2
0	1	1	1	0	0	1	1	3
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0	2
1	0	1	0	0	1	0	0	4
1	0	1	1	0	1	1	0	6
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	1	1	3
1	1	1	0	0	1	1	0	6
1	1	1	1	1	0	0	1	9

It may be seen, for example, that the product of 1x1 (A_1A_0=01 and B_1B_0=01) yields the result of 1 ($P_3P_2P_1P_0$=0001). Similarly, the product of 3x2 (A_1A_0=11 and B_1B_0=10) yields 6 ($P_3P_2P_1P_0$=0110).

Modular Design

Large and complex circuits should always be designed and tested modularly. This implies that a circuit should be broken down into blocks that may be built and tested on their own. For example, the circuit for each output bit of the 2-bit multiplier described above should be built and tested independently of the others. This will aid in circuit debugging and it will ensure that if one circuit is non-functional, the others will not be affected. This example is simple and may not warrant modular design, however, it is important to understand the concepts of modularity and it's place in any design.

By contrast, the circuit in Figure 2.1 is a condensed combinational logic design of the 2-bit multiplier. It incorporates sharing of common sum and product terms.

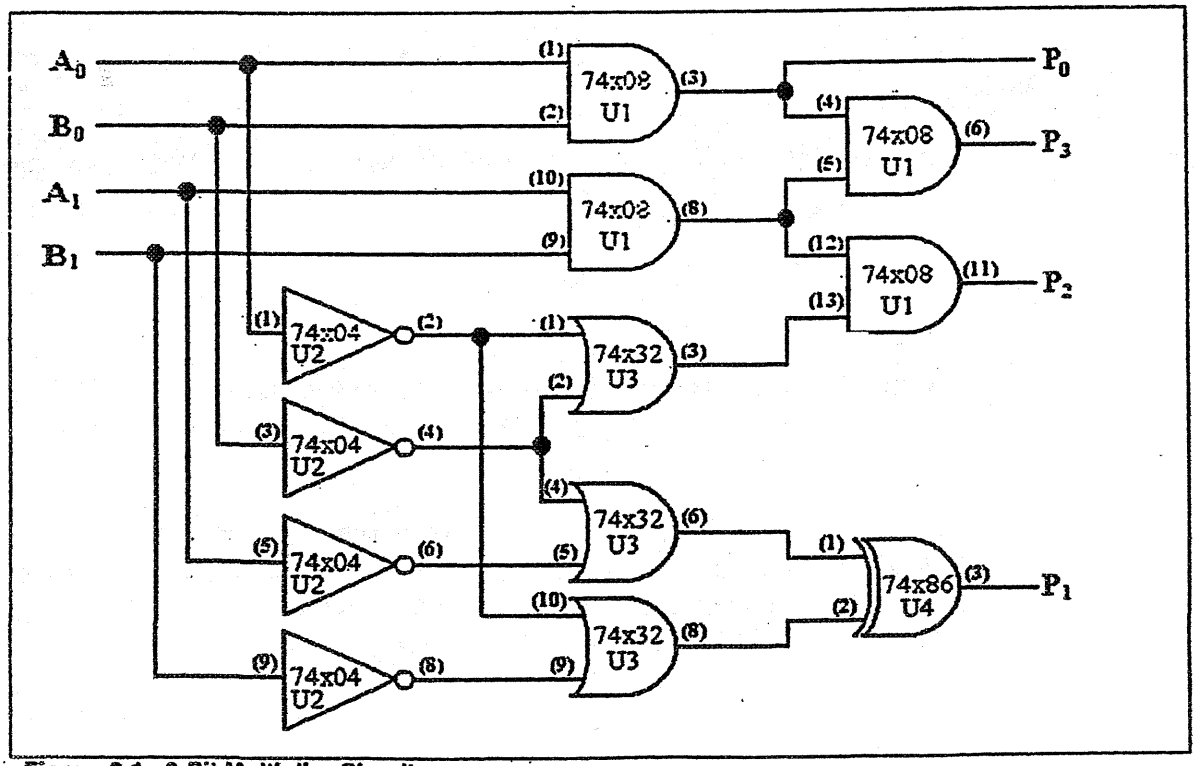


Figure 2.1: 2-Bit Multiplier Circuit

PRE-LAB

1) Read all of Experiment 2 (pages 14-16) to become familiar with the Procedures for completing this experiment.

2) Design the 2-bit multiplier using the truth table given in Table 2.1. Obtain the standard sum of products (SSOP) from the truth table. Minimize the logic using K-maps.

3) Draw the logic circuit diagram for the 2-bit multiplier. Do not forget to label each gate with its name, instance number, and pin numbers.

4) Analyze the circuit in Figure 2.1. Show that its truth table is the same as that given in Table 2.1.

PROCEDURE

1) Connect the 2-bit multiplier circuit that was designed in the Pre-Lab. Verify its functionality by testing all possible input values. Record your results in a truth table.

2) Connect the circuit in Figure 2.1. Verify its functionality by testing all possible input values. Record your results in a truth table.

Questions:

1) Describe in your own words the purpose of modular design. Why do we break down circuits into modules and design them independently?

2) The circuit in Figure 2.1 is a "condensed" design for a 2-bit multiplier. What are the advantages and disadvantages between the circuit that you have designed and the one in Figure 2.1? In your opinion, which design is better and why?

EXPERIMENT 3

DESIGN OF MSI COMPONENTS

OBJECTIVE

- To gain experience in connecting digital circuits on a breadboard.
- To design a 2-to-1 multiplexer.
- To design a combinational adder circuit.

INTRODUCTION

Multiplexer:

A multiplexer is a device that directs one of many inputs to a single output. The input is selected using "select" lines that are inputs to the device. Figure 2.1(a) illustrates the system diagram of an n-to-1 multiplexer where n is the number of inputs and m is the number of select lines. It is always the case that $n = 2^m$.

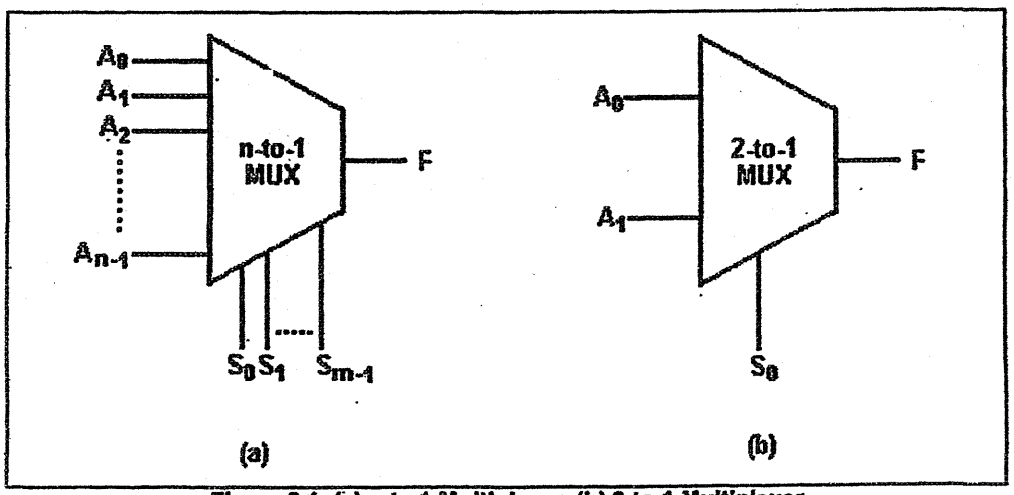


Figure 2.1: (a) n-to-1 Multiplexer (b) 2-to-1 Multiplexer

Figure 2.1(b) shows the block diagram of a 2-to-1 multiplexer. When the select line S_0 is low the output is A_0 (i.e. $F = A_0$). When the select line is high then the output is A_1 (i.e. $F = A_1$).

Binary Adder:

The binary addition of two 1-bit numbers may be performed by adding the two bits to produce a sum bit and a carry bit. A circuit to perform this addition is called a "half-adder".

The binary addition of three 1-bit numbers may be performed by adding the three bits to produce a sum bit and a carry bit. A circuit to perform this addition is called a "full-adder".

The binary addition of two multi-bit numbers may be performed by adding the bits and carry, beginning with the least significant. For example, two 4-bit numbers may be added as follows:

```
 1 1 1 0      ← carry
  0111
+ 1110
 10101
```

It should be noticed that the least significant bits are added together with no carry. This implies using a half-adder. All other bits are added with a carry, thus implying a full-adder.

PRE-LAB

1) Read all of Experiment 3 (pages 17-20) to become familiar with the Procedures for completing the Procedures for completing this experiment.

2) Design a 2-to-1 multiplexer using standard logic gates such as inverters, NANDs, NORs, ANDs, ORs, etc. Obtain the standard sum of products (SSOP) from the truth table. Minimize the logic using K-maps.

3) Draw the logic diagram for the 2-to-1 mux. Do not forget to label each gate with its name, instance number, and pin numbers.

4) Draw a **half**-adder circuit using standard logic gates such as inverters, NANDs, NORs, ANDs, ORs, XORs, etc. Obtain the standard sum of products (SSOP) from the truth table. Minimize the logic using K-maps.

5) Draw the logic circuit diagram for the half-adder. Do not forget to label each gate with its name, instance number, and pin numbers.

6) Design a **full**-adder circuit using standard logic gates such as inverters, NANDs, NORs, ANDs, ORs, XORs, etc. Obtain the standard sum of products (SSOP) from the truth table. Minimize the logic using K-maps.

7) Draw the logic circuit diagram for the full-adder. Do not forget to label each gate with its name, instance number, and pin numbers.

8) Using the half-adder and full-adder circuits previously designed, generate the logic circuit for a 2-bit adder (i.e. a circuit that can add two binary numbers, each having 2-bits).

PROCEDURE

Part 1

Connect the 2-to-1 multiplexer circuit that was designed in the Pre-Lab. Verify its functionality by testing all possible input values. Record your results in a truth table.

Part 2

1) Connect the half-adder circuit designed in the Pre-Lab. Verify its functionality by testing all possible input values. Record your results in a truth table.

2) Connect the full-adder circuit designed in the Pre-Lab. **DO NOT remove the half-adder circuit!** Verify its functionality by testing all possible input values. Record your results in a truth table.

3) Connect the 2-bit adder using the half-adder and full-adder. Verify its functionality by testing all possible input values. Record your results in a truth table.

EXPERIMENT 4

LATCHES AND FLIP-FLOPS

OBJECTIVE

- To gain experience in connecting digital circuits on a breadboard.
- To acquire design, test, and debugging skills in sequential circuit design.
- To obtain an understanding of the design and functionality of latches and flip-flops.

INTRODUCTION

In order to design sequential logic circuits it is necessary to use logic elements that can store digital information. These devices are commonly referred to as latches and flip-flops.

Some of the most common latches and flip-flops are:

- Set-Reset (SR) Latch
- Clocked SR Latch
- JK Flip-Flop
- Toggle (T) Flip-Flop
- Delay (D) Flip-Flop

A *flip-flop* is a sequential device that samples its inputs and changes its output only at times determined by a clock signal. A *latch* is sequential device that watches all of its inputs continuously and changes its outputs at any time, independent of a clocking signal. Note that many textbooks refer to "latches" and "flip-flops" synonymously.

The SR Latch is the basic building block for the other flip-flops listed above. The logic diagram for the NAND and NOR implementations of an SR Latch is shown in Figure 4.1.

The Clocked SR Latch is a basic SR latch with control logic that enables the latch to "hold" its previous output values regardless of the input signals. This device is sometimes referred to as an "SR Latch with Enable" or "SR Flip-Flop".

A JK Flip-Flop is a device that incorporates the functionality of an SR flip-flop but accounts for the "forbidden" input combination of the SR latch. This device has three inputs and two complementary outputs. Its inputs are J, K, and CP. CP is a clock pulse that synchronizes the state change. Inputs J and K are the equivalent set and reset lines of an SR flip-flop. When J is '1' and K is '0' the next state will be a 1 (i.e. Q = 1). When J is '0' and K is '1' the next state will be '0'. When J and K are '0' the next state will "hold" the previous state. When J and K are both '1' the output will toggle.

A T flip-flop is a sequential device that toggles or holds the output. When the T input is '0' the next state is equal to the previous state. When the T input is '1' the next state will be the compliment of the present state.

A D flip-flop is a sequential device that "delays" the input by one clock pulse. In other words, the input to the D flip-flop will propagate to the output of the flip-flop after the next clock pulse.

Flip-flops may be characterized in terms of transition tables, or equivalently, state transition diagrams. The transition table of a flip-flop is obtained by deducing the next state (i.e. next output) for every possible combination of input values.

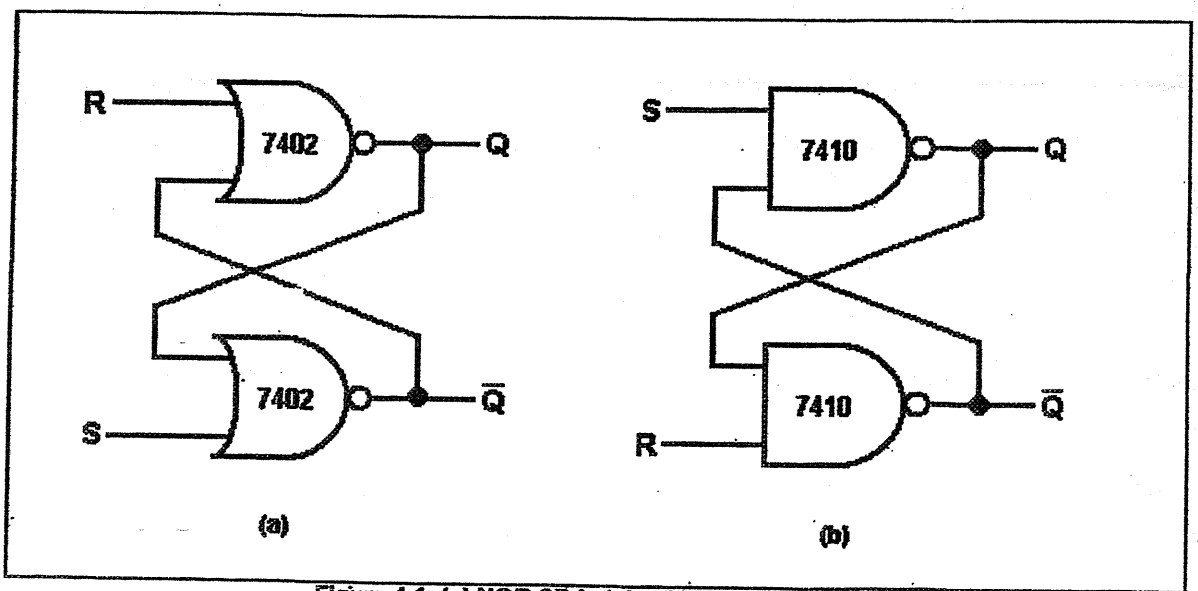


Figure 4.1: (a) NOR SR Latch (b) NAND SR Latch

PRE-LAB

1) Read all of Experiment 4 to become familiar with the Procedures for completing this experiment.

2) A state transition table for a latch is a table which lists as inputs the latch inputs (i.e. S and R for a SR latch, D for a D-type latch, etc. as well as the present value of the latch output (typically designated as Q(present)), the table lists the next state of the latch as the output (typically designated as Q(next)). For example, the state transition table for a NOR implementation would contain the following:

Table 1: State Transition Table for SR-NOR latch

S	R	Q(present)	Q(next)	Comments
0	0	0	0	Hold
0	0	1	1	Hold
0	1	0	?	
0	1	1	?	
1	0	0	?	
1	0	1	?	
1	1	0	?	
1	1	1	?	

Complete the state transition table for the NOR implementation of the SR latch. Draw the logic diagram for a NOR SR latch. Be sure to include instance names, part numbers and pin numbers as appropriate.

3) Derive the state transition table for the NAND implementation of a SR latch. Draw the its logic diagram.

4) Derive the state transition table for a NOR implementation of a SR latch with an enable input (i.e. a level-sensitive clocked SR latch). Draw it's logic diagram.

5) Derive the state-transition table for a NAND implementation of a D latch with an enable input. Draw the accompanying logic diagram.

PROCEDURE

Part 1

Connect the SR NOR latch circuit using 7402 NOR gates. Verify its functionality by testing all possible input combinations. Record your results in a state transition table.

Part 2

Connect the SR NAND latch circuit. Verify its functionality by testing all possible input combinations. Record your results in a state transition table.

Part 3

Connect the SR NOR latch with enable input. Verify its functionality by testing all possible input combinations. Record your results in a state transition table.

Part 4

Connect the D-type latch with enable input using a NAND SR latch implementation. Verify its functionality by testing all possible input combinations. Record your results in a state transition table.

QUESTIONS

1) What happens to the Q and Q' outputs of a NAND SR latch when both the S and R inputs have a logic '1' value?

2) What happens to the Q and Q' outputs of a NOR SR latch when both the S and R inputs have a logic '1' value?

3) Explain why a latch with a enable input does not change it's output value when the enable input is logic '0'.

4) What is the difference between a *sequential* circuit and a *combinational* circuit. What characteristic (in terms of hardware implementation) do all sequential circuits exhibit?

EXPERIMENT 5

ANALYSIS AND DESIGN OF COUNTERS

OBJECTIVE

- To further increase skills in connecting digital circuits and testing and debugging sequential designs.
- To gain experience in the analysis and design of sequential circuits.
- To obtain an understanding of the design and functionality of various sequential digital counter circuits.

INTRODUCTION

Analysis of Sequential Circuits:

The analysis of sequential circuits may easily be done by following several simple steps. The steps are as follows:

1) Label the inputs and outputs on the logic circuit diagram. Label each flip-flop and subscript its inputs. For example, if a circuit has two JK flip-flops and one D flip-flop, then label one JK flip-flop 'A' and its inputs J_A and K_A. The next JK flip-flop in the circuit could be named 'B' with inputs J_B and K_B. The D flip-flop may be named 'C' with input D_C.
2) Determine the flip-flop inputs in terms of the system inputs and present state outputs from each flip-flop.
3) Generate a state transition table from the equation determined in step 2.
4) Generate a state transition diagram from the table obtained in step 3.

Design of Sequential Circuits:

The design of sequential circuits may be done by reversing the step from the analysis, as follows:

1) Derive a state transition diagram from a specification.
2) Generate a state transition table from the state diagram. For each state variable, include columns in the table for the flip-flop inputs. Use the appropriate flip-flop characteristic equation to determine the values to the flip-flop inputs. For example, the characteristic equation for a JK flip-flop is $Q(t+1) = JQ' + K'Q$.
3) Derive the Boolean equation for each input of every flip-flop. Minimize the Boolean algebra by using K-maps.
4) Determine the outputs as a function of flip-flop present state variables and system inputs. Minimize the Boolean algebra by using K-maps.
5) Draw the circuit diagram.

PRE-LAB

1) Read all of Experiment 5 (pages 26-30) to become familiar with the Procedures for completing this experiment.

2) Analyze the sequential counter circuit shown in Figure 5.1. Derive the state transition table and diagram.

3) Analyze the sequential counter circuit shown in Figure 5.2. Derive the state transition table and diagram.

4) Design a sequential counter with one input and two outputs. The circuit should count up from (i.e. 0→1→2→3→0→1→2→....) when the input is high. The circuit should count down (i.e. 3→2→1→0→3→2→1→....) when the input is low. The two outputs should represent the binary value of the count. Compose the state transition diagram and table. Use JK flip-flops to implement the design. Draw the logic circuit diagram. Don't forget the label each gate and flip-flop with its instance name and number, and associated pin numbers.

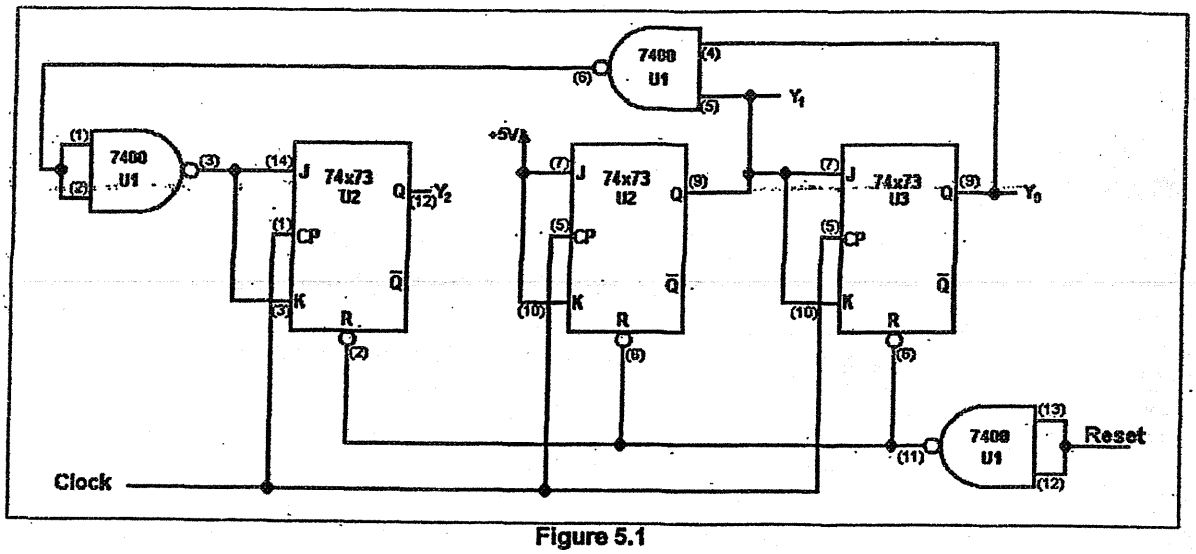

7400
U1
74x73
U2
74x73
U2
74x73
U3
7400
U1
7400
U1
+5V
J
K
CP
R
Q
$\overline{Q}$
Y_2
Y_1
Y_0
Clock
Reset

Figure 5.1

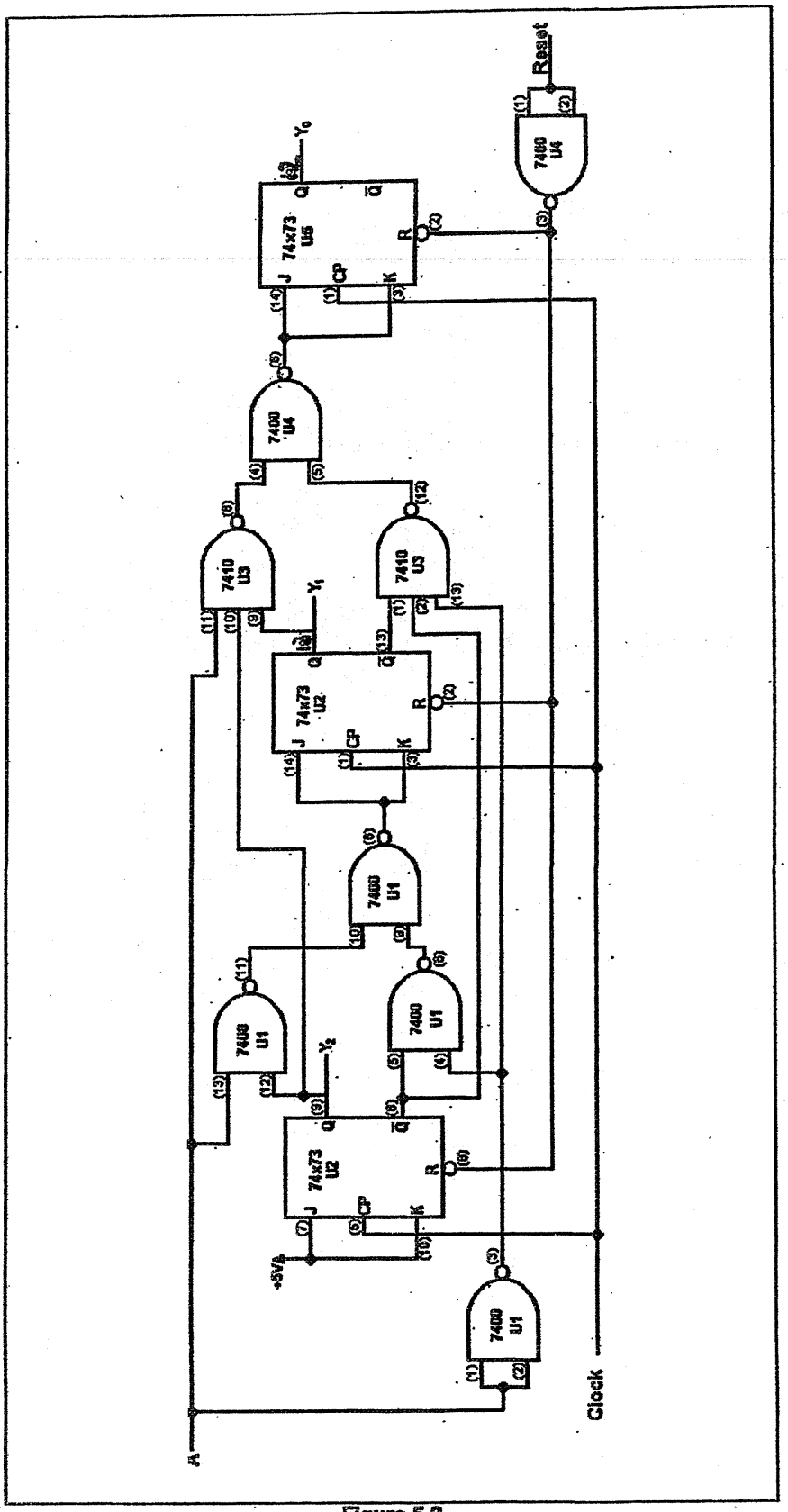

Reset
7400 U4
Y0
74x73 U5
J
CP
K
R
Q
7400 U4
7410 U3
7410 U3
Y1
74x73 U2
7400 U1
7400 U1
7400 U1
Y2
74x73 U2
+5V
7400 U1
Clock
A

Figure 5.2

PROCEDURE

Part 1

Connect the counter circuit shown in Figure 5.1. Verify its functionality by testing all possible counter values. Record the results in a state transition table.

Part 2

Connect the counter circuit given in Figure 5.2. Verify its functionality by testing all possible counter values. Record the results in a state transition table.

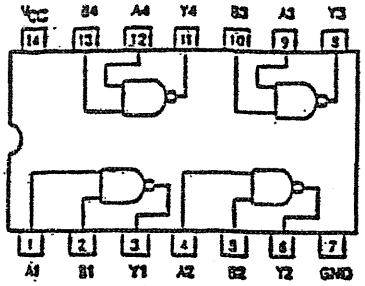
Part 3

Connect the up-down counter design in the Pre-Lab. Verify its functionality by testing all possible counter values. Record the results in a state transition table.

APPENDIX A

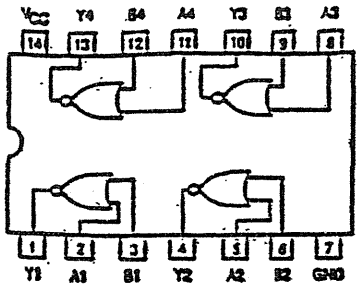
Specification of TTL Integrated Circuits

LOGIC DIAGRAM



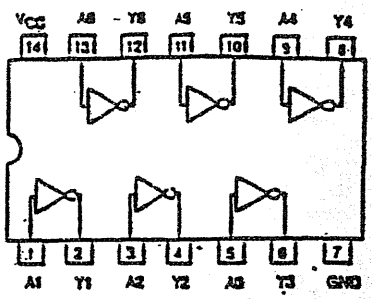
74LS00

LOGIC DIAGRAM



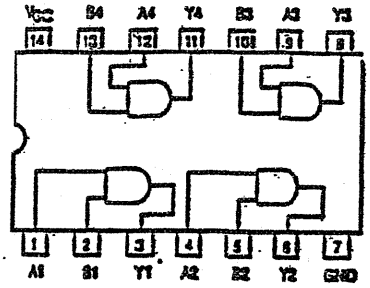
74LS02

LOGIC DIAGRAM



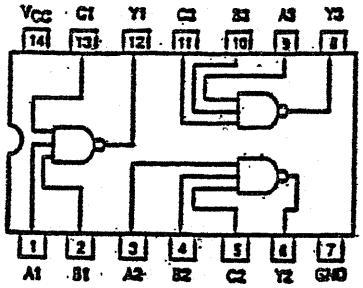
74LS04

LOGIC DIAGRAM



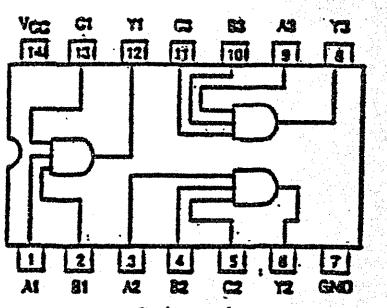
74LS08

LOGIC DIAGRAM



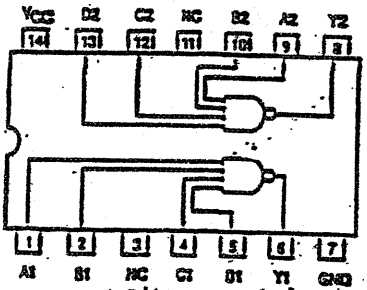
74LS10

LOGIC DIAGRAM



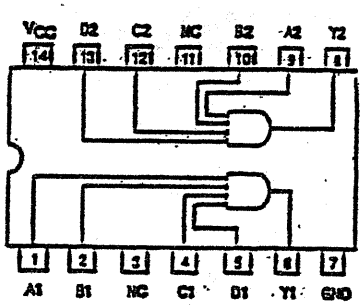
74LS11

LOGIC DIAGRAM



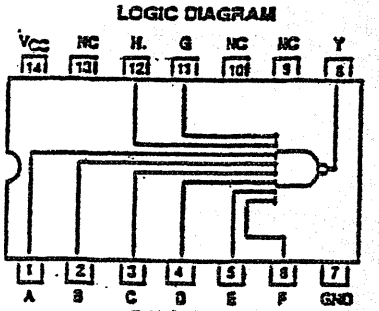
74LS20

LOGIC DIAGRAM



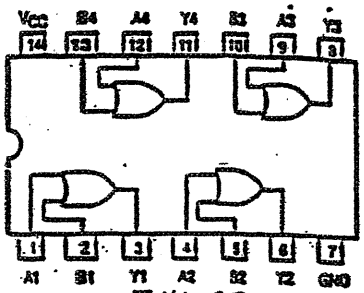
74LS21

LOGIC DIAGRAM



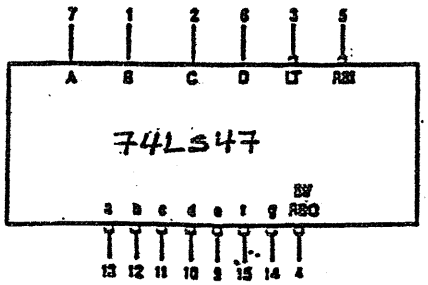
74LS30

LOGIC DIAGRAM

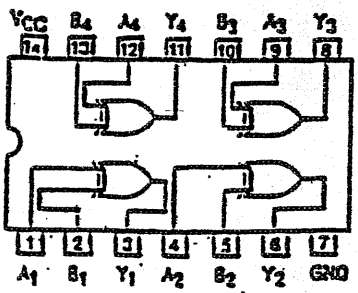


74LS32

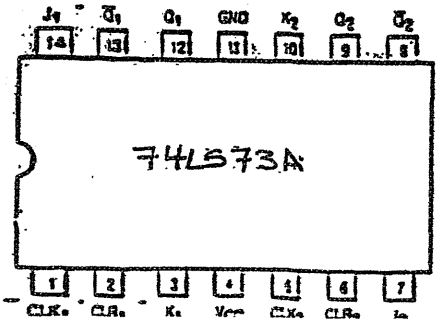
LOGIC SYMBOL

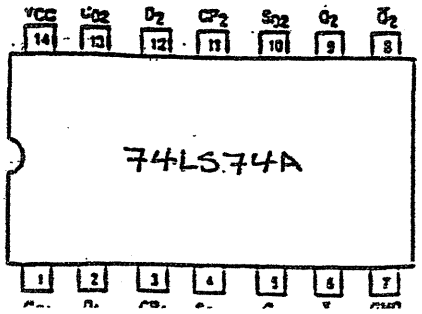


LOGIC DIAGRAM



74LS86





QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

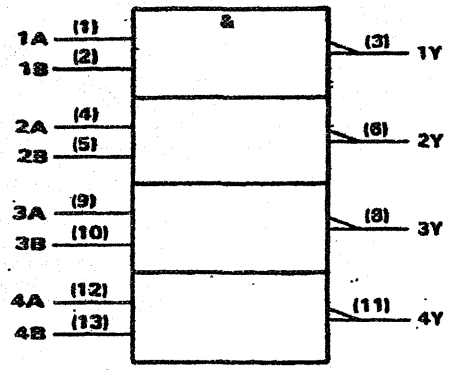
These devices contain four independent 2-input NAND gates.

The SN5400, SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

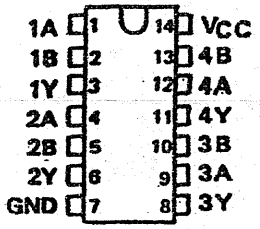
logic symbol†



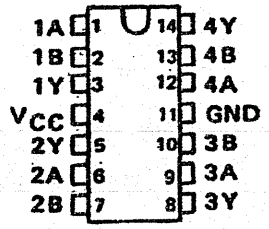
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

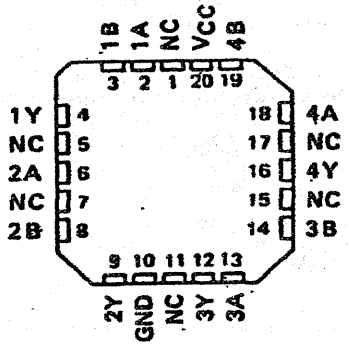
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400 . . . N PACKAGE
SN74LS00, SN74S00 . . . D OR N PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)

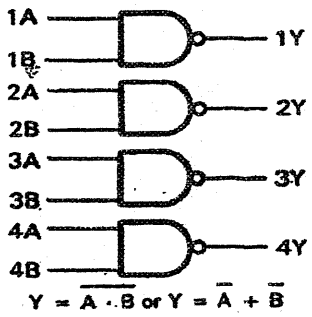


SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



$Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

	SN5400			SN7400			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

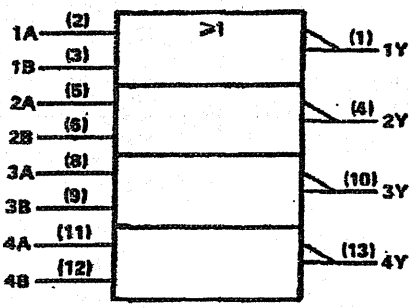
These devices contain four independent 2-input NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

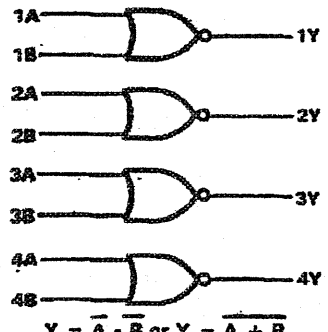
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



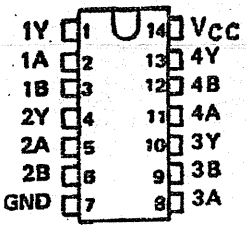
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

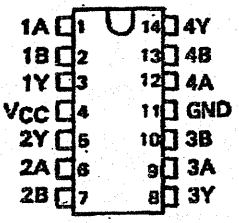


$Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$

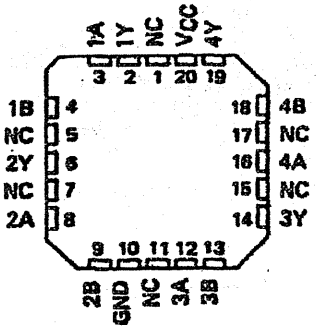
SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE
(TOP VIEW)



SN5402 . . . W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54LS02			SN74LS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54LS02			SN74LS02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.6	3.2		1.6	3.2	mA
I_{CCL}	V_{CC} = MAX,	See Note 2			2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ,	C_L = 15 pF		10	15	ns
t_{PHL}						10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

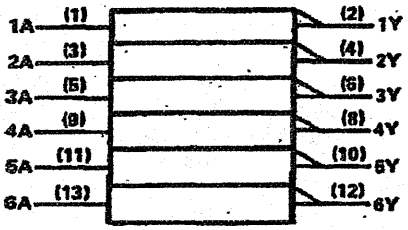
These devices contain six independent inverters.

The SN5404, SN54LS04, and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74LS04, and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

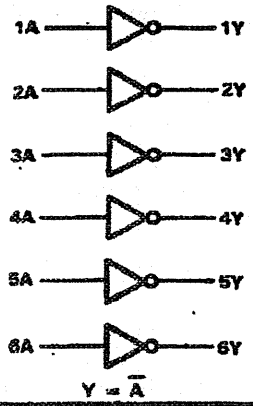
INPUTS A	OUTPUT Y
H	L
L	H

logic symbol†



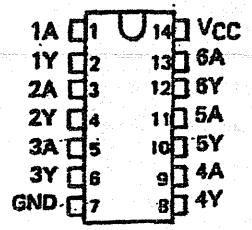
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

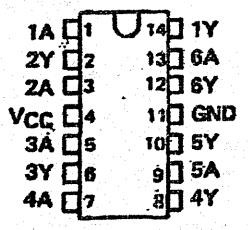


$Y = \overline{A}$

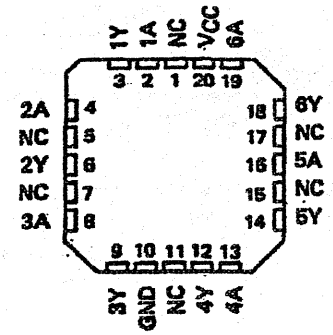
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404 . . . N PACKAGE
SN74LS04, SN74S04 . . . D OR N PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

recommended operating conditions

	SN54LS04			SN74LS04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS04			SN74LS04			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4			0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS} §	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

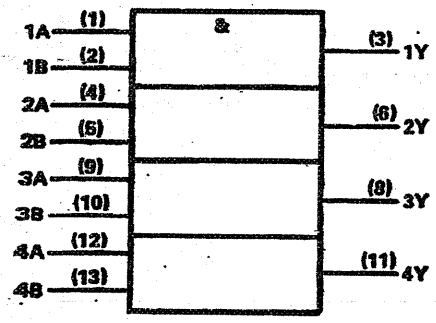
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C.

FUNCTION TABLE (each gate)

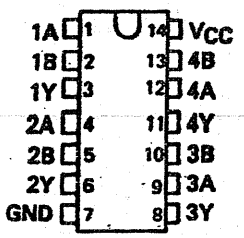
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

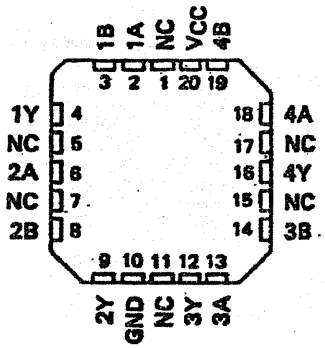


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE
(TOP VIEW)

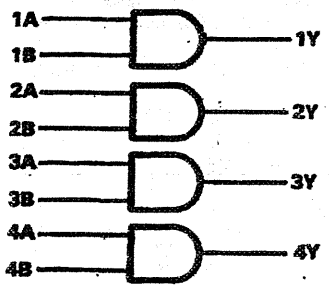


SN54LS08, SN54S08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.8			−0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5408			SN7408			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		11	21		11	21	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		17.5	27	ns
t_{PHL}					12	19	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

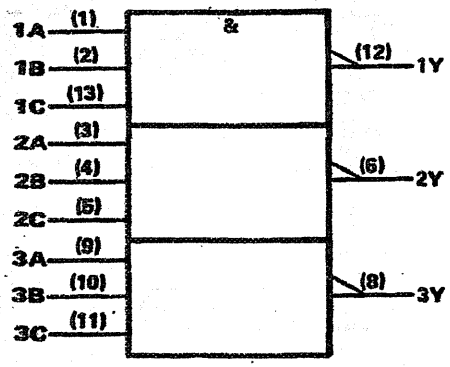
These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10, and SN54S10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7410, SN74LS10, and SN74S10 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

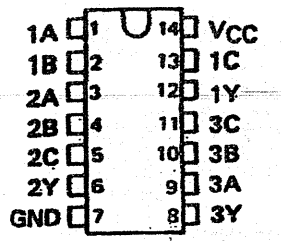


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

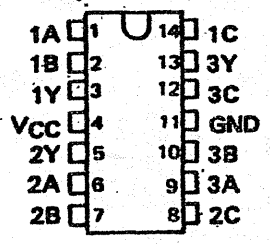
positive logic

$$Y = \overline{A \cdot B \cdot C} \text{ or } Y = \overline{A} + \overline{B} + \overline{C}$$

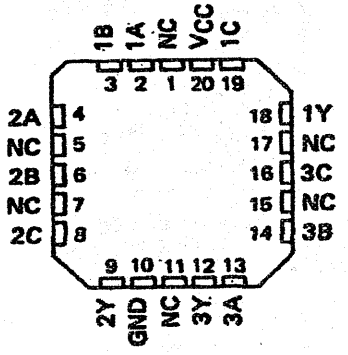
SN5410 . . . J PACKAGE
SN54LS10, SN54S10 . . . J OR W PACKAGE
SN7410 . . . N PACKAGE
SN74LS10, SN74S10 . . . D OR N PACKAGE
(TOP VIEW)



SN5410 . . . W PACKAGE
(TOP VIEW)

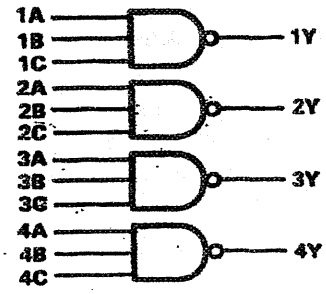


SN54LS10, SN54S10 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



recommended operating conditions

	SN54LS10			SN74LS10			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS10			SN74LS10			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4			0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		0.6	1.2		0.6	1.2	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		1.8	3.3		1.8	3.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

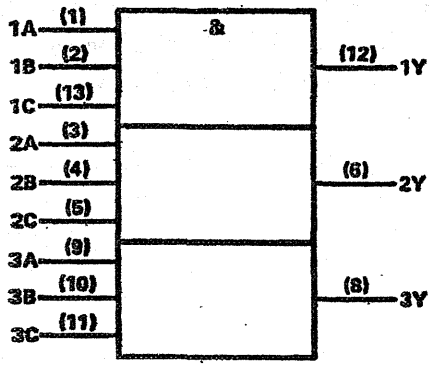
These devices contain three independent 3-input AND gates.

The SN54LS11 and SN54S11 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS11 and SN74S11 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

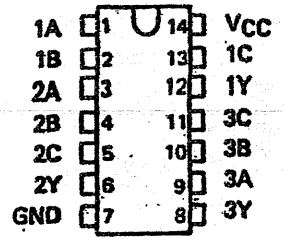
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

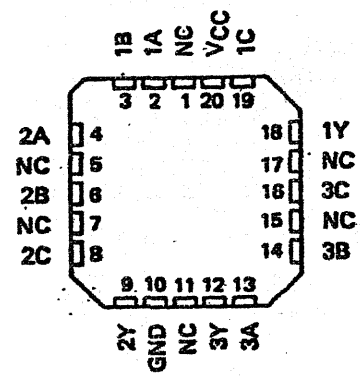


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN54LS11, SN74S11 . . . J OR W PACKAGE
SN74LS11, SN74S11 . . . D OR N PACKAGE
(TOP VIEW)

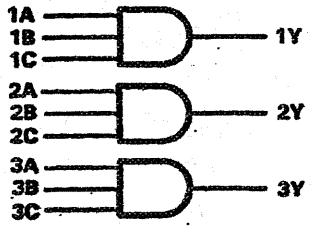


SN54LS11, SN54S11 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$Y = A \cdot B \cdot C$ or

$Y = \overline{\overline{A} + \overline{B} + \overline{C}}$

recommended operating conditions

	SN54LS11			SN74LS11			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS11			SN74LS11			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		1.8	3.6		1.8	3.6	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		3.3	6.6		3.3	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	R_L = 2 kΩ, C_L = 15 pF		8	15	ns
t_{PHL}					10	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

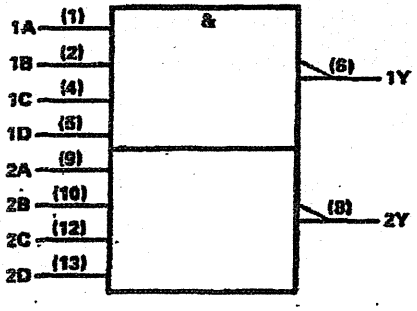
These devices contain two independent 4-input NAND gates.

The SN5420, SN54LS20, and SN54S20 are characterized for operation over the full military range of −55°C to 125°C. The SN7420, SN74LS20, and SN74S20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

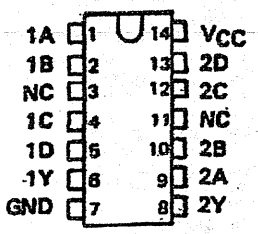
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†

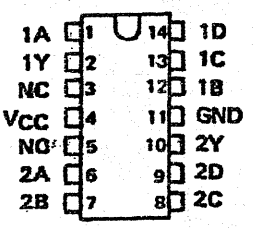


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

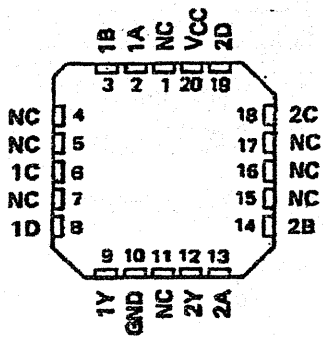
SN5420 . . . J PACKAGE
SN54LS20, SN54S20 . . . J OR W PACKAGE
SN7420 . . . N PACKAGE
SN74LS20, SN74S20 . . . D OR N PACKAGE
(TOP VIEW)



SN5420 . . . W PACKAGE
(TOP VIEW)

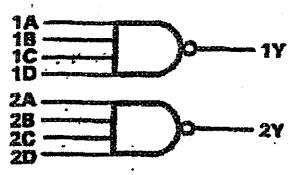


SN54LS20, SN54S20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram



positive logic $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

recommended operating conditions

	SN54LS20			SN74LS20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS20			SN74LS20			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4			0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		0.4	0.8		0.4	0.8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

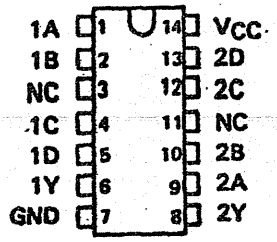
These devices contain two independent 4-input AND gates.

The SN54LS21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS21 is characterized for operation from 0°C to 70°C.

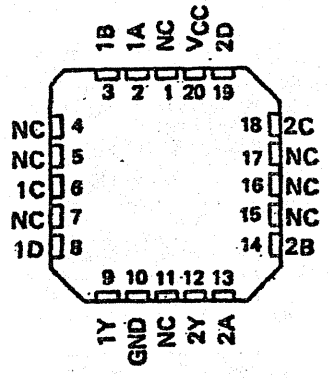
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

SN54LS21 . . . J OR W PACKAGE
SN74LS21 . . . D OR N PACKAGE
(TOP VIEW)

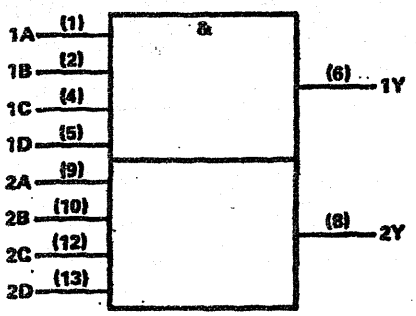


SN54LS21 . . . FK PACKAGE
(TOP VIEW)



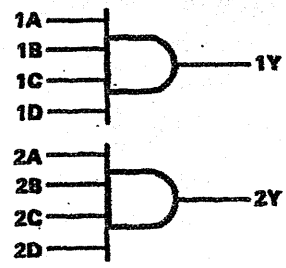
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram



(positive logic) $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$

recommended operating conditions

	SN54LS21			SN74LS21			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS21			SN74LS21			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		2.2	4.4		2.2	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		8	15	ns
t_{PHL}					10	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

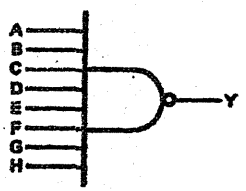
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military range of −55°C to 125°C. The SN7430, SN74LS30, and SN74S30 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic diagram

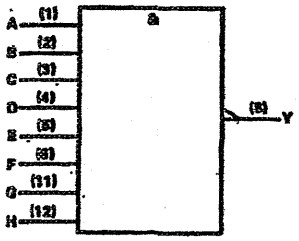


positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

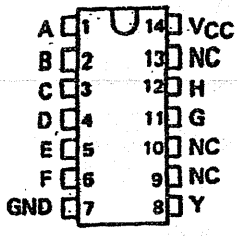
logic symbol†



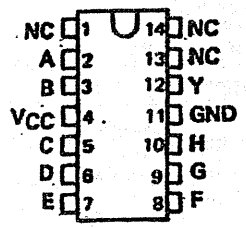
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

‡Pin numbers shown are for D, J, N, and W packages.

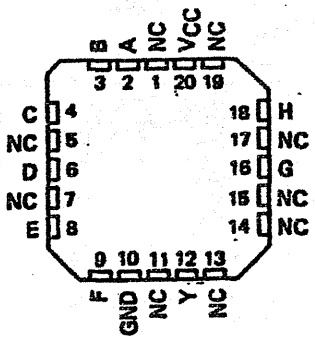
SN5430 . . . J PACKAGE
SN54LS30, SN54S30 . . . J OR W PACKAGE
SN7430 . . . N PACKAGE
SN74LS30, SN74S30 . . . D OR N PACKAGE
(TOP VIEW)



SN5430 . . . W PACKAGE
(TOP VIEW)



SN54LS30, SN54S30 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5430 . . . . . −55°C to 125°C
SN7430 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5430			SN7430			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5430			SN7430			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0		1	2		1	2	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		3	6		3	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 400 Ω, C_L = 15 pF		13	22	ns
t_{PHL}					8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

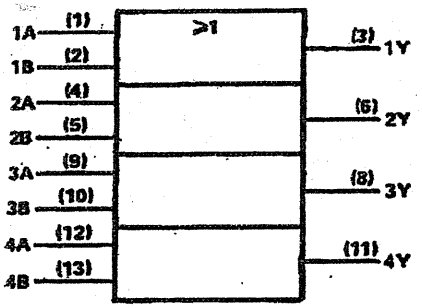
These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of −55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

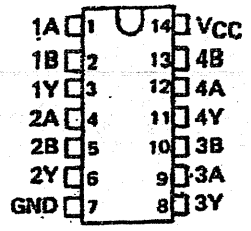
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

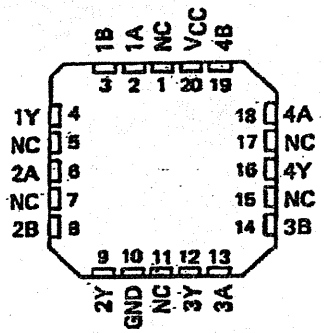


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, or W packages.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . N PACKAGE
SN74LS32, SN74S32 . . . D OR N PACKAGE
(TOP VIEW)

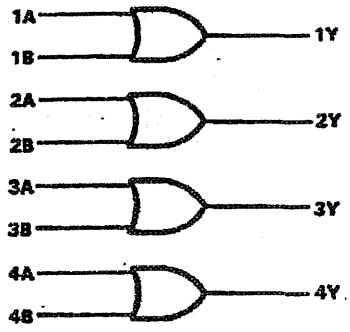


SN54LS32, SN54S32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram



positive logic

$Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$

recommended operating conditions

		SN54LS32			SN74LS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS32			SN74LS32			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IL} = MAX,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	See Note 2			3.1	6.2		3.1	6.2	mA
I_{CCL}	V_{CC} = MAX,	V_I = 0 V			4.9	9.8		4.9	9.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ,	C_L = 15 pF		14	22	ns
t_{PHL}						14	22	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

SDLS111 – MARCH 1974 – REVISED MARCH 1988

'46A, '47A, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

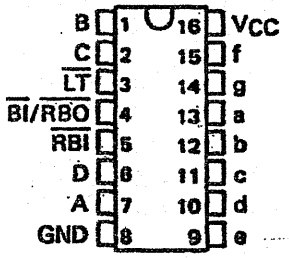
'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

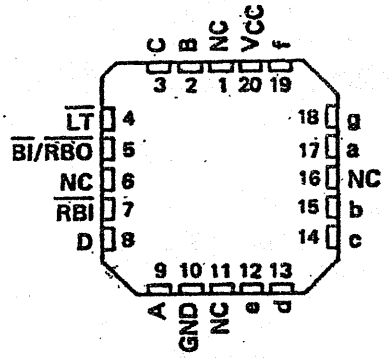
'LS49 feature

- Open-Collector Outputs
- Blanking Input

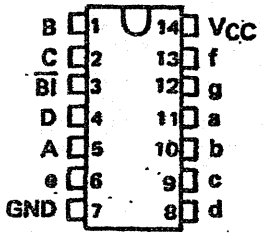
SN5446A, SN5447A, SN54LS47, SN5448, SN54LS48 . . . J PACKAGE
SN7446A, SN7447A, SN7448 . . . N PACKAGE
SN74LS47, SN74LS48 . . . D OR N PACKAGE
(TOP VIEW)



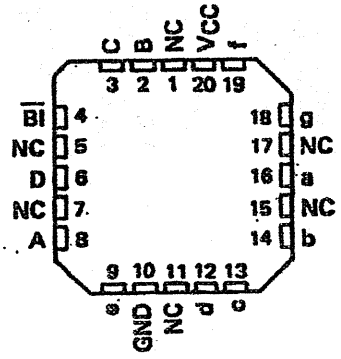
SN54LS47, SN54LS48 . . . FK PACKAGE
(TOP VIEW)



SN54LS49 . . . J OR W PACKAGE
SN74LS49 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS49 . . . FK PACKAGE
(TOP VIEW)



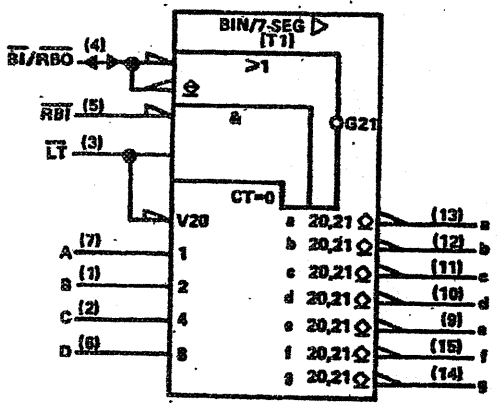
NC — No internal connection

- **All Circuit Types Feature Lamp Intensity Modulation Capability**

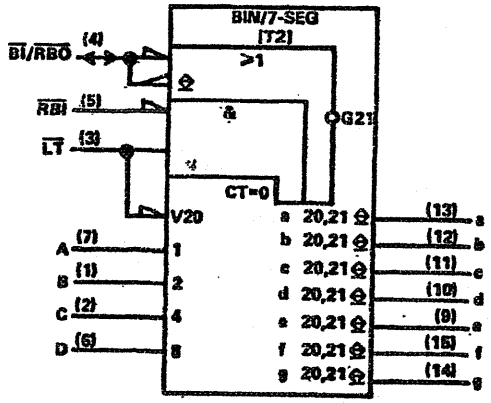
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J,W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols†

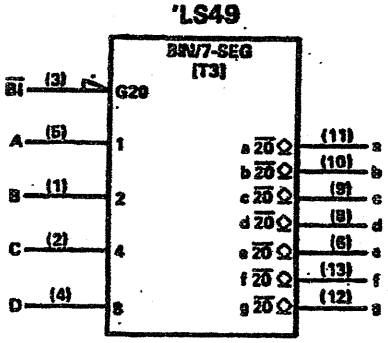
'46A, '47A, 'LS47



'48, 'LS48



'LS49



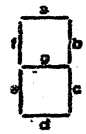
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

description

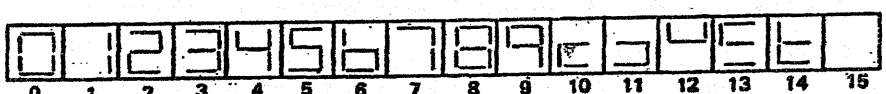
The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. The '48, 'LS48, and 'LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except 'LS49 have full ripple-blanking input/output controls and a lamp test input. The 'LS49 circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{BI}$), which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 and '247 and the SN54LS247/SN74LS247 and 'LS248 compose the 6 and the 9 with tails and were designed to offer the designer a choice between two indicator fonts.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'LS47 FUNCTION TABLE (T1)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†$\overline{BI}/\overline{RBO}$ is wire AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$).

'48, 'LS48
FUNCTION TABLE (T2)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

† $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$).

'LS49
FUNCTION TABLE (T3)

DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	$\overline{BI}$	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are low regardless of the level of any other input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN5446A, SN5447A . . . . . –55°C to 125°C
SN7446A, SN7447A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	$\overline{BI}/\overline{RBO}$			–200			–200			–200			–200	μA
Low-level output current, I_{OL}	$\overline{BI}/\overline{RBO}$			8			8			8			8	mA
Operating free-air temperature, T_A		–55		125	–55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = –12 mA				–1.5	V
V_{OH}	High-level output voltage	$\overline{BI}/\overline{RBO}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –200 μA		2.4	3.7		V
V_{OL}	Low-level output voltage	$\overline{BI}/\overline{RBO}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.27	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 40 mA			0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$	V_{CC} = MAX, V_I = 0.4 V				–1.6	mA
		$\overline{BI}/\overline{RBO}$					–4	
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$	V_{CC} = MAX				–4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN54'		64	85	mA
				SN74'		64	103	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 120 Ω, See Note 3			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from $\overline{RBI}$ input				100	ns
t_{on}	Turn-on time from $\overline{RBI}$ input				100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

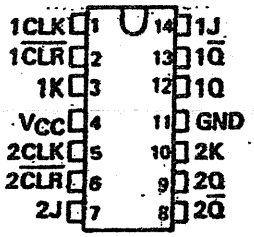
description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C.

SN5473, SN54LS73A . . . J OR W PACKAGE
SN7473 . . . N PACKAGE
SN74LS73A . . . D OR N PACKAGE
(TOP VIEW)



'73
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

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TEXAS INSTRUMENTS
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recommended operating conditions

			SN5473			SN7473			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		$\overline{CLR}$ low	25			25			
t_{su}	Input setup time before CLK↑		0			0			ns
t_h	Input hold time data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5473			SN7473			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	$\overline{CLR}$ or CLK						80			80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	$\overline{CLR}$						−3.2			−3.2	
	CLK						−3.2			−3.2	
I_{OS}§		V_{CC} = MAX			−20		−57	−18		−57	mA
I_{CC}¶		V_{CC} = MAX,	See Note 2			10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
¶ Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	20		MHz
t_{PLH}	$\overline{CLR}$	$\overline{Q}$			16	25	ns
t_{PHL}		Q			25	40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			16	25	ns
t_{PHL}					25	40	ns

f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

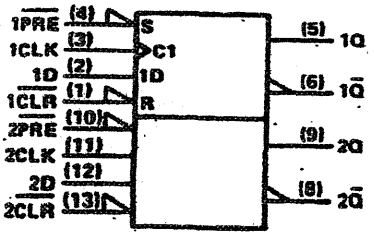
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

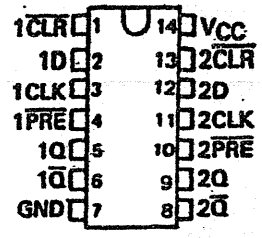
†The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol‡

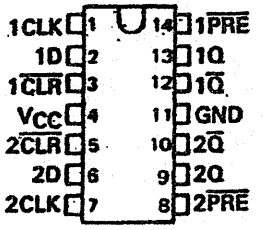


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

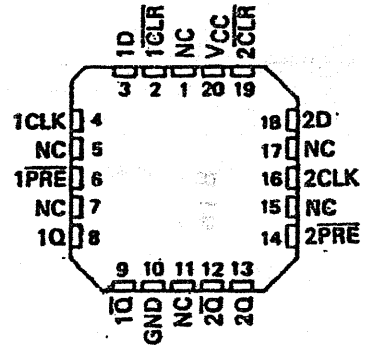
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

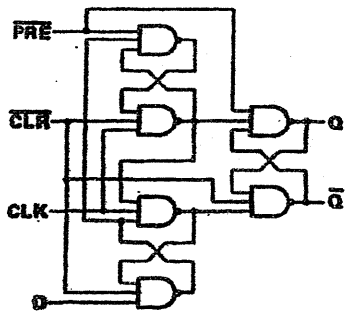


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS
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recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS74A			SN74LS74A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 8 mA					0.35	0.5	
I_I	D or CLK	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$				0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$				40			40	
I_{IL}	D or CLK	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$				−0.8			−0.8	
I_{OS}§		V_{CC} = MAX, See Note 4	−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX, See Note 2		4	8		4	8	mA

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

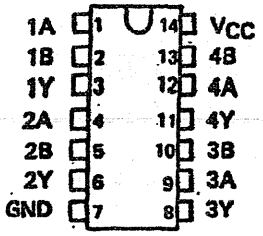
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.

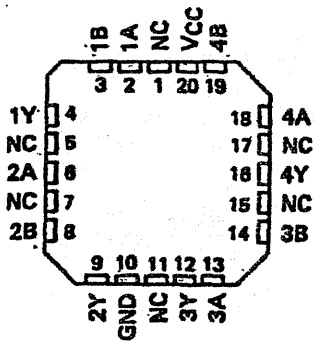
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE
SN7486 . . . N PACKAGE
SN74LS86A, SN74S86 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

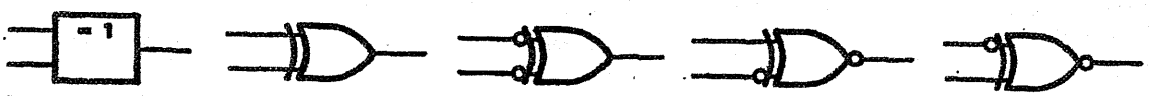
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN5486, 54LS86A, and the SN54S86 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7486, SN74LS86A, and the SN74S86 are characterized for operation from 0°C to 70°C.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



These are five equivalent Exclusive-OR symbols valid for an '86 or 'LS86A gate in positive logic; negation may be shown at any two ports.

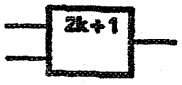
LOGIC IDENTITY ELEMENT

The output is active (low) if all inputs stand at the same logic level (i.e., A=B).

EVEN-PARITY

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5486 . . . . . −55°C to 125°C
SN7486 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5486			SN7486			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5486			SN7486			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		30	43		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 400 Ω, See Note 3		15	23	ns
t_{PHL}					11	17	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					13	22	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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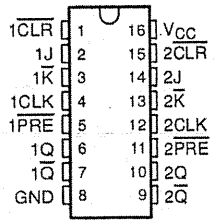
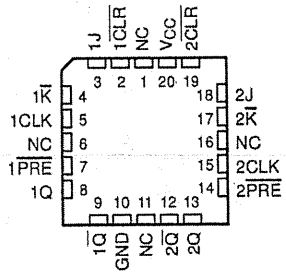
- Wide Operating Voltage Range of 2 V to 6 V
- Low Input Current of 1 μA Max
- High-Current Outputs Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40-μA Max I_{CC}
- Typical t_{pd} = 12 ns
- ±4-mA Output Drive at 5 V

SN54HC109 . . . J OR W PACKAGE
SN74HC109 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC109 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{K}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC109N	SN74HC109N
	SOIC – D	Tube of 40	SN74HC109D	HC109
		Reel of 2500	SN74HC109DR	
		Reel of 250	SN74HC109DT	
	SOP – NS	Reel of 2000	SN74HC109NSR	HC109
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC109J	SNJ54HC109J
	CFP – W	Tube of 150	SNJ54HC109W	SNJ54HC109W
	LCCC – FK	Tube of 55	SNJ54HC109FK	SNJ54HC109FK

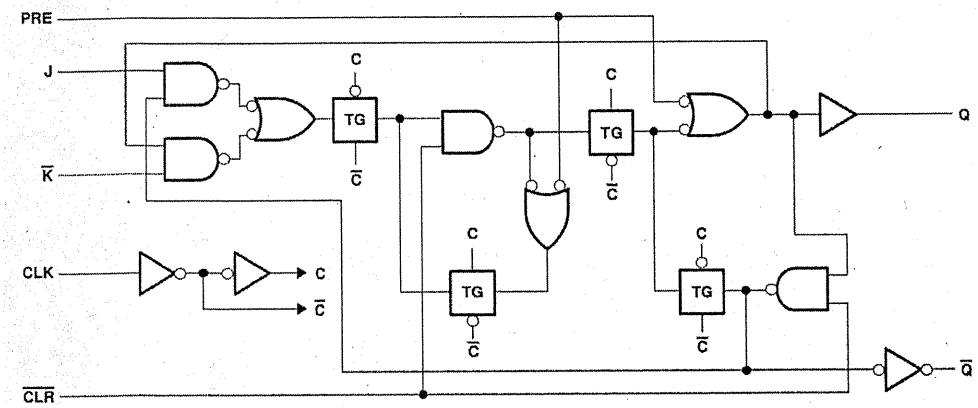
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

† This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Package thermal impedance, θ_{JA} (see Note 1): D package ..... 73°C/W
N package ..... 67°C/W
NS package ..... 64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK, J, or W packages ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS packages ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			SN54HC109			SN74HC109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.3			0.5	V
		V_{CC} = 4.5 V			0.9			1.35	
		V_{CC} = 6 V			1.2			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			4		80		40	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC109		SN74HC109		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data (J, $\overline{K}$)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time	Data after CLK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		ns
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		60	230		345		290	ns
			4.5 V		15	46		69		58	
			6 V		12	39		59		49	
	CLK	Q or $\overline{Q}$	2 V		50	175		250		220	
			4.5 V		15	35		50		44	
			6 V		12	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF