Virtex-4 Introduction

September 13, 2004

Agenda

- Introduction
- High-performance FPGA design
- Embedded processing
- High-speed serial connectivity
- High-performance DSP

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- Introduction
- High-performance FPGA design
- Embedded processing
- High-speed serial connectivity
- High-performance DSP

News

- Xilinx ramps Virtex-4 shipments
- Xilinx ships ISE 6.3i tools with support for Virtex-4
- Xilinx forms DSP division with new Vice President & General Manager Omid Tahernia
- Xilinx forms new Embedded Processing division

Customers Require Programmability

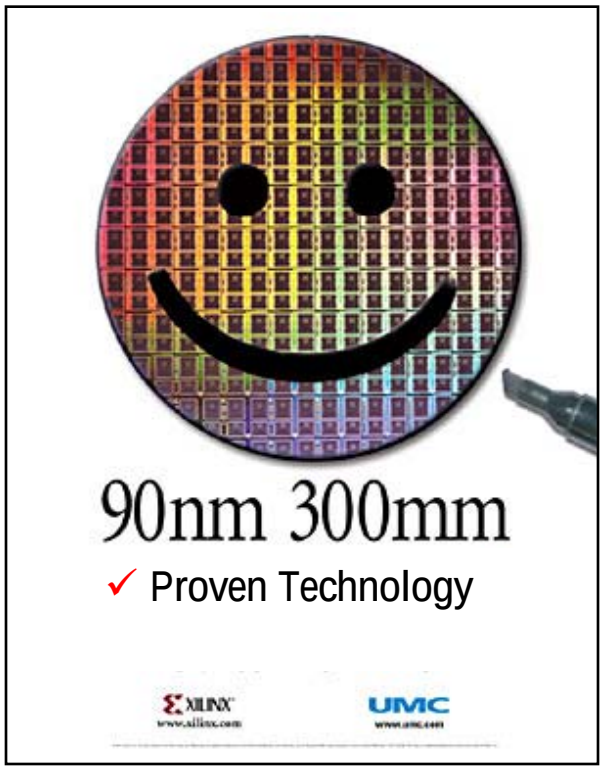
ASIC/FPGA Vendor Ranking

	1998	1999	2000	2001	2002	2003
1.	Lucent	IBM	IBM	IBM	IBM	IBM
2.	IBM	Lucent	Lucent	Agere	NEC	NEC
3.	NEC	NEC	LSI Logic	LSI Logic	Agere	XILINX
4.	LSI Logic	LSI Logic	NEC	NEC	XILINX	
5.	Fujitsu	Fujitsu	XILINX	XILINX		
6.	Altera	XILINX				
7.	XILINX					

Source: Gartner Dataquest
Note: Lucent spun-off their semiconductor division in 2001 creating Agere Systems

90nm Commitment Fulfilled

- Virtex-4 Platform FPGA
  - 2nd family shipping on 90nm
- Spartan-3 in full production
  - Lowest cost FPGA
- First FPGA company to ship 90nm devices
  - Shipping since March 2003



Xilinx Trusted Supplier of Programmable Systems

- Xilinx FPGAs for Embedded Processing
  - 42,000+ 8-bit PicoBlaze downloads
  - 8,800+ 32-bit UltraController downloads
  - 10,000+ Platform Studio Suites
    - Includes MicroBlaze
- Xilinx FPGAs for High-Speed Serial Connectivity
  - 7 out of 10 Virtex-II Pro designs using Multi-Gigabit Transceivers (up to 3.125Gbs)
- Xilinx FPGAs for high-performance DSP
  - 1/3 of Xilinx total FPGA design wins

JPMorgan Chase Spectacular
(Time Square, NY)
Uses 343 Xilinx FPGAs
Integrates 1000+ PicoBlaze processors
Distributed Processing

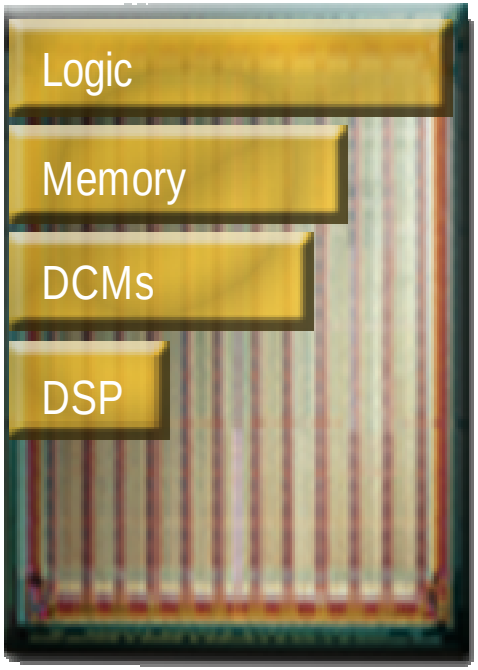
Source: Xilinx Estimates

Breakthrough Performance at the Lowest Cost

- World's fastest FPGA:
  Beats Competing FPGAs in EVERY Performance Category
  - 500 MHz clocks, >1Gbps LVDS, 10.3125 Gbps transceivers
- 1 – 5 Watts Lower Power per FPGA
  - 73% lower static power, Up to 86% lower dynamic power, 94% lower In-Rush current
- 7x less SSO Noise and Crosstalk
  - Superior signal integrity enabled by unique packaging and validated by SI experts (E.g., Dr. Howard Johnson)
- World's highest capacity FPGA
  - 200,000 logic cells, integrated IP blocks
- Industry's lowest system cost
  - Selection of 17 different devices and 3 domain optimized platforms
- Highest – Performance interfaces made easy
  - Hardware proven support for DDR2 SDRAM, DDR SDRAM, QDR II SRAM, RLDRAM II

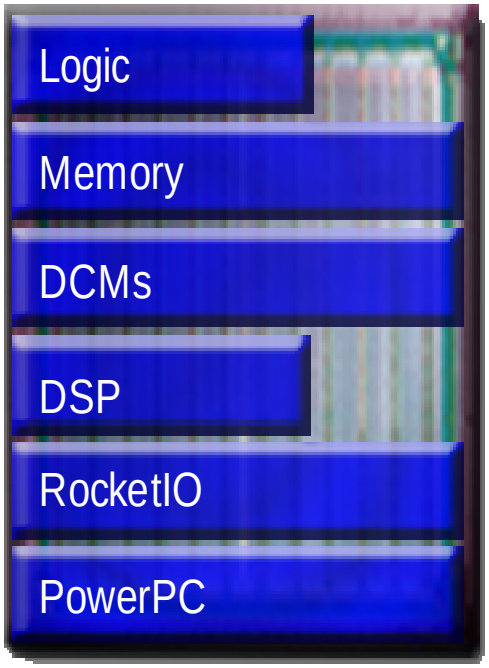
Multiple Platforms
Endless Possibilities

LX Platform
Highest logic density & performance



SX Platform
Unrivaled DSP performance

FX Platform
Only FPGA with hard µP & serial transceivers

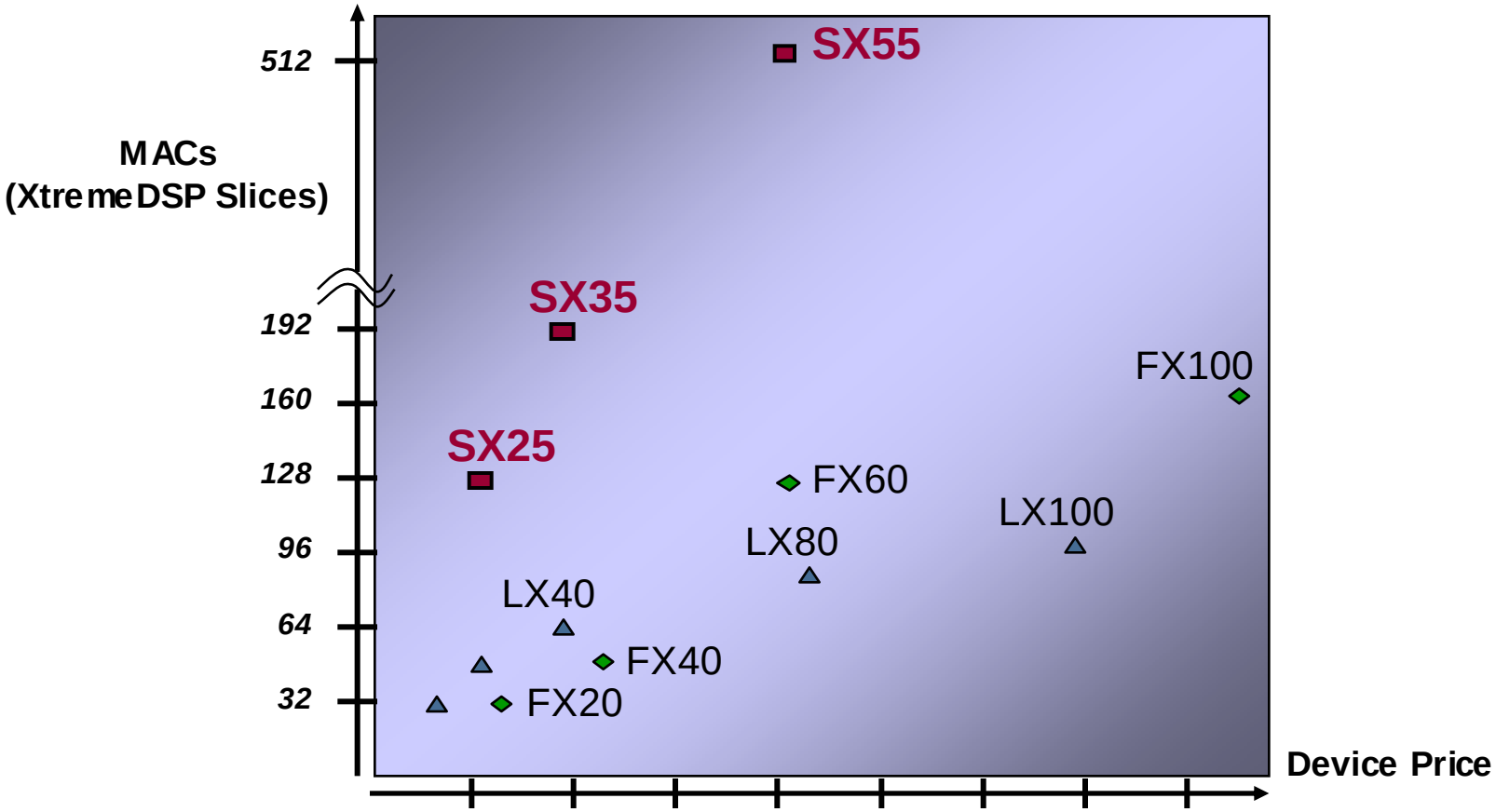


Enabled by the ASMBL Architecture

Choice of 17 Devices

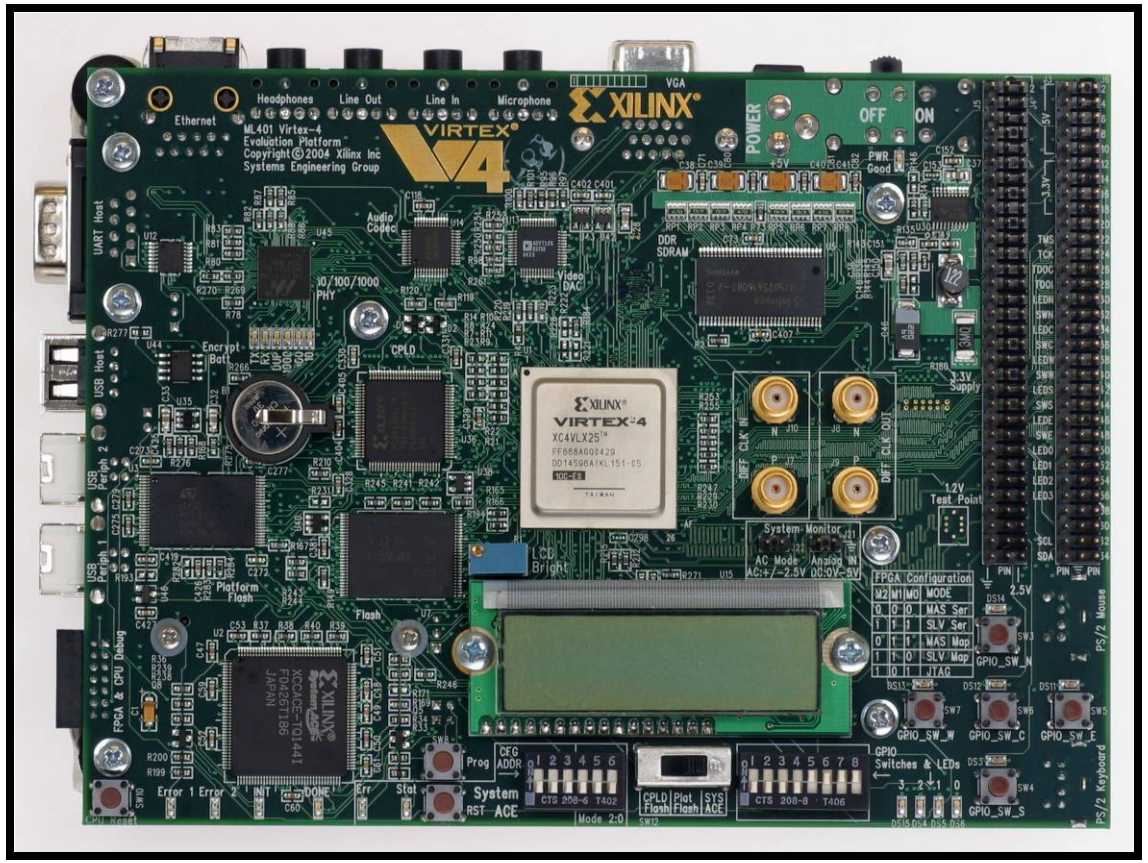
Device	Logic Cells	Block RAM [Kb]	DCM	SelectIO	XtremeDSP Slice	PowerPC	10/100/ 1000 EMAC	RocketIO transceiver
XC4VLX15	13,824	864	4	320	32	-	-	-
XC4VLX25	24,192	1,296	8	448	48	-	-	-
XC4VLX40	41,472	1,728	8	640	64	-	-	-
XC4VLX60	59,904	2,880	8	640	64	-	-	-
XC4VLX80	80,640	3,600	12	768	80	-	-	-
XC4VLX100	110,592	4,320	12	960	96	-	-	-
XC4VLX160	152,064	5,184	12	960	96	-	-	-
XC4VLX200	200,448	6,048	12	960	96	-	-	-
XC4VSX25	23,040	2,304	4	320	128	-	-	-
XC4VSX35	34,560	3,456	8	448	192	-	-	-
XC4VSX55	55,296	5,760	8	640	512	-	-	-
XC4VFX12	12,312	648	4	320	32	1	2	-
XC4VFX20	19,224	1,224	4	320	32	1	2	8
XC4VFX40	41,904	2,592	8	448	48	2	4	12
XC4VFX60	56,880	4,176	12	576	128	2	4	16
XC4VFX100	94,896	6,768	12	768	160	2	4	20
XC4VFX140	142,128	9,936	20	896	192	2	4	24

Example: SX Optimized for High-Performance DSP



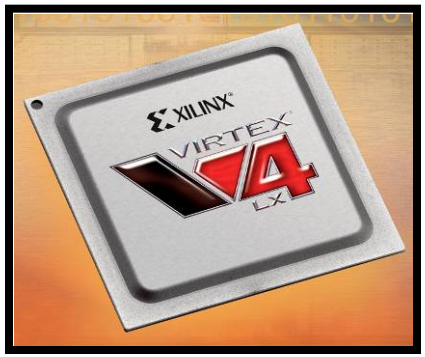
SX Provides highest ratio of XtremeDSP slices to logic (price)

Design Tools and First Silicon Available Now



Design Kit Example: Virtex-4 ML401 Evaluation Platform

ISE 6.3i with Virtex-4 support
(shipping EA since Feb '04)



XC4VLX25 shipping NOW
(EA shipment since Jun '04)

Agenda

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- High-speed serial connectivity
- High-performance DSP

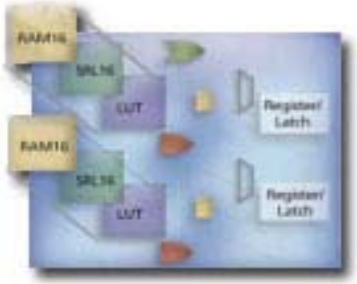
Virtex-4 Addresses Need for Higher Performance

Customer challenges
- Meeting timing in high-performance systems
- Clock management, clock edge control and clock quality
- Signal integrity, including ground bounce and jitter

Virtex-4 – delivers up to 2x performance

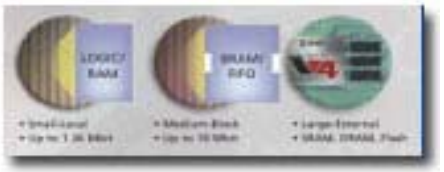
- Hard IP with guaranteed timing
- Enhanced clock management
- Improved signal integrity

Breakthrough Innovation: Embedded Hard IP



200,000
Logic Cells

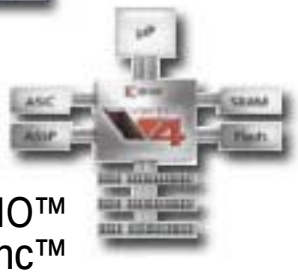
500 MHz Xesium™
Differential Clocking



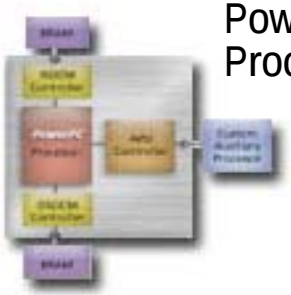
500 MHz BRAM
with FIFO & ECC

0.6-10.3125 Gbps
RocketIO™
Transceivers

AES Secure Chip
Design Security



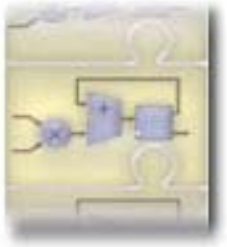
1 Gbps SelectIO™
with ChipSync™



PowerPC®
Processor with APU

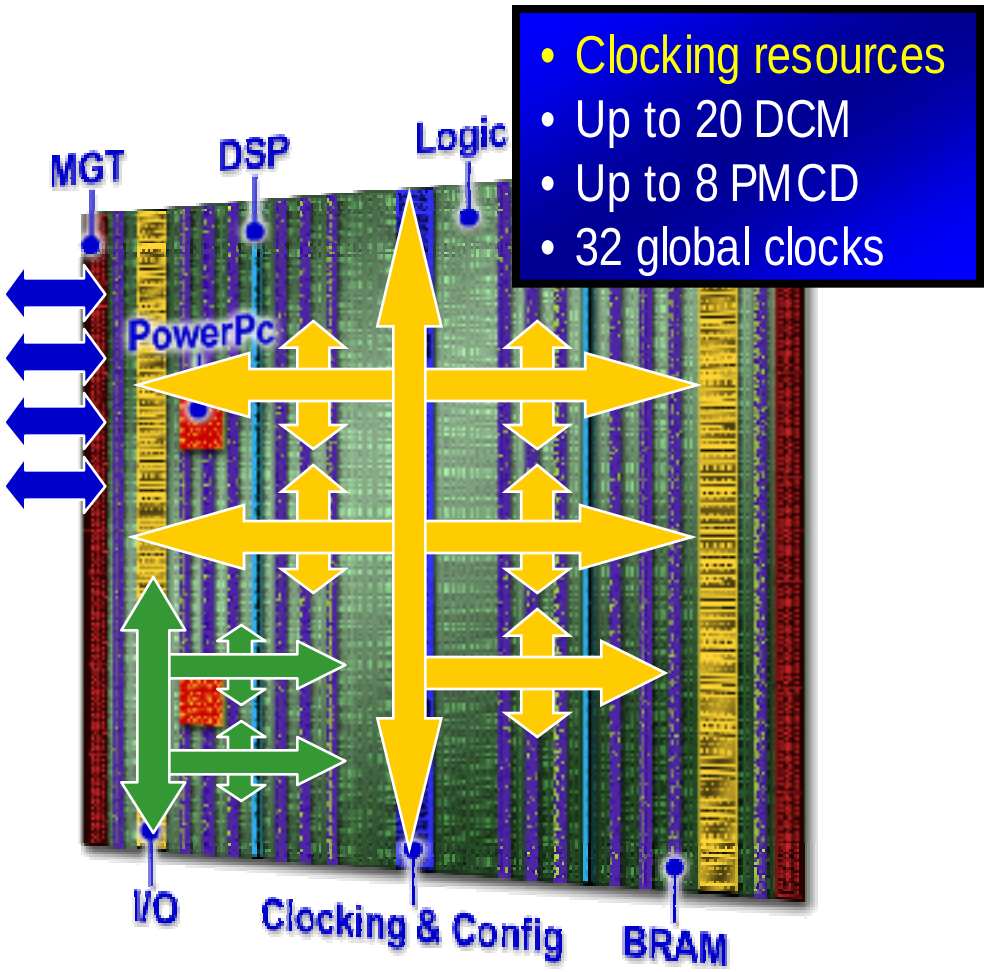
10/100/1000
Ethernet MAC

500 MHz
XtremeDSP™ Slice



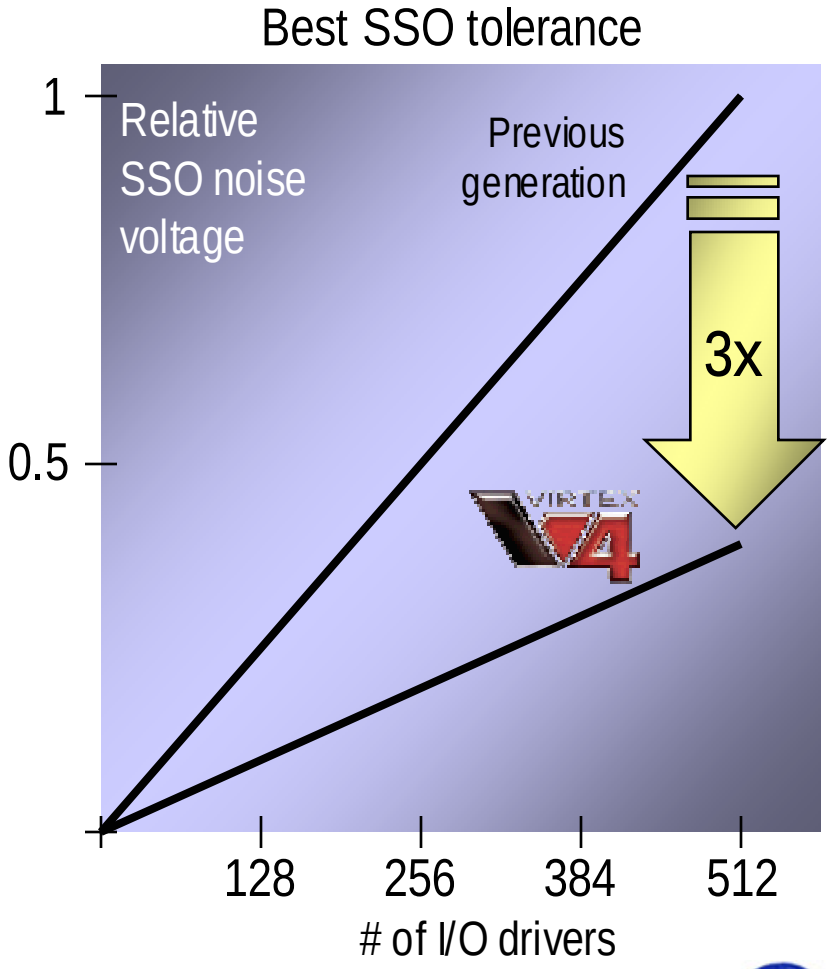
Breakthrough Innovation: Enhanced Clock Management

- Xesium™ clocking technology
- Better performance & quality
  - Differential clock distribution
  - 500 MHz internal clocks
- Simplified design
  - ~2x more clocking resources over Virtex-II Pro
  - Easy-to-use wizard



Breakthrough Innovation: Improved Signal Integrity

- High-speed systems require low-skew clock & wide data paths
  - More signals are switching within a very short time
  - Potential malfunction through ground bounce and jitter
- Virtex-4 provides industry's best noise resistance
  - Best PWR/GND pairs to I/Os ratio
  - Best PWR/GND pins distribution

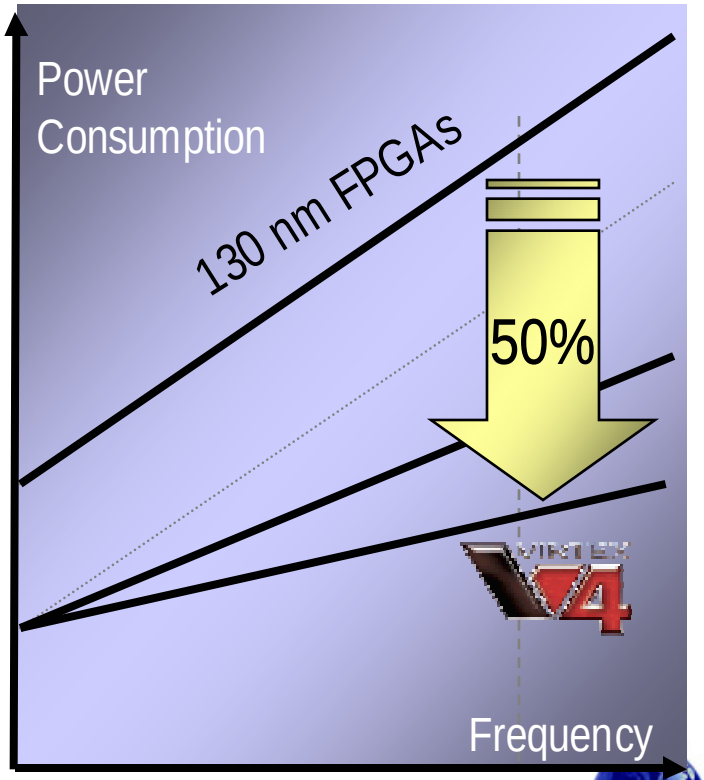


Virtex-4 Addresses Need for Lower Power Consumption

Customer challenges
- Static power (leakage) grows exponentially with process generations
- Dynamic power grows with frequency ($P = cv^2f$)

Virtex-4 cuts power by >50%

- 40% lower static power with Triple-Oxide technology
- 50% lower dynamic power through process shrink
- Up to 10x lower dynamic power with integrated IP



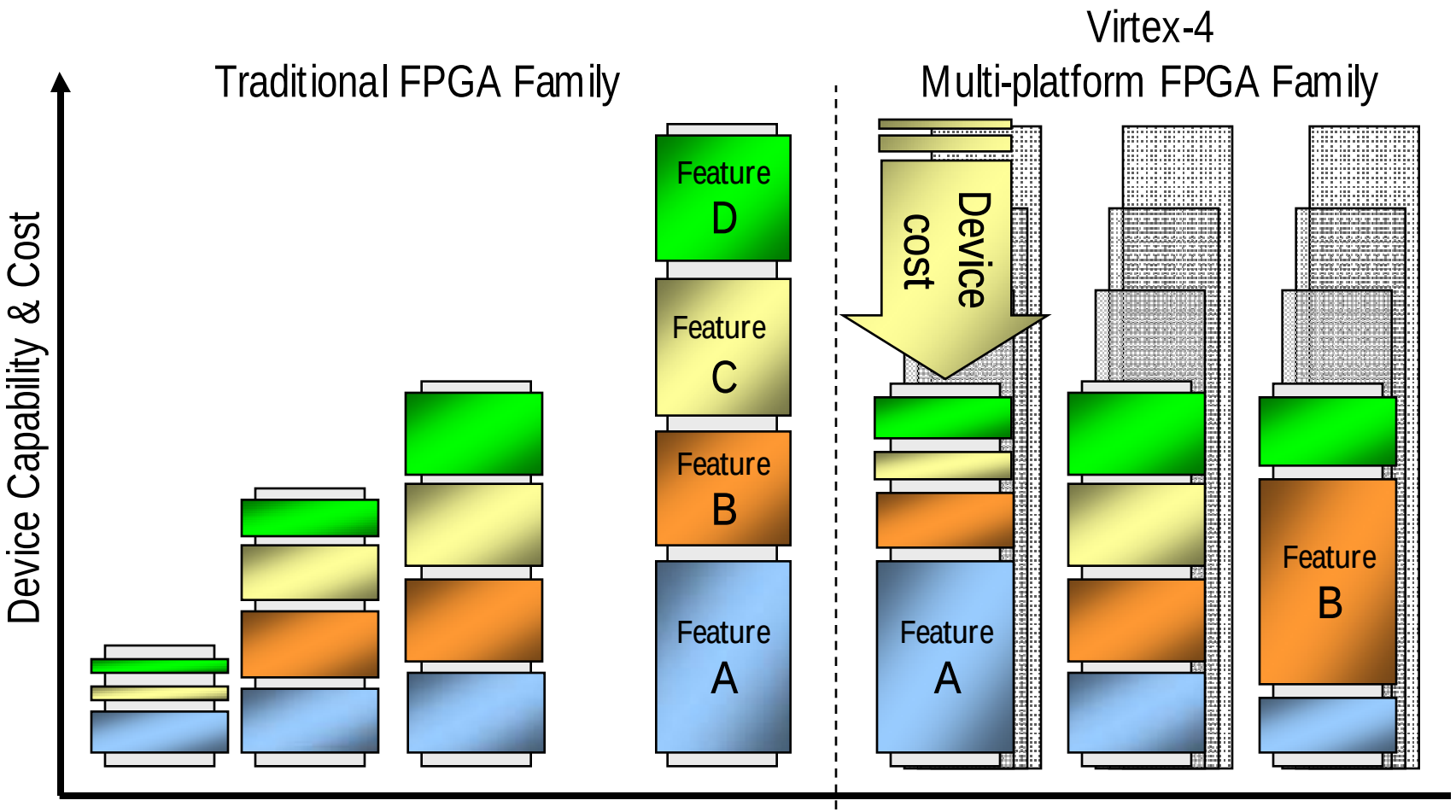
Virtex-4 Addresses Need for Lowest System Cost

Customer challenge
- Integrate more functionality while providing a generic programmable platform

Virtex-4 lowers system cost by 2x - 10x

- Advanced 90 nm/300 mm cuts device cost by 50%
- Multi-platform offering can reduce cost by up to 10X
- Wealth of integrated IP lowers FPGA cost & board BOM
- EasyPath further lowers system cost by up to 80%

Multi-Platform Offering Can Reduce Cost By Up To 10X



Enabled by the breakthrough ASMBL™ architecture

Wealth of Integrated IP Lowers FPGA Cost & Board BOM

- Block RAM with built-in FIFO control logic
- SelectIO with built-in synchronization logic
- Integrated clock management circuitry
- Serial transceivers with integrated equalization
- XtremeDSP slice with integrated MAC
- Integrated 10/100/1000 Ethernet MAC

EasyPath Further Lowers System Cost By Up To 80%

- Tested specifically for customer's design
- Identical in every way to the FPGA
- Fastest turnaround in the industry
- Reduces FPGA unit cost by 50-80 %

Virtex-4 Addresses Need for Simpler Interfacing Designs

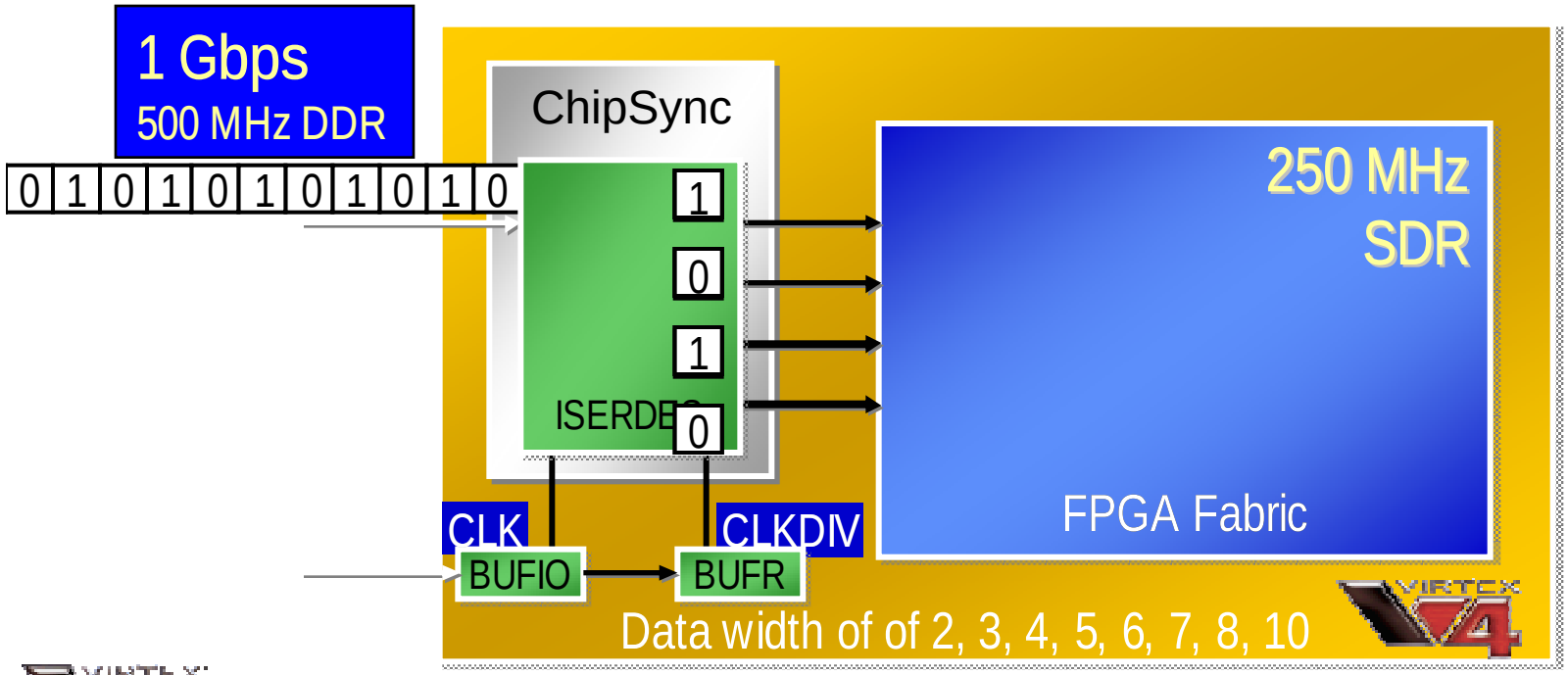
Customer challenges
- Very difficult to meet timing for high-speed source synchronous interfaces
- Synchronization of data/clock (data capture) for memory I/Fs such as DDR2, QDR II
- Finish design on time

Virtex-4 solves toughest design challenges

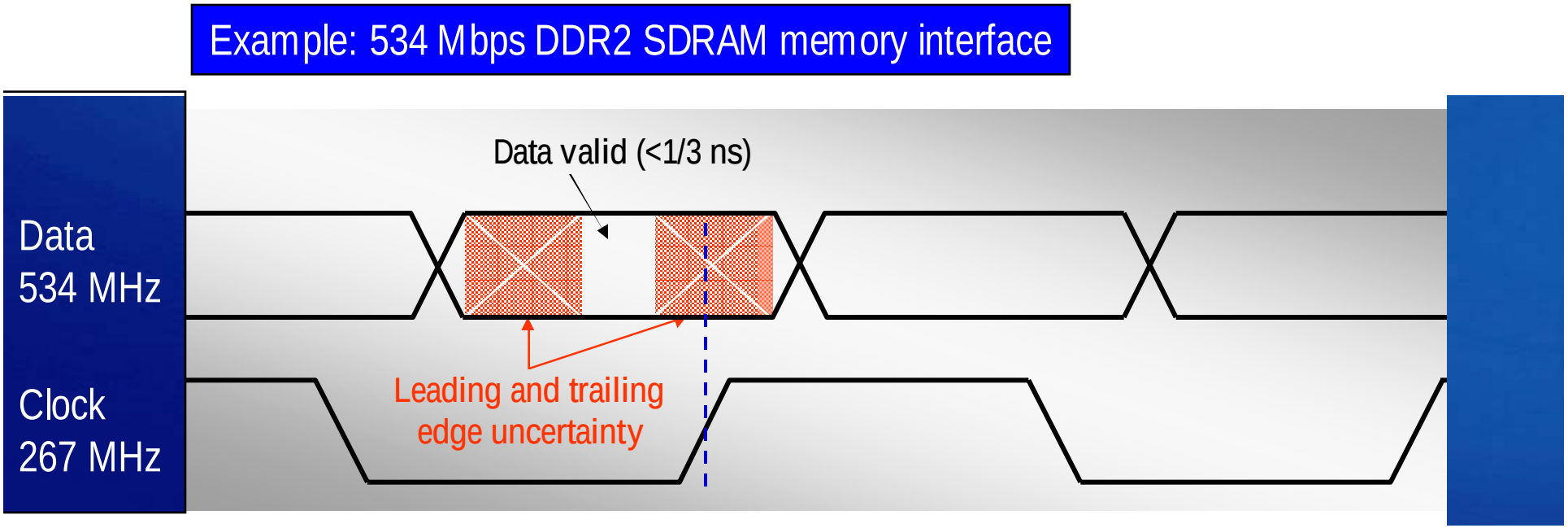
- Timing critical circuitry pre-built in silicon on every I/O
- Automatic synchronization of data and clock
- Easy-to-use toolkits available today

Timing Critical Circuitry Pre-Built in Silicon on Every I/O

- ChipSync™ technology automatically manages incoming data and frequency division



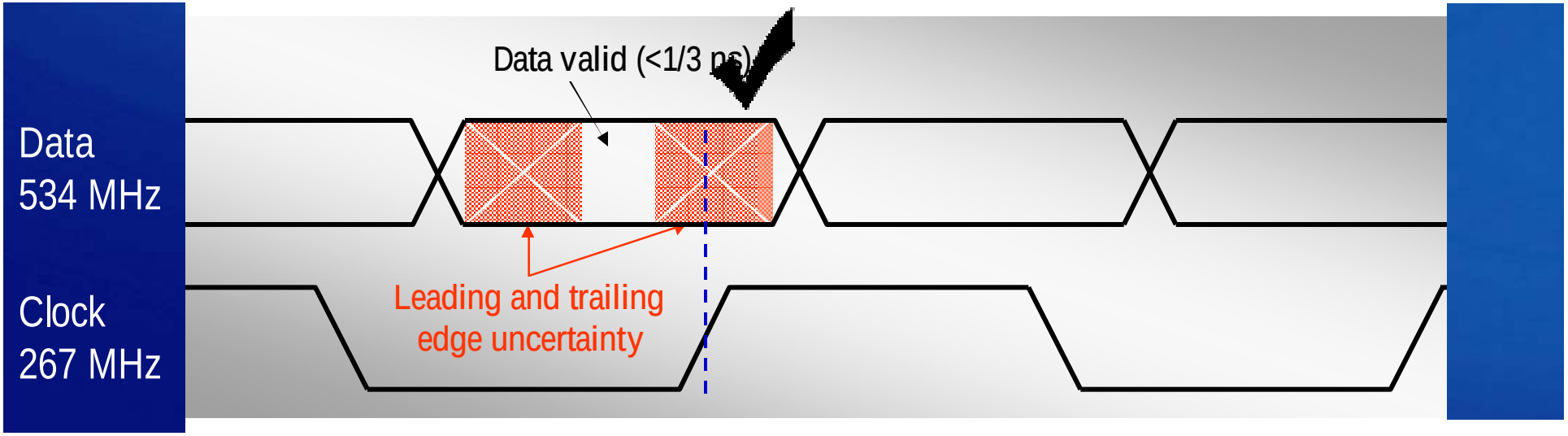
Automatic Synchronization of Data and Clock



Automatic Synchronization of Data and Clock

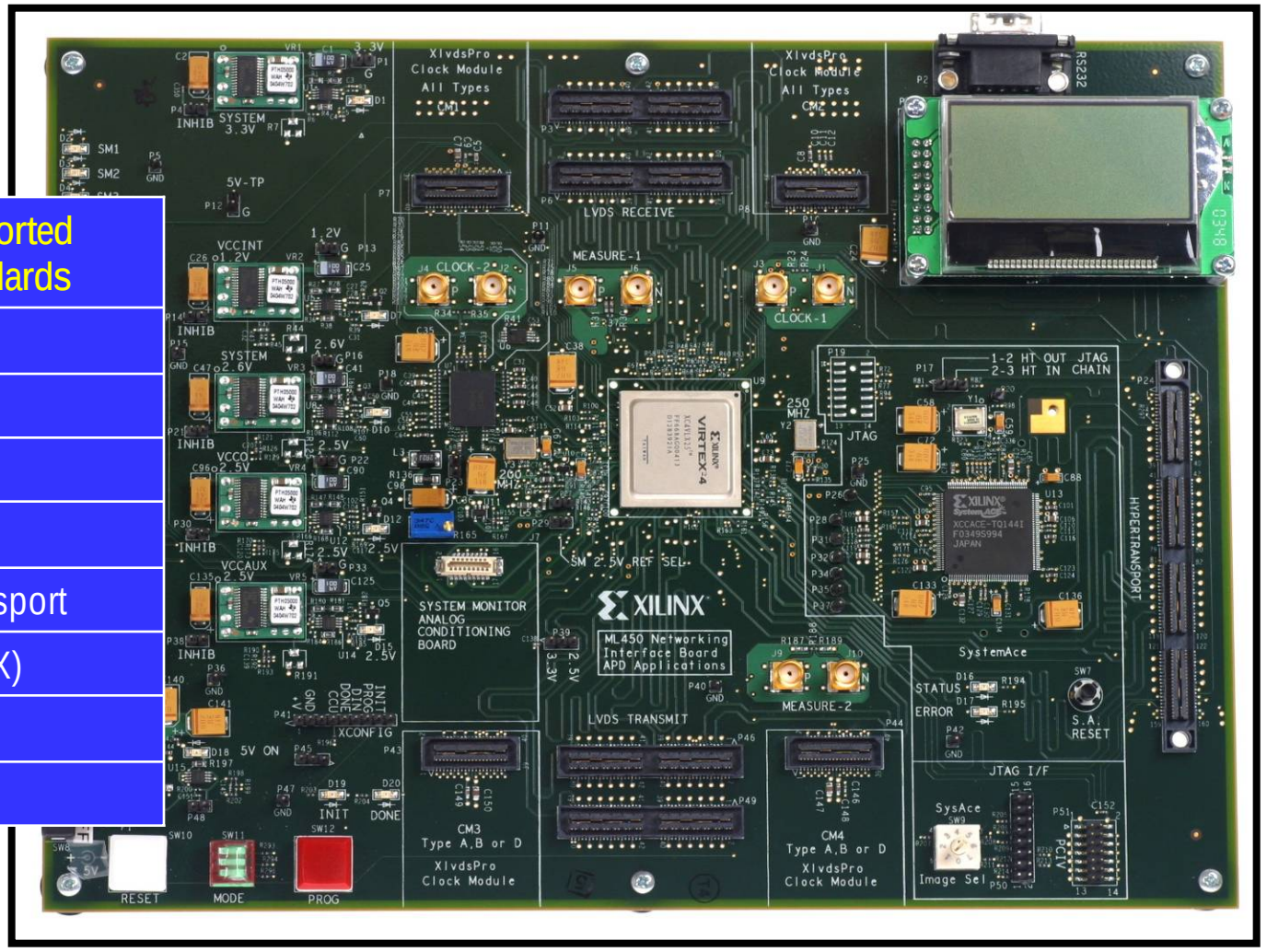
- ChipSync technology aligns data automatically
- Eliminates setup and hold time issues

Example: 534 Mbps DDR2 SDRAM memory interface



Easy-to-Use Source Synch I/F Toolkit Available Today

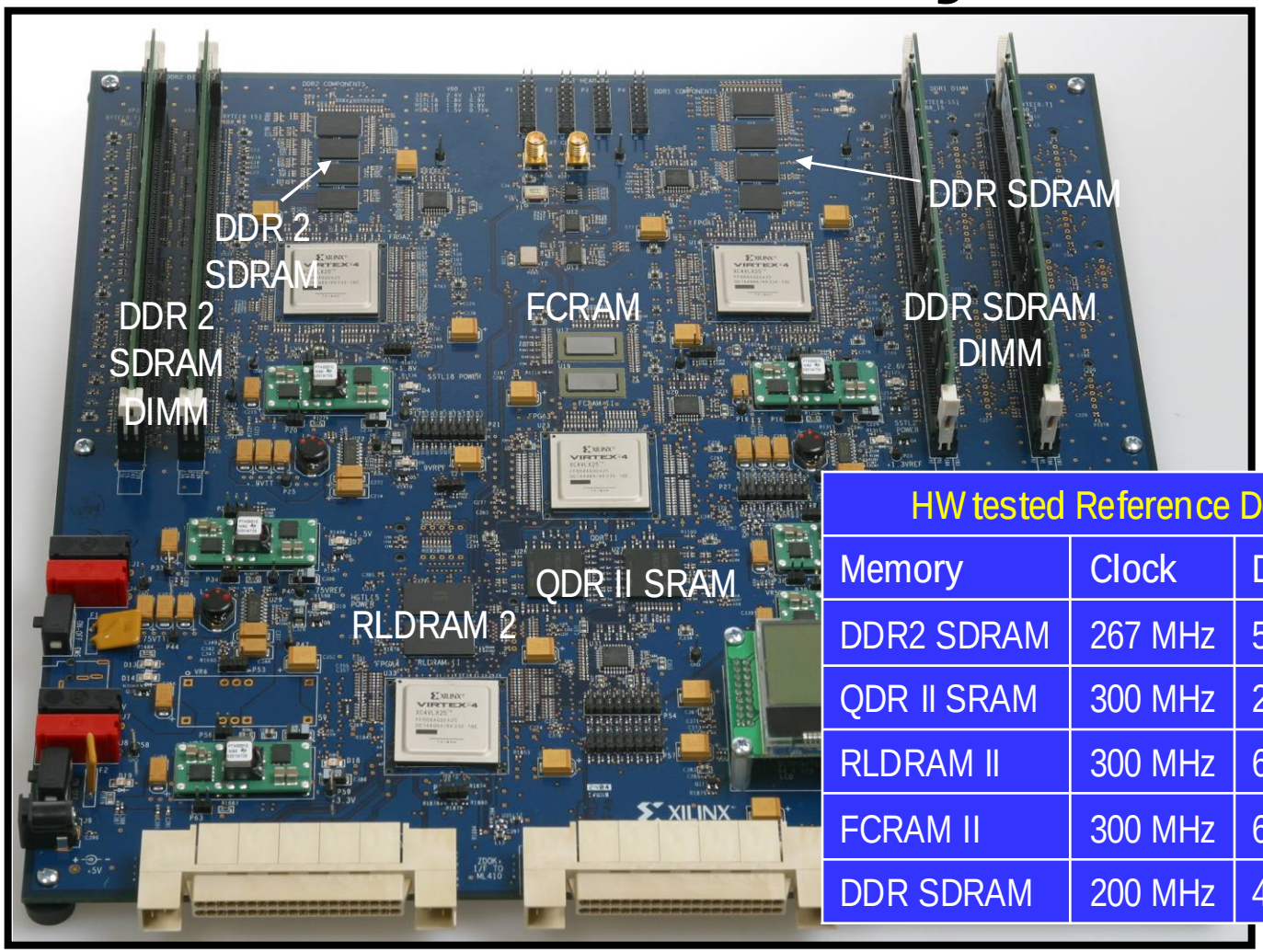
Supported Standards
SPI-4.2
SFI-4
XSBI
RapidIO
HyperTransport
NPSI (CSIX)
Utopia IV
GFP



Source Synchronous I/F Kit, ML450

Easy-to-Use Memory Toolkit Available Today

Memory Toolkit, ML461



HW tested Reference Designs		
Memory	Clock	Data rate
DDR2 SDRAM	267 MHz	534 Mbps
QDR II SRAM	300 MHz	2x600 Mbps
RLDRAM II	300 MHz	600 Mbps
FCRAM II	300 MHz	600 Mbps
DDR SDRAM	200 MHz	400 Mbps

ISE 6.3i for Virtex-4 Shipping Today

- Widens performance lead by up to 40%
  - Hierarchical design planning and timing closure with optional PlanAhead tool
- Makes design of Virtex-4 easy
  - Architecture wizards (e.g., ChipSync, XtremeDSP, RocketIO, DCMs…)
  - PACE for simultaneous switching output
  - ChipScope Pro debug and analysis
- Now supporting Enterprise 3.0 Linux low-cost OS platforms

Complete Virtex-4 Design Solutions Available Today

XtremeDSP Domain

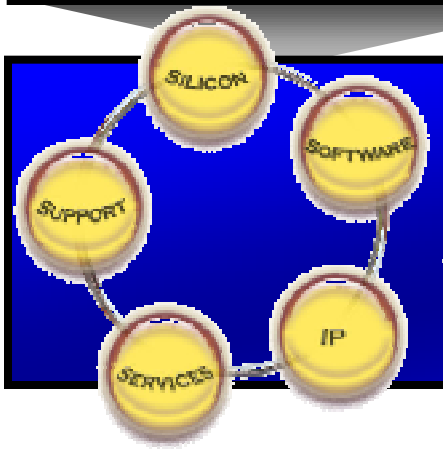
- System Generator for DSP
- DSP Cores/Algorithms

Connectivity Domain

- Connectivity IP
- Source Synch Design Kits

Processing Domain

- Platform Studio & EDK
- MicroBlaze processor
- Processing IP



- Front-to-back design flow
- LogiCORE IP
- Design Kits
- Reference Designs
- ChipScope Pro
- Third-party EDA
- Design Services
- Support
- Customer Education

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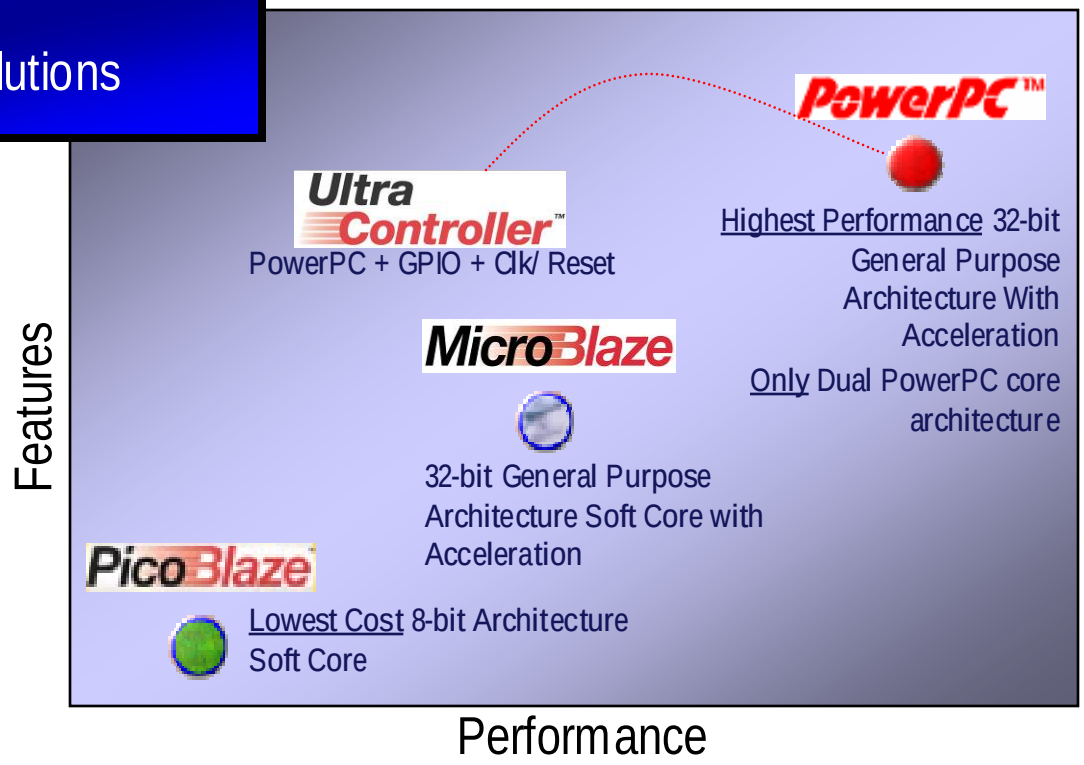
- High-performance DSP

The Most Complete Range of FPGA Embedded Solutions

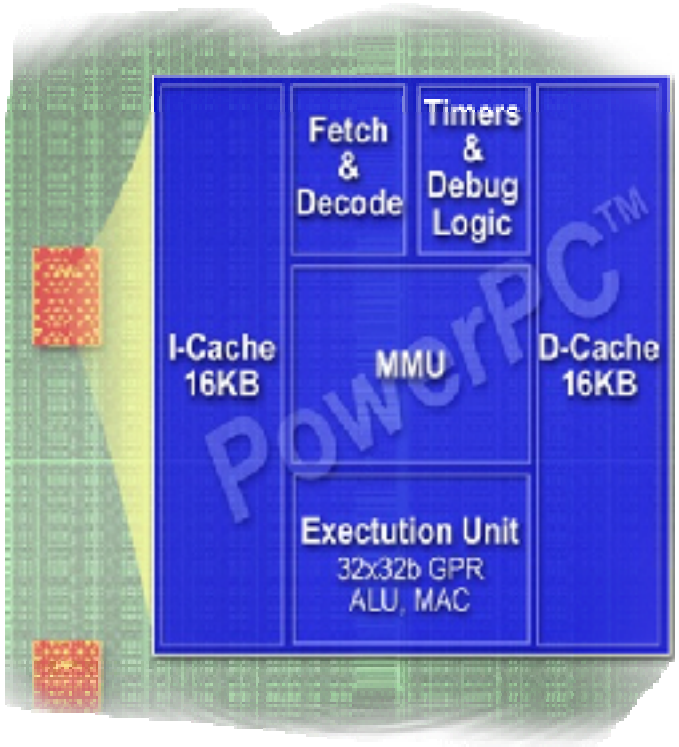
Customer Challenge
- Range of processing solutions



Plus: A broad range of common peripherals and IP

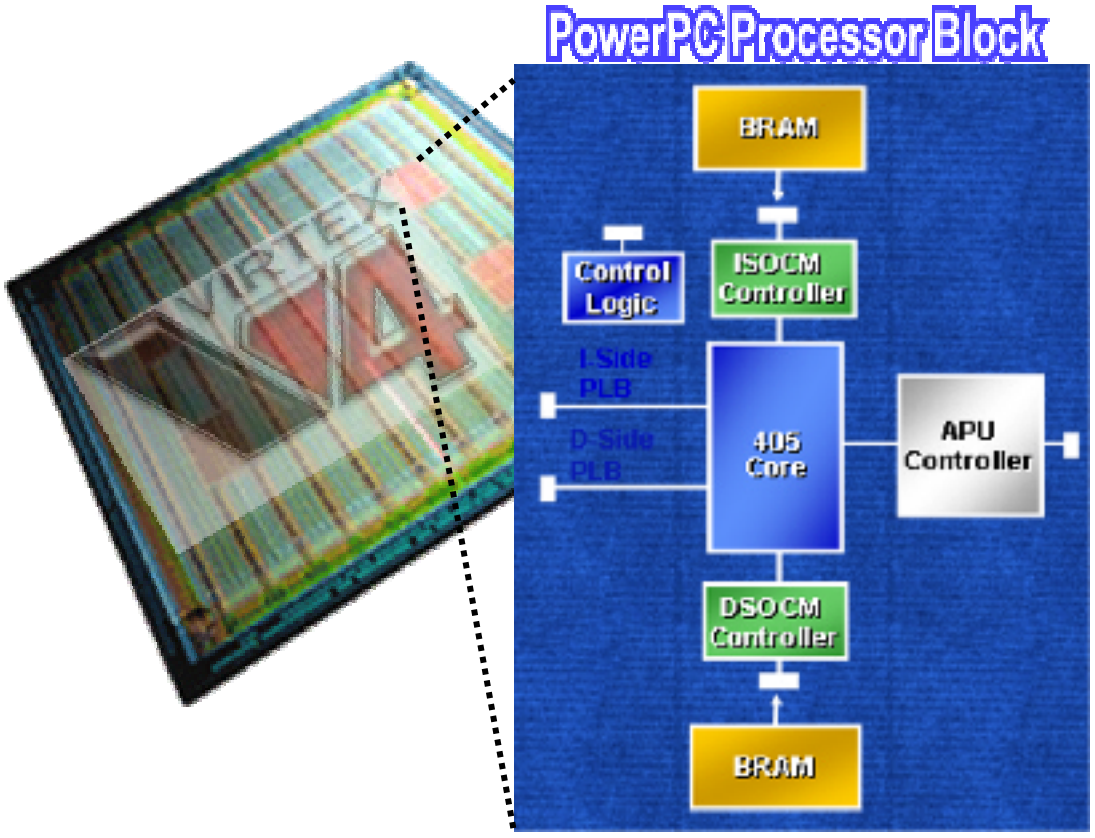
World's Highest Performance FPGA Processing Solution

Customer Challenge
- Performance



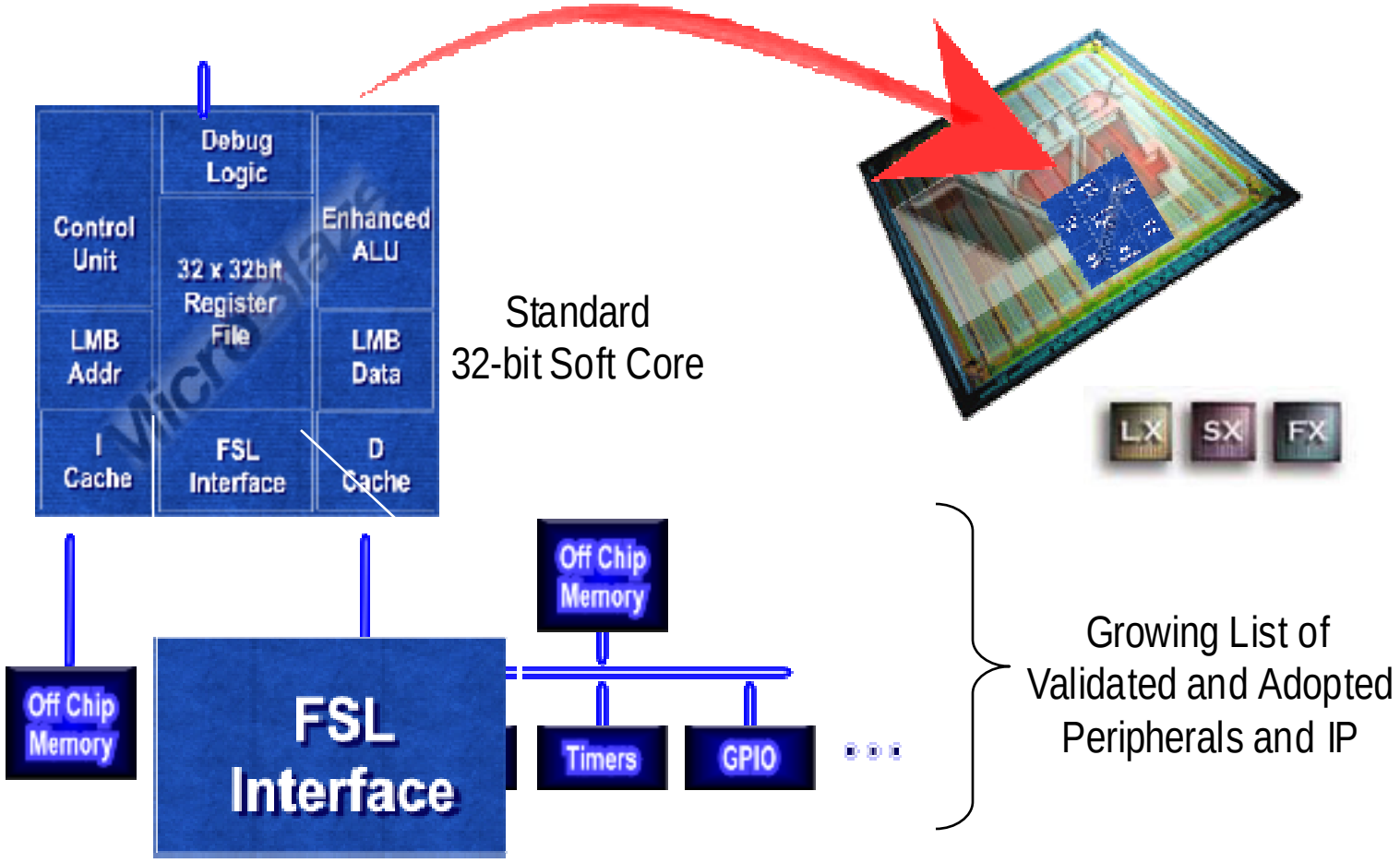
- *Highest Performance* FPGA embedded cores
  - 680 DMIPS@ 450MHz
  - *Dual* Cores
- 2nd Generation FPGA with PowerPC 405
  - Maintains HW and SW Investment
  - Enhanced bus interfaces

Accelerate Performance Beyond the Core



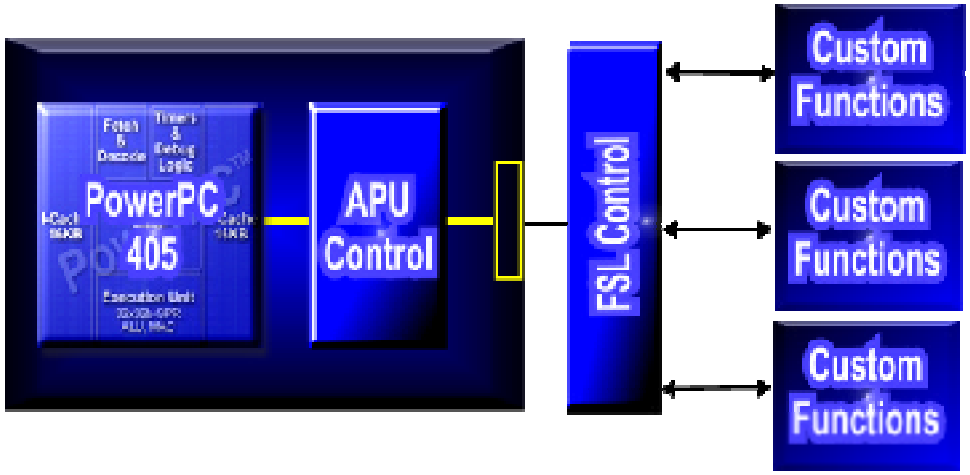
- New Auxiliary Processing Unit (APU)
  - Direct interface from CPU pipeline to FPGA logic
  - Simplifies integration of Coprocessor and hardware accelerators
- Reduce number of bus cycles by factor of 10X
- Increase performance by over 20X

Accelerate V-4 With MicroBlaze



Flexible Coprocessor Configuration

- Direct Connect with Xilinx FSL
  - Ease of Use
  - Common Interface
  - Complements MicroBlaze
- Configure with Xilinx Platform Studio



Industry's Most Complete Design Environment

Customer Challenge
- A Robust Design Environment

Processor Cores, IP and Silicon	Development Tools	Development Boards & Reference Designs	Services And OS Support

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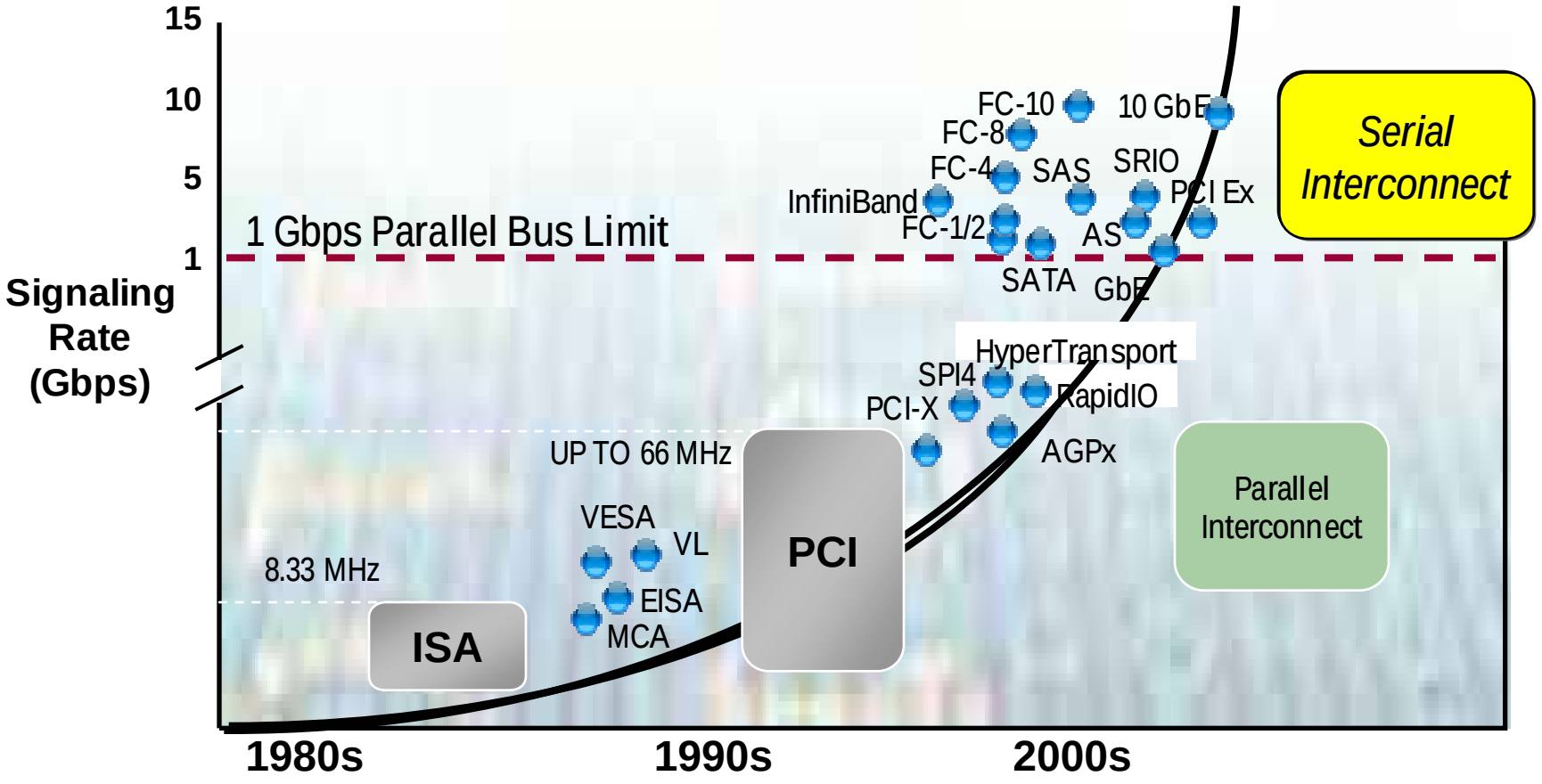
- High-performance DSP

Explosion of System Connectivity Standards



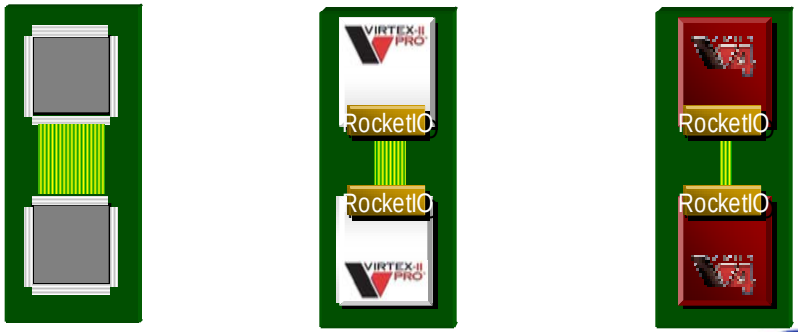
Source: Intel/Xilinx

Serial I/O Lowers PC Board Cost and Power Consumption

Customer challenges
- Reducing PC board and system cost
- Reduce power consumption for lower enclosure cost

Example: 10 Gbps aggregate bandwidth

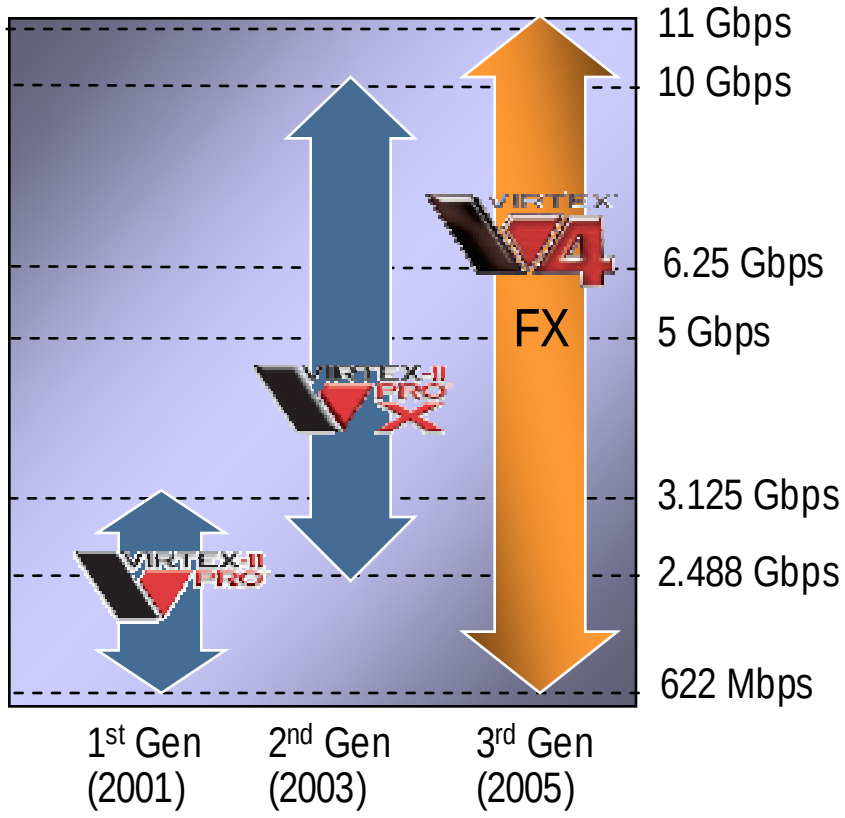
	Parallel 800Mbps DDR	Serial 3.125Gbps (4x 3.125Gbps)	Serial 10Gbps (1x 10Gbps)
Example PC Board Cost	$1150	$625	$250
Link Power Consumption	4W	2.8W	1.2W



Virtex-4 Meets Need for More and Scalable Bandwidth

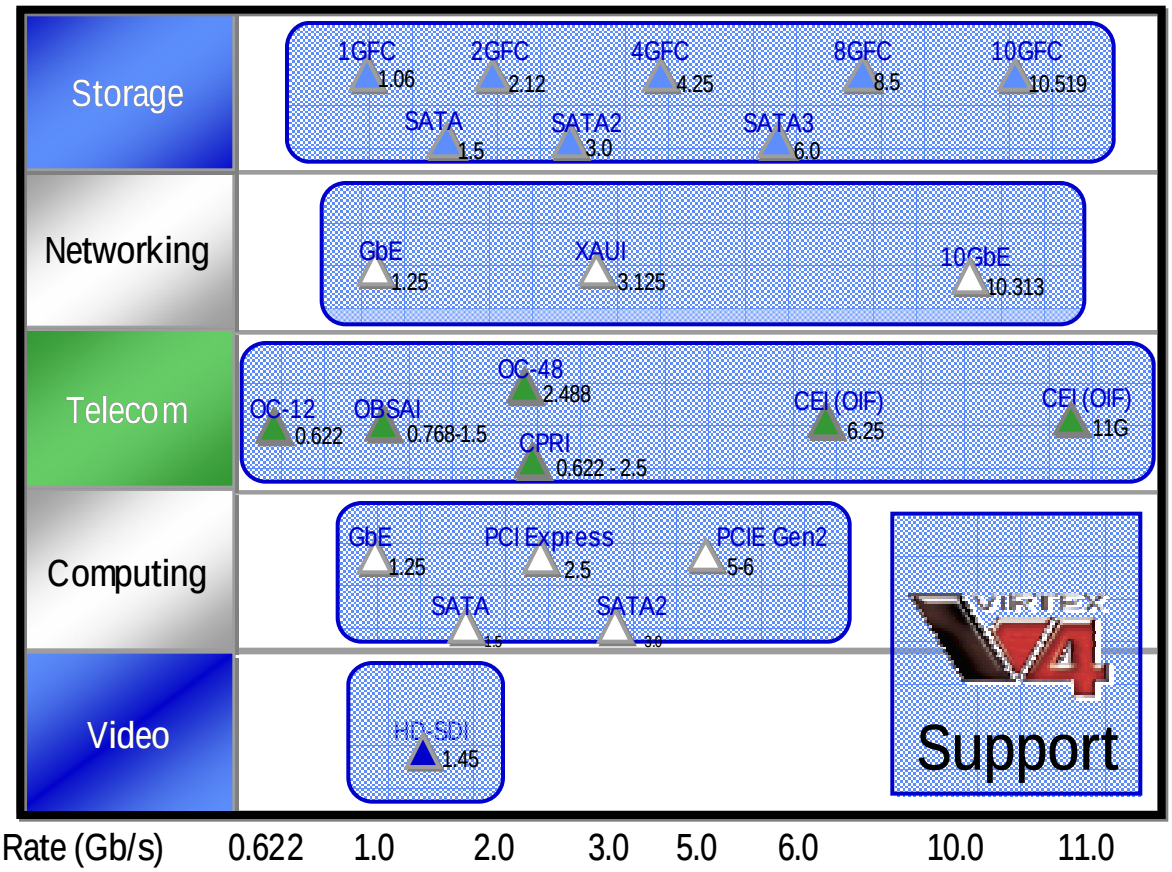
Customer challenges
- Supporting faster I/O standards
- Upgrading current and future systems
- Interfacing to multiple standards with different speed

- Only platform with 622Mbps to 11.1Gbps transceivers
- Proven third generation serial I/O technology from Xilinx



Virtex-4 Meets Need for Multiple Standards Compliance

Customer challenges
- Plethora of interfacing protocols
- Differing electrical compliance requirements
- Bridging between parallel and serial devices

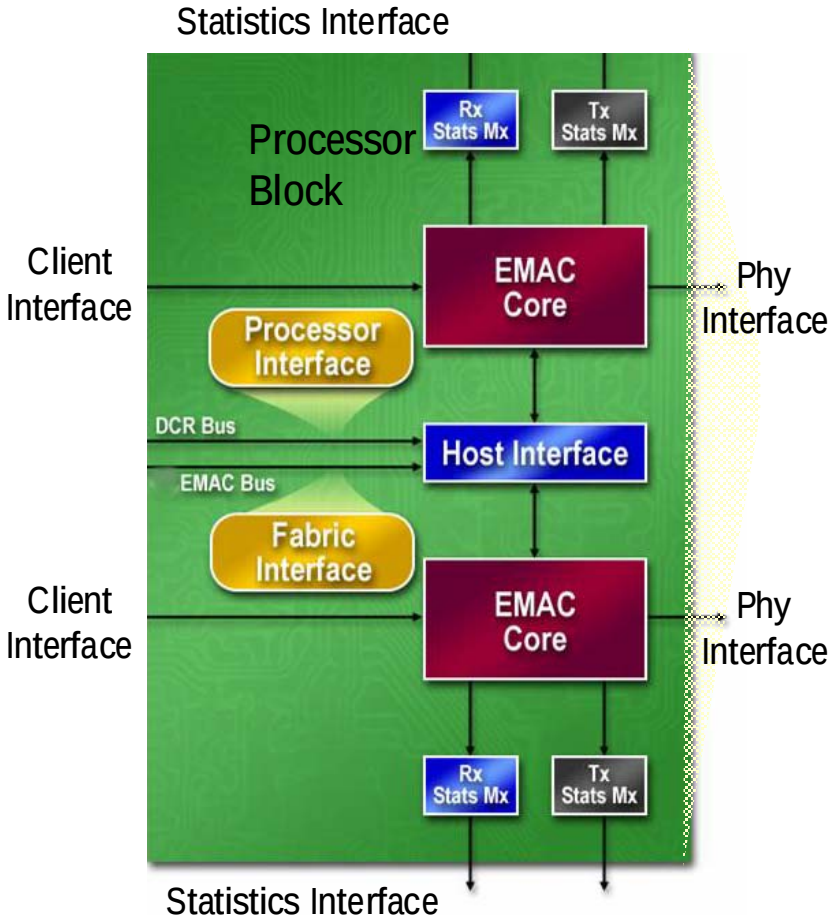


Most Flexible Support for All Popular Protocols

Integrated Tri-Mode EMAC Lowers Cost of Connectivity

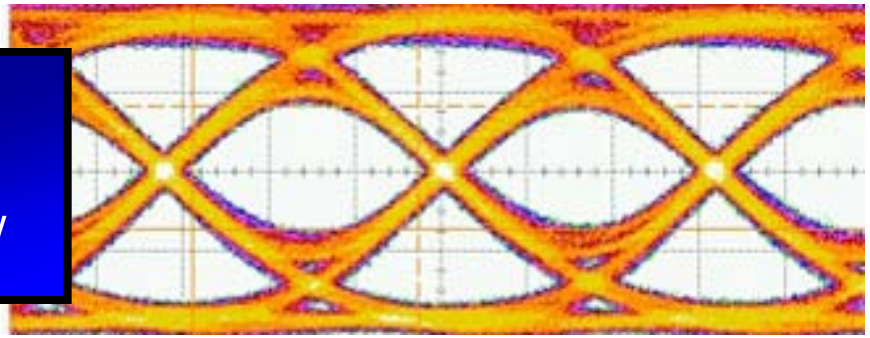
Customer challenge
- Connecting FPGAs to ASIC/ASSPs without consuming logic resources

- Industry's first integrated 10/100/1000 Ethernet MAC
  - Up to 4 EMACs in FX devices



Signal Integrity Solved with Built-in Equalization

Customer challenge
- Mitigate channel loss to improve throughput and ensure signal integrity



- Virtex-4 provides advanced channel equalization techniques for improving signal integrity
- Transmit Pre-emphasis
  - Equalizes lossy channels by modifying transmit signal
  - Required for channels up to 3.125 Gbps
- Receive Equalization
  - Receive equalization techniques (1st FPGA with Linear and DFE)
  - Optimizes receive signal and opens the data eye
  - Required for upgrading legacy backplanes and channels upwards of 5 Gbps

Agenda

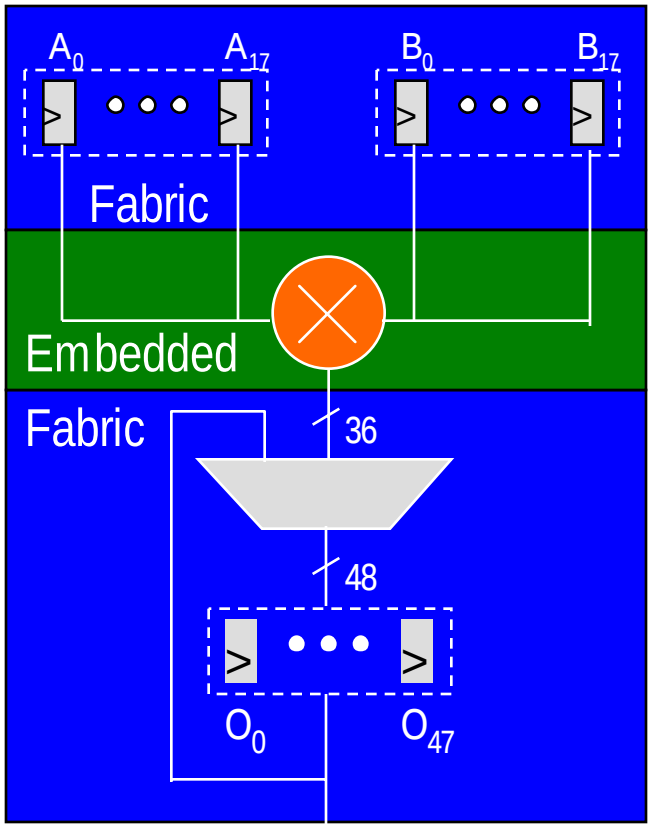
- Introduction
- High-performance FPGA design
- Embedded processing
- High-speed serial connectivity
- High-performance DSP

Virtex-4 Meets Need for Higher DSP Performance

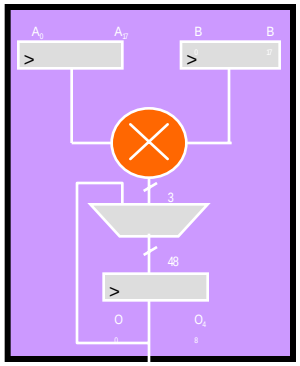
Customer challenges
- Designing highly parallel systems to improve channel performance and cost
- Achieving performance without manual hand-tuning (e.g., insert pipelining)

- Virtex-4 – world's fastest FPGA for DSP
  - New XtremeDSP Slice Delivers 2x Performance in less than 1/10th the Area
  - The SX Platform is the Highest DSP Performance FPGA Ever

New XtremeDSP Slice Delivers 2x Performance in 1/10th the Area

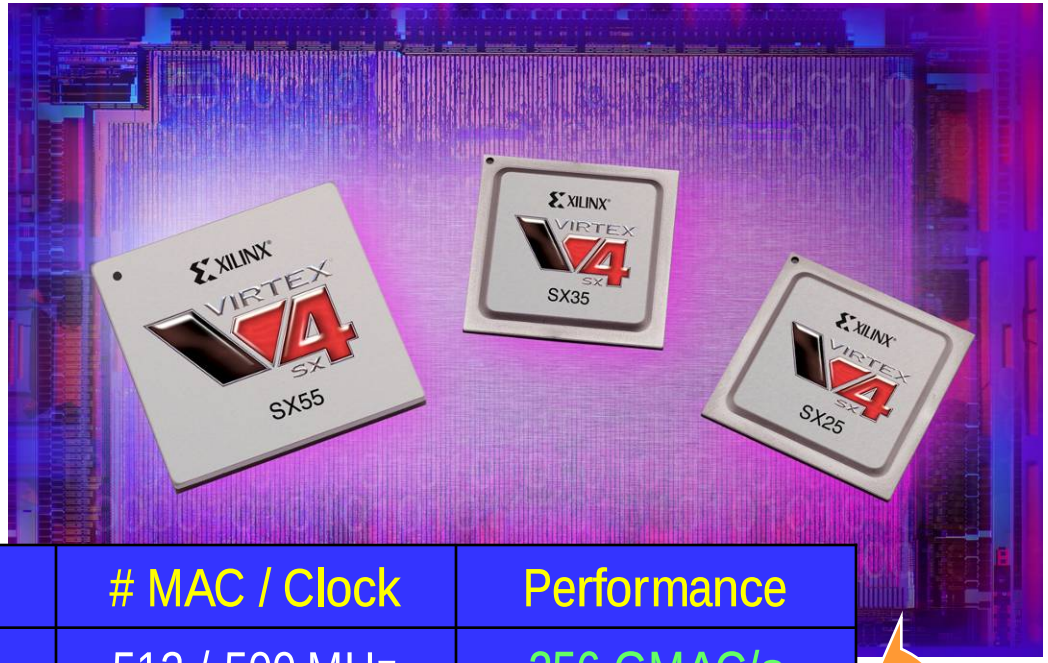


- Previous generation FPGAs @ 250MHz



- Virtex-4 XtremeDSP Slice @ 500MHz
  - 18x18 multiplier
  - 48-bit accumulator
- Integrated MAC
  - 2x performance advantage
  - 1/10 the power
  - 1/7 the area

The SX Platform is the Highest DSP Performance FPGA Ever



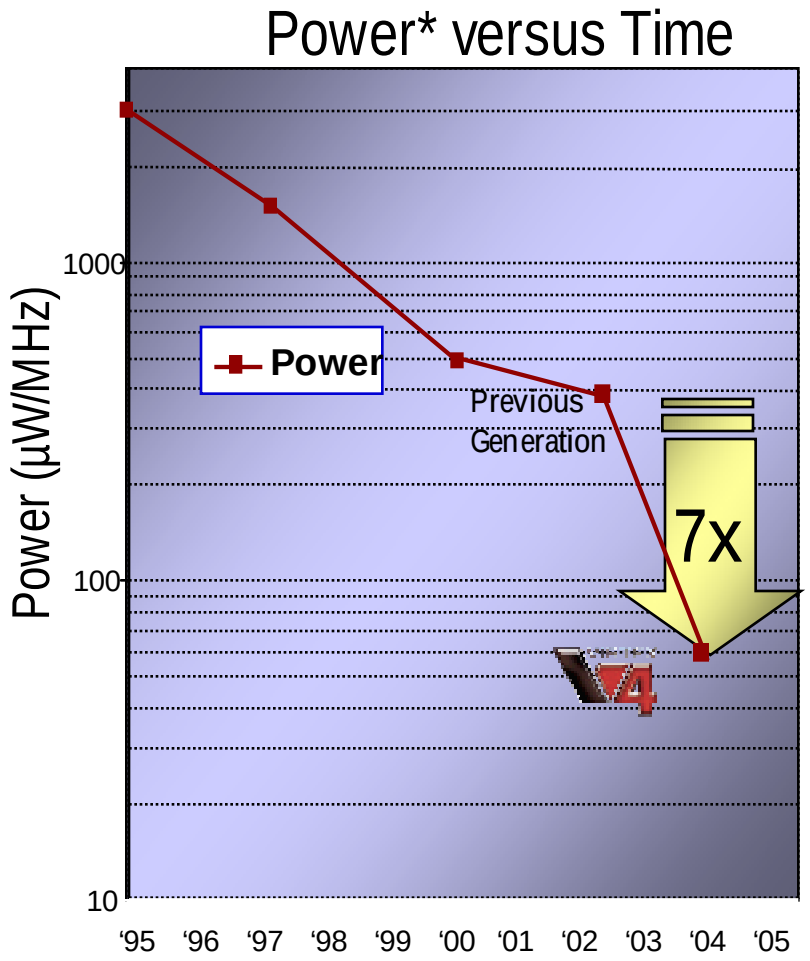
Device	# MAC / Clock	Performance
4VSX55	512 / 500 MHz	256 GMAC/s
4VSX35	192 / 500 MHz	96 GMAC/s
4VSX25	128 / 500 MHz	64 GMAC/s
Previous generation	444 / 250 MHz	111 GMAC/s

>2x

Virtex-4 SX Addresses Need for Lower Power

Customer challenge
- Achieve lower power per channel for infrastructure

- Virtex-4 significantly reduces power
  - XtremeDSP Slice Lowers DSP Power by 7x

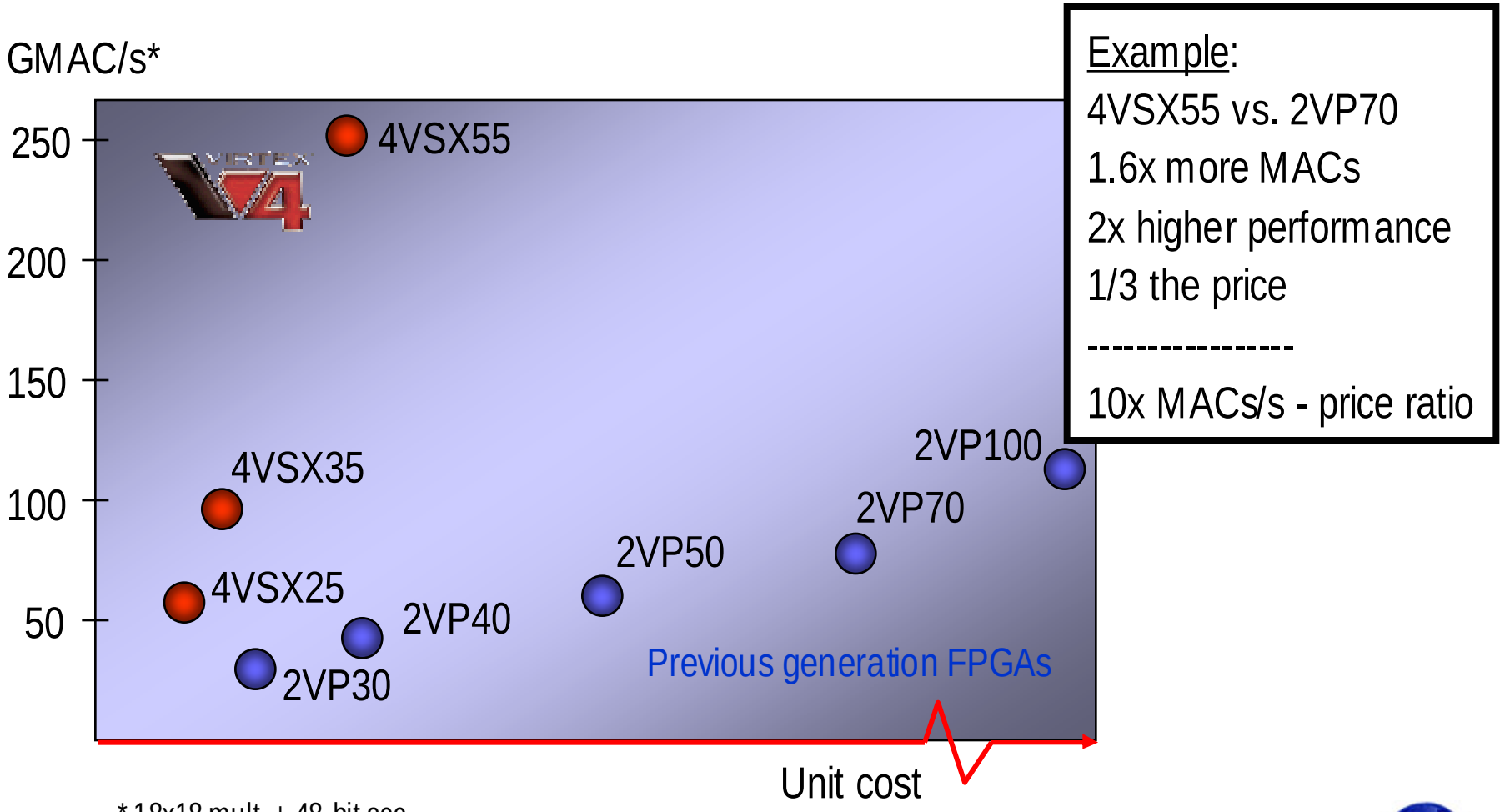


Virtex-4 Meets Need for High-performance DSP at Low-Cost

Customer challenges
- Avoid risky and expensive switch to ASIC
- Meet requirements on cost sensitive high-performance DSP applications (e.g. JTRS)

- Virtex-4 – breakthrough in DSP performance per dollar
  - SX Provides Up to 10x Higher MACs/s - Price Ratio

SX Provides Up to 10x Higher MACs/s - Price Ratio



* 18x18 mult. + 48-bit acc.

Complete DSP Design Solution

Applications Expertise	New DSP division, partnerships
DSP Services	Design Services, education & support
Design/Verification Tools	System Generator for DSP
DSP Algorithms	Filters, Forward Error Correction…
Silicon	Optimized programmable FPGA platforms

Summary

- Up to 2x faster – world's fastest FPGA
  - 500 MHz clocks, >1Gbps LVDS, 11.1 Gbps transceivers
- 2x more capacity - world's highest capacity FPGA
  - 200,000 logic cells, integrated IP blocks
- 2x – 10x lower cost – industry's lowest system cost
  - ½ price for same functionality, up to 10x better performance/price ratio
- 2x lower power– industry's lowest power/performance
  - 40% static power, 50% dynamic power
- Easiest-to-use design solutions
  - Easy source synchronous and memory interfacing

Appendix

Virtex-4 LX Family

			4VLX15	4VLX25	4VLX40	4VLX60	4VLX80	4VLX100	4VLX160	4VLX200
Logic Cells			13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448
BRAM Blocks			48	72	96	160	200	240	288	336
Block RAM Kbits			864	1,296	1,728	2,880	3,600	4,320	5,184	6,048
DCMs			4	8	8	8	12	12	12	12
DSP Slices			32	48	64	64	80	96	96	96
System Monitors			0	1	1	1	1	1	1	1
Max Select IO			320	448	640	640	768	960	960	960
Total IO Banks			9	11	13	13	15	17	17	17
Package	**Size**	**IO**								
SF363	17	240	240	240						
FF668	27	448	320	448	448	448				
FF1148	35	768			640	640	768	768	768	
FF1513	40	960						960	960	960

X	**X** = IO capacity

Virtex-4 FX Family

				4VFX12	4VFX20	4VFX40	4VFX60	4VFX100	4VFX140
			Logic Cells	12,312	19,224	41,904	56,880	94,896	142,128
			BRAM Blocks	36	68	144	232	376	552
			Block RAM Kbits	648	1,224	2,592	4,176	6,768	9,936
			DCMs	4	4	8	12	12	20
			DSP Slices	32	32	48	128	160	192
			System Monitors	0	0	1	1	1	1
			Max Select IO	320	320	448	576	768	896
			Total IO Banks	9	9	11	13	15	17
			Processors	1	1	2	2	2	2
			EMACs	2	2	4	4	4	4
			MGTs	0	8	12	16	20	24
Package	**Size**	**MGT**	**IO**						
SF363	17	0	240	240					
FF668	27	0	448	320					
FF672	27	12	352		(8) 320	(12) 352	(12) 352		
FF1152	35	20	576			(12) 448	(16) 576	(20) 576	
FF1517	40	24	768					(20) 768	(24) 768
FF1760	42.5	28	896						(24) 896

(Y) X	**Y** = MGT Channels and **X** = IO capacity

Virtex-4 SX Family

			4VSX25	4VSX35	4VSX55
Logic Cells			23,040	34,560	55,296
BRAM Blocks			128	192	320
Block RAM Kbits			2,304	3,456	5,760
DCMs			4	8	8
DSP Slices			128	192	512
System Monitors			0	1	1
Max Select IO			320	448	640
Total IO Banks			9	11	13
Package	**Size**	**IO**			
FF668	**27**	**448**	**320**	**448**	
FF1148	**35**	**768**			**640**

X	**X** = IO capacity