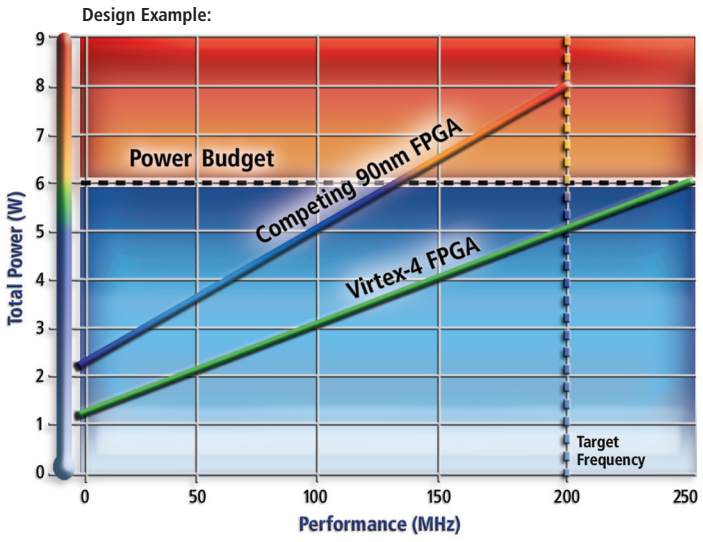
ED-low power ad 3/17/05 5:00 PM Page 1

With Competing FPGAs, Power Has Become a Burning Issue.

Design Example:



Design Example: LX60 vs. 2S60. Target Frequency = 200 MHz. Worst-case process.
20K LUTs, 20K Flip-Flops, 1Mbit On-Chip RAM, 64 DSP Blocks, 128 2.5V I/Os
Based on Xilinx tool v4.0 and competitor tool v2.1
For higher density devices, achieve up to 5W lower power

Get 1-5W lower power per FPGA, only with the Virtex-4 family

Check the specs for yourself at realistic operating temperatures (T_j = 85°C). Different logic architecture or dielectric just won't do it. No competing FPGA comes close to Virtex-4 for total power savings:

- **73% lower static power**
- **Up to 86% lower dynamic power**
- **94% lower inrush current (Take it to the lab and see!)**

Unique Triple-Oxide Technology & Embedded IP

At the 90nm technology node, power is the next big challenge for system level designers. An inferior device can suffer leakage, dramatic surges in static power, and thermal runaway. That's why we designed our Virtex-4 FPGAs with Triple-Oxide Technology™, embedded IP, and power-saving configuration circuitry. Now you can meet your performance goals, while staying within the power budget.

Visit ***www.xilinx.com/virtex4/lowpower*** today, and get the right solution on board before your power issues start heating up.

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