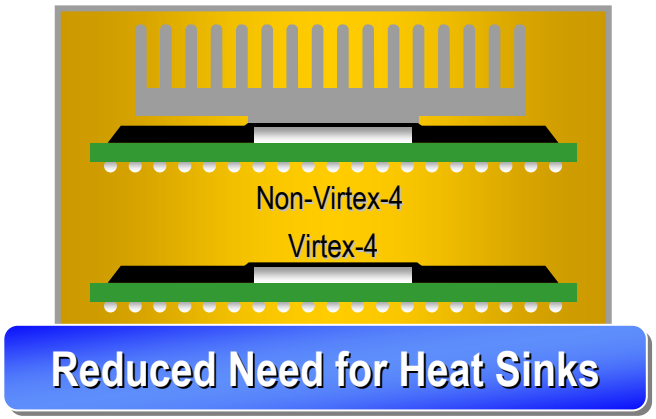
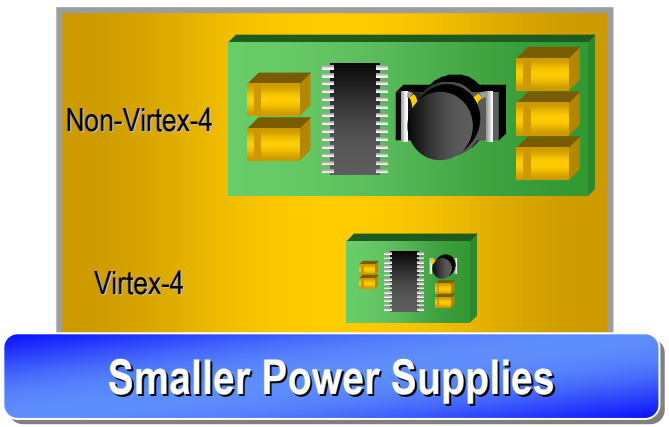
Virtex™-4 Low Power Advantage

Overview

- Why is reduced power important?
- Virtex™-4: 1 to 5 Watts lower total power per FPGA
  - 73% lower static power with exclusive triple-oxide technology
  - Up to 86% lower dynamic power with embedded hard IP
- Meet total power budget & target performance
- Tools for power estimation and analysis

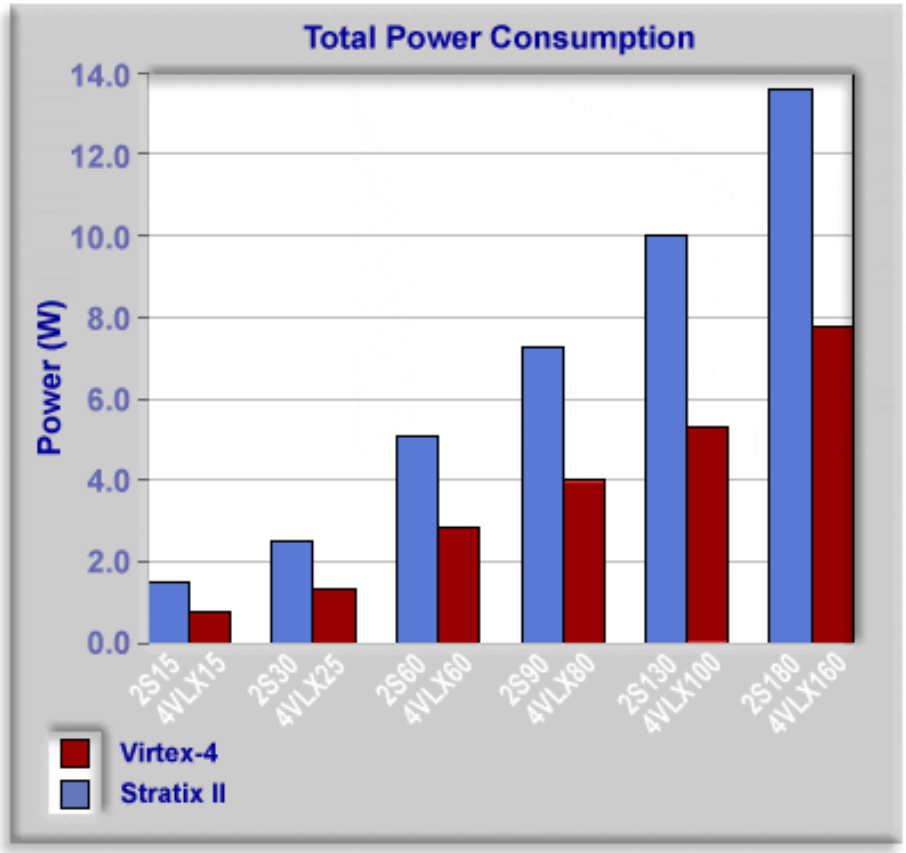
Why is Reduced Power Important?





- Reduced thermal concerns
  - Smaller no heat sinks needed
  - Simpler system thermal design (airflow, fans)
- Easier power supply design
  - Smaller supply circuitry
  - Reduced components
  - Less PCB space
- Lower cost power system
  - High-end power supplies cost from $0.50-$1.00/Watt
- Higher system reliability

1 to 5 Watts Lower Power/FPGA

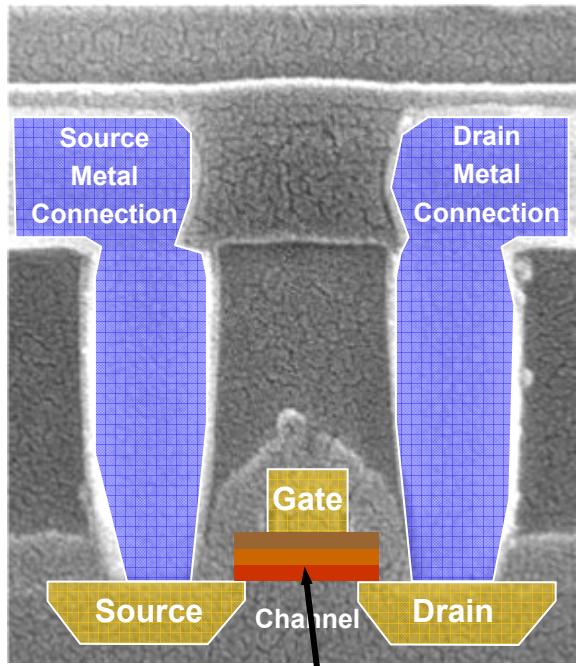


Design Details – Logic & Memory
Static power at Tj=85°C
Dynamic power at 200MHz - 50% of LUTs & FFs in Virtex-4 device; equivalent ALUTS & FFs in corresponding Stratix II device. 12.5% toggle rate - All M4K blocks used in Stratix II; equivalent 18Kb Block RAM in corresponding Virtex-4 device

Using abundant Virtex-4 hard IP reduces power further!

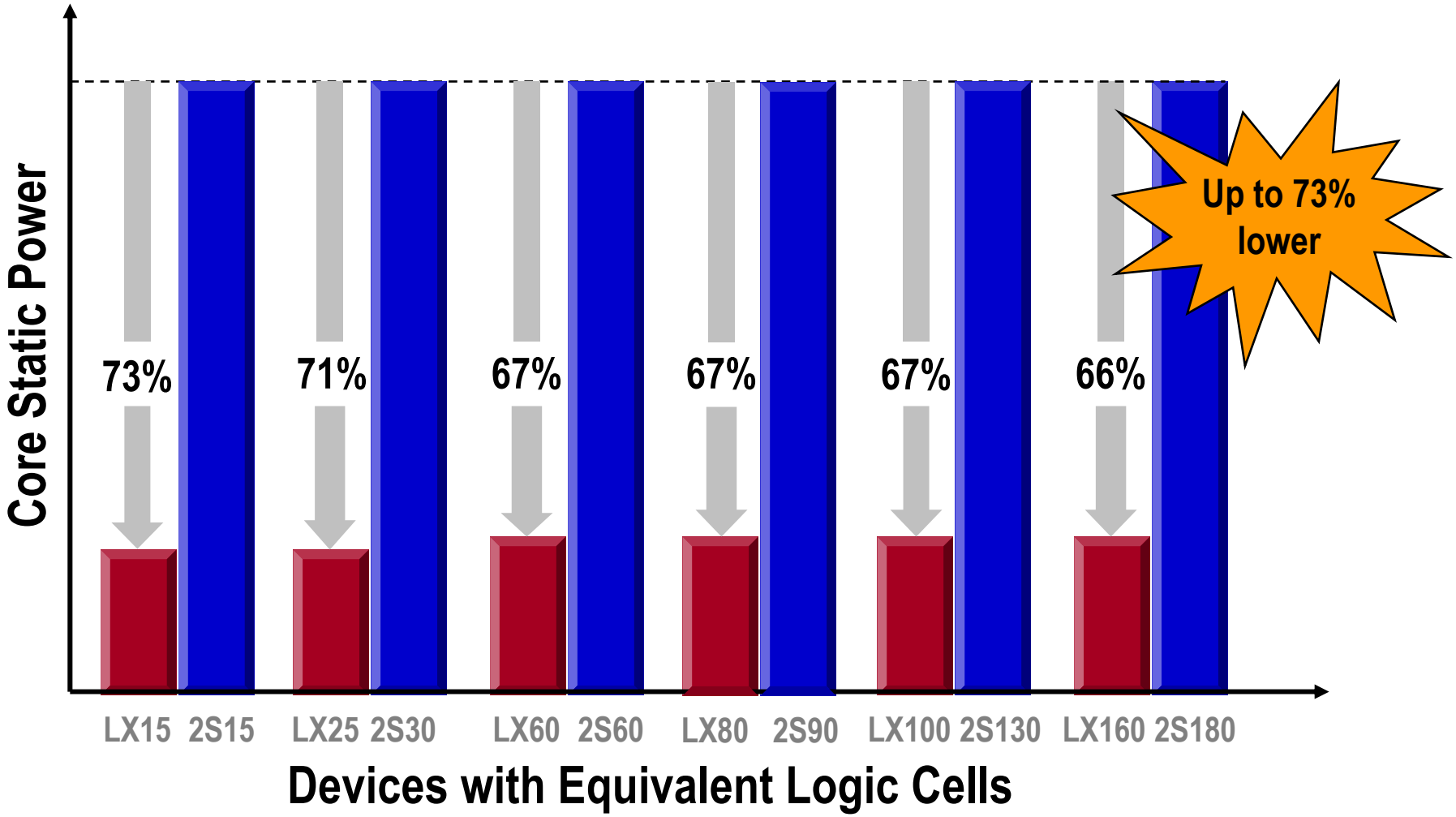
Exclusive Triple-Oxide Technology = Lower Static Power

- Law of physics: Leakage current increases as channel length and gate oxide thickness decrease
- Two oxide thicknesses are commonly used in the industry
  - Thin oxide in the fast core logic
  - Thick oxide in the versatile I/O
- Virtex-4 adds a third medium thickness oxide to **reduce** leakage current without compromising performance



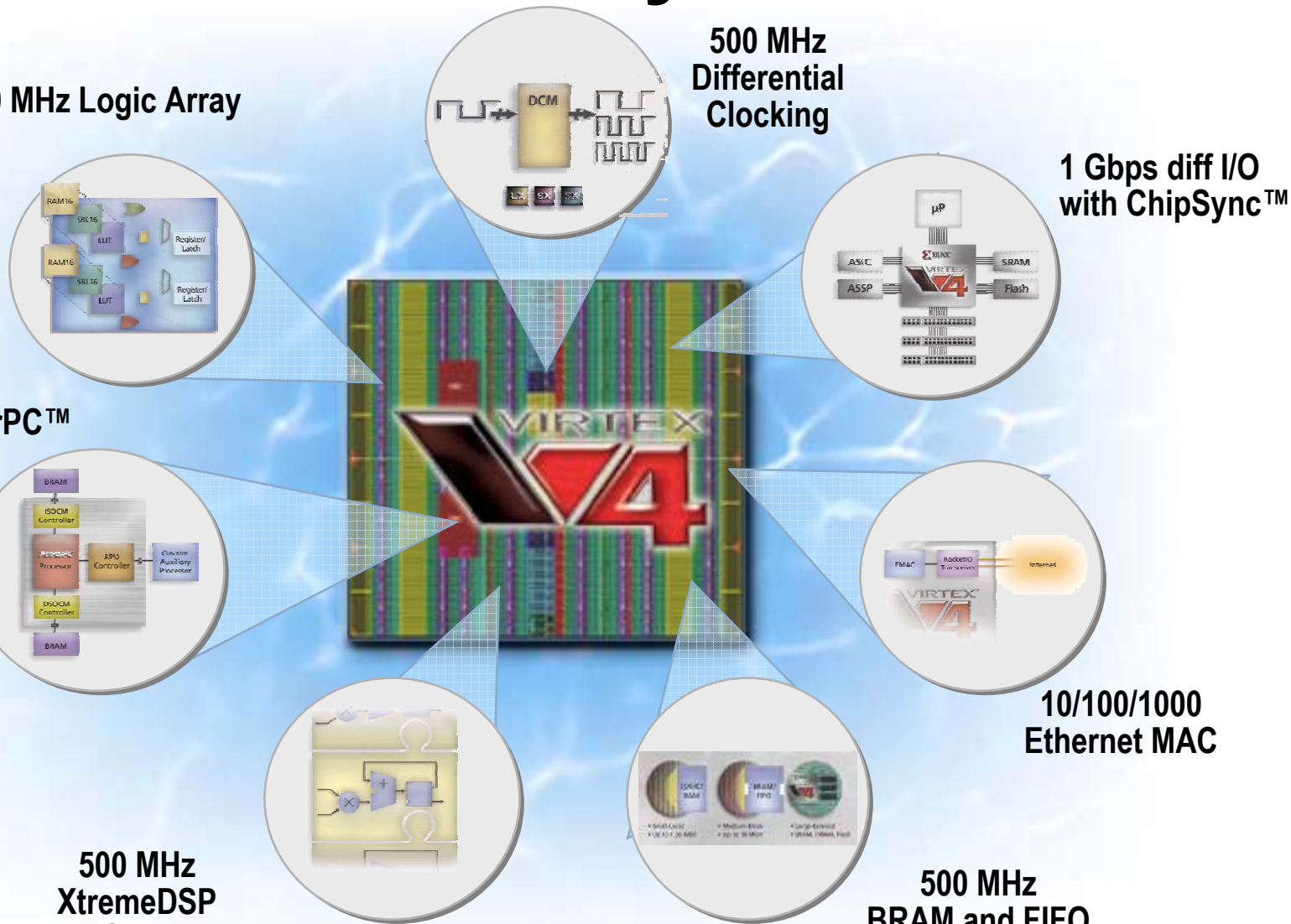
Only Xilinx FPGAs benefit from this technology

73% Less Static Power

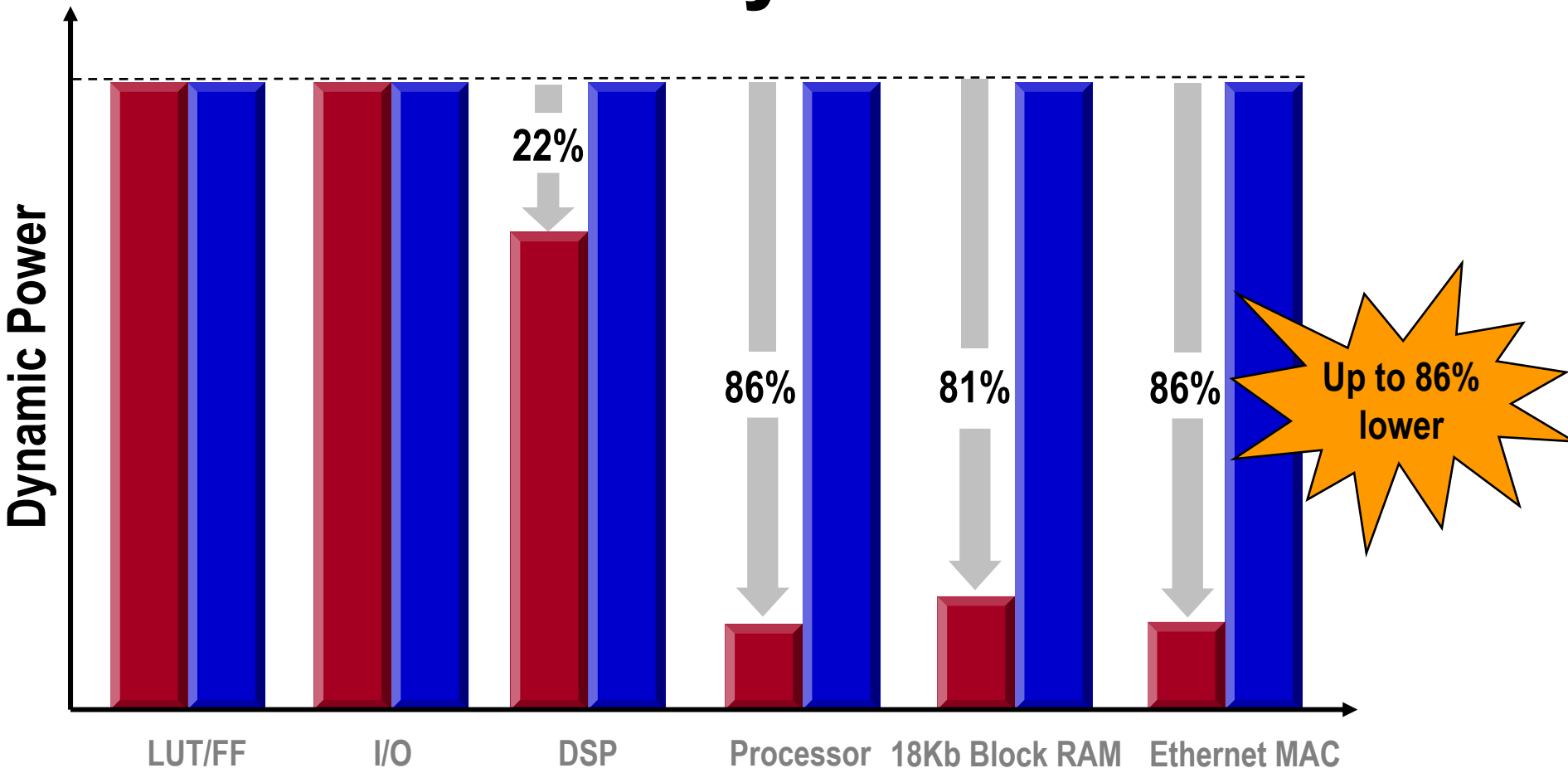


Xilinx WPTv4.1 vs. Stratix II PowerPlay v2.1, Tj=85°C

Hard IP = Lower Dynamic Power

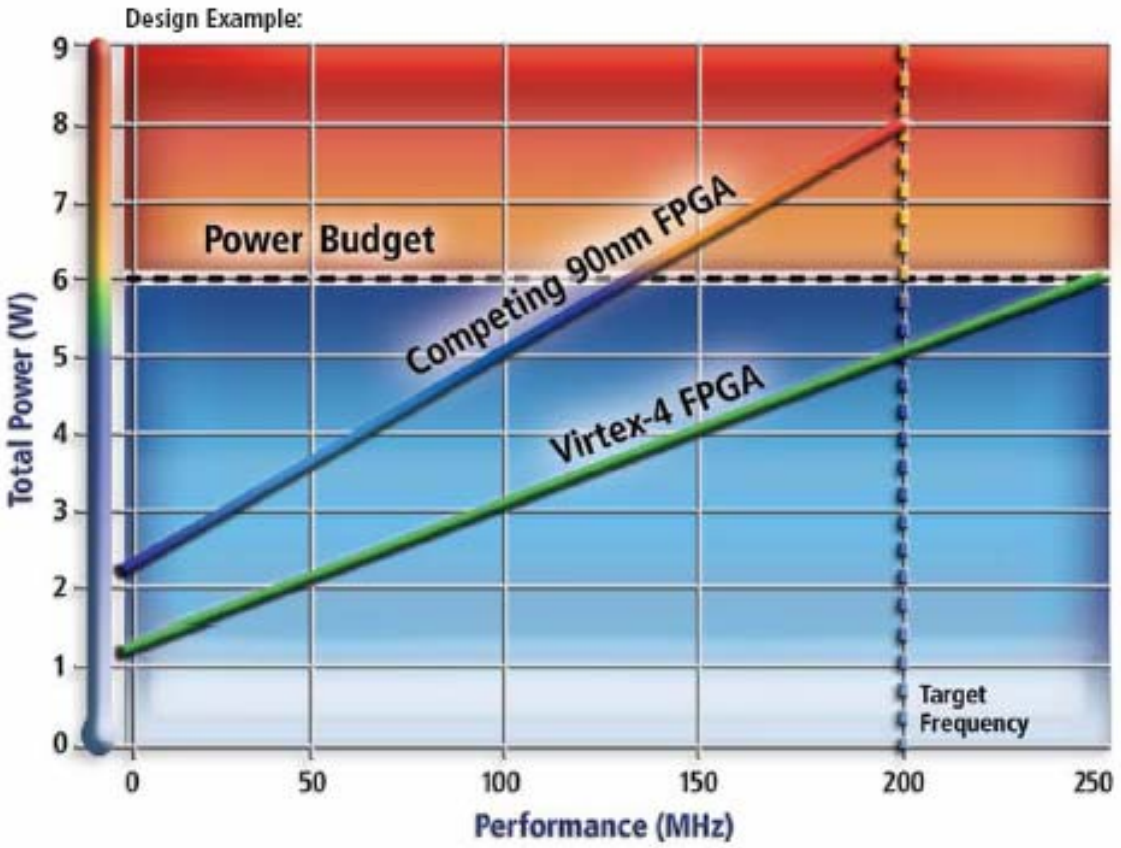


86% Less Dynamic Power



Xilinx WPTv4.1 vs. Stratix II PowerPlay v2.1

Meet Your Total Power Budget
Static and Dynamic



Design Example
Requirements -Power Budget = 6 Watts per FPGA -Target Frequency = 200 MHz -Worst case condition at Tj = 85°C
Virtex-4 total power 4.9 W
Stratix II total power 7.9 W

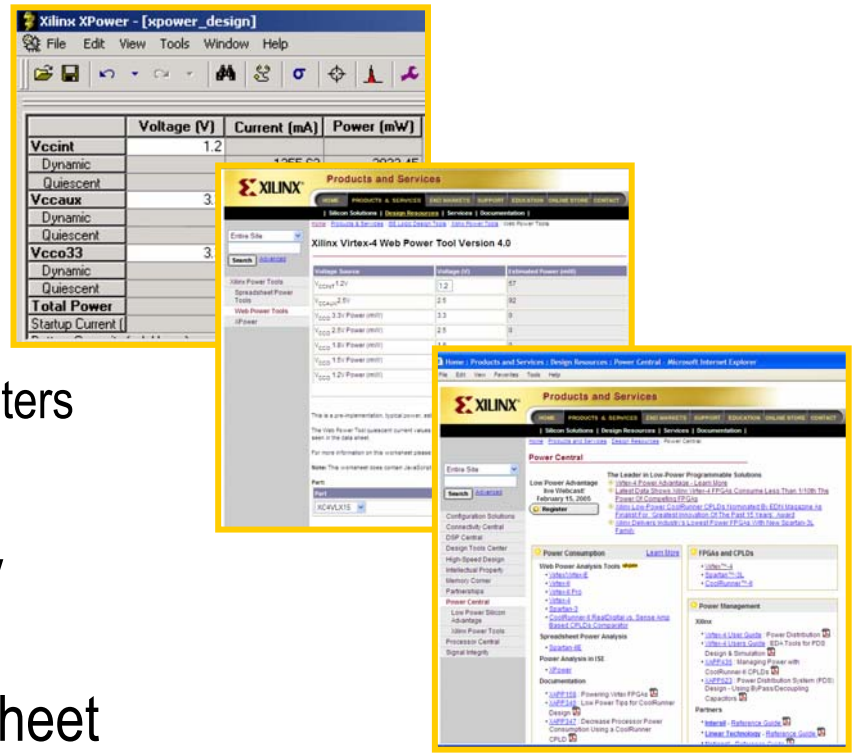
Virtex-4 LX60	Stratix II 2S60
20K LUT/FF	20K ALUT/FF
63x 18Kb BRAM	252x M4K RAM
64x DSP Slices	64x DSP Blocks
128x LVCMOS 2.5V	128x LVCMOS 2.5V

Based on 1.3V max voltage for Virtex-4 but 1.2V for Stratix II reported by Altera tool. Using industry standard 1.3V for Stratix II, Virtex-4 advantage higher!

Virtex-4 gives more performance within a given power budget

Innovative Tools for Power Analysis

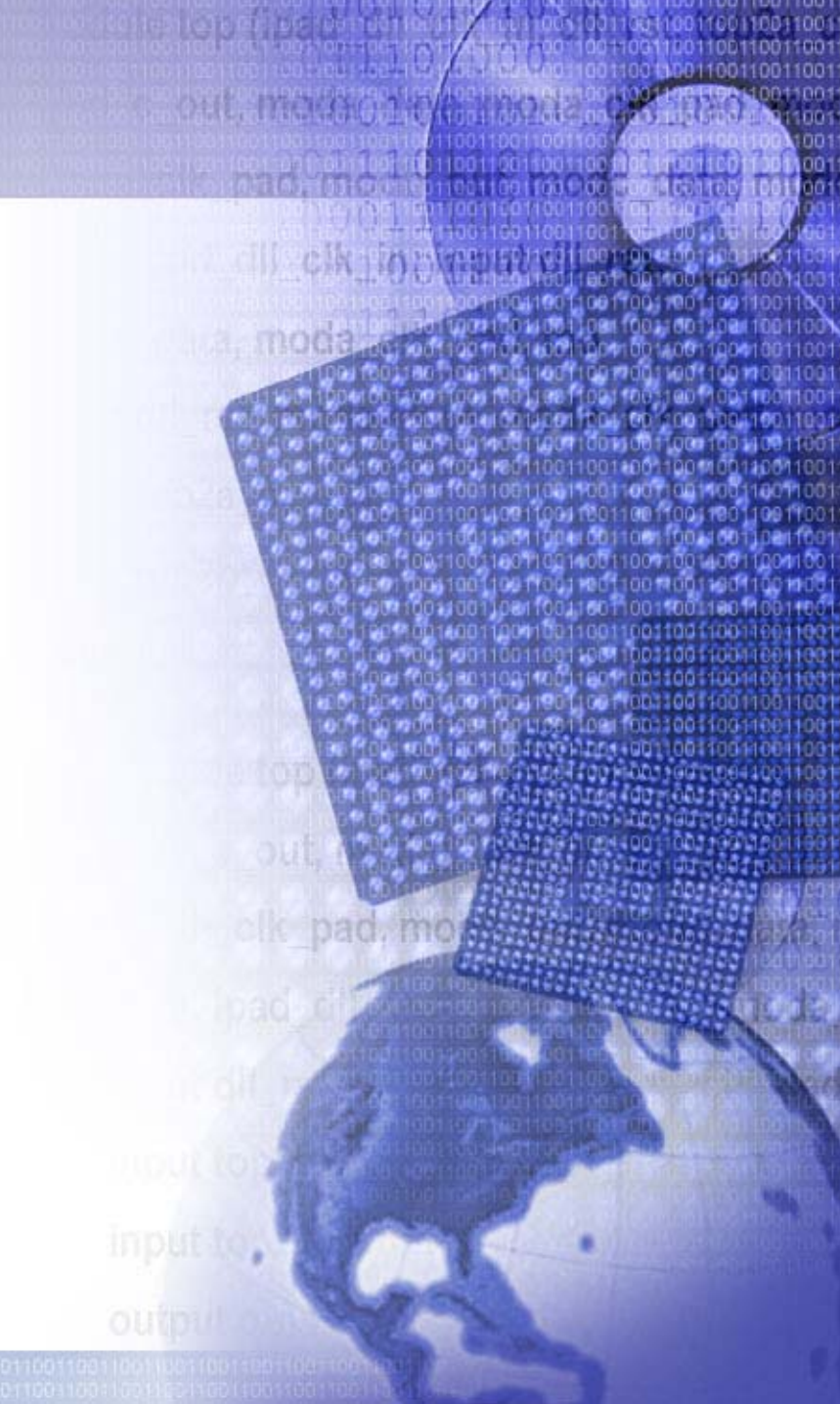
- XPower™ in ISE® software
  - Accurate prediction by design
  - Integrated into design flow
- Web Power Tool
  - Estimation based on early design parameters
- Power Management Solutions
  - Application notes, articles & power supply recommendations
- Power data specified in Virtex-4 datasheet and web power tool
  - Altera does not publish specs in datasheet; state data in tools are not specs & subject to change



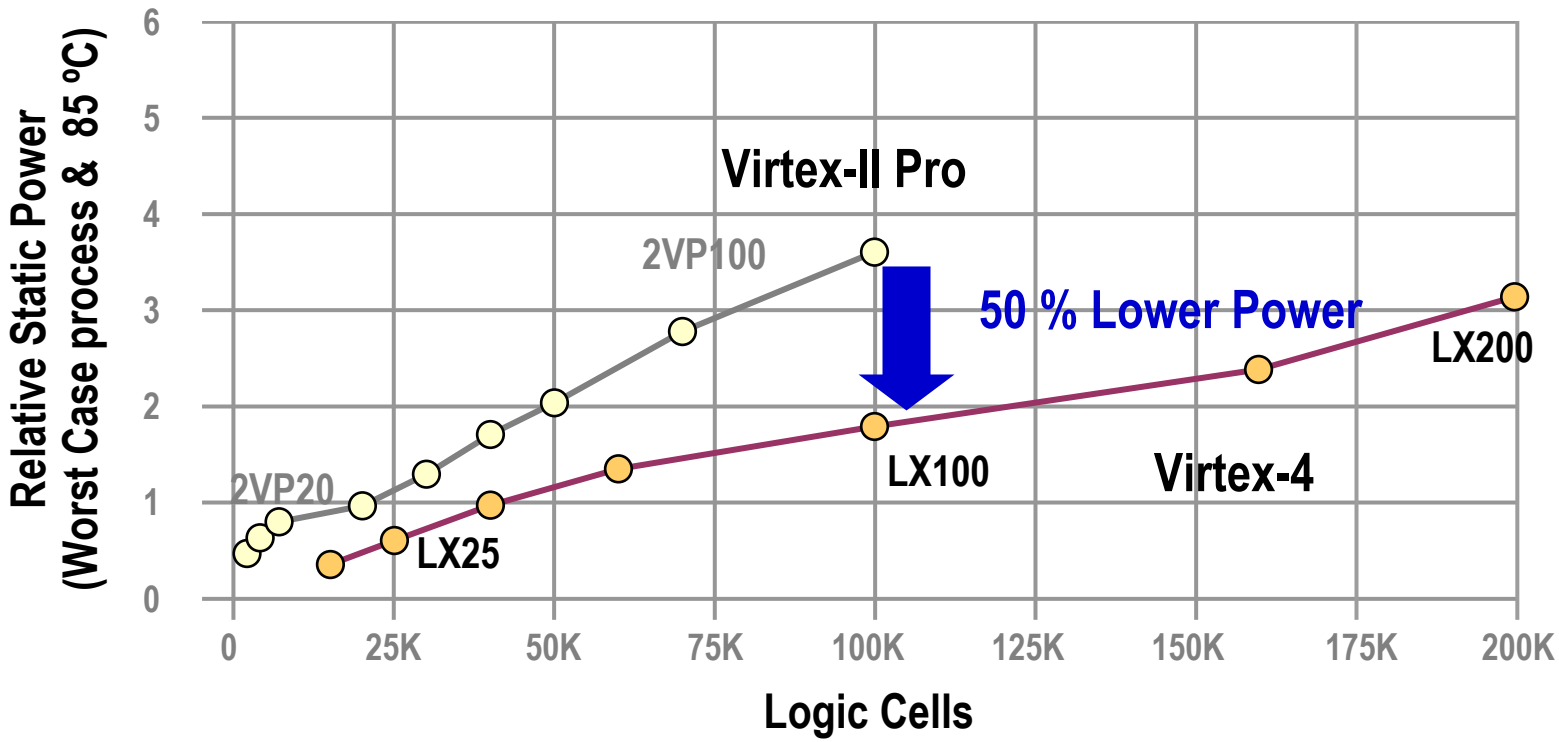
Summary

- Virtex™-4 delivers 1 to 5 Watts lower power per FPGA enabled by unique innovations
  - 73% lower static power with industry's first triple-oxide technology
  - Up to 86% lower dynamic power with high-performance embedded IP
- Reduced power simplifies design
  - Cuts BOM by eliminating the need for expensive regulators and heat sinks
  - Reduces thermal concerns and improves reliability
  - Reduced capital and operational costs
- Virtex-4 FPGAs help you meet your power budget without compromising performance
- Get started today
  - Visit www.xilinx.com/virtex4/lowpower for power analysis tools and solutions
  - Order your free ISE evaluation software and purchase the starter kit

Reference

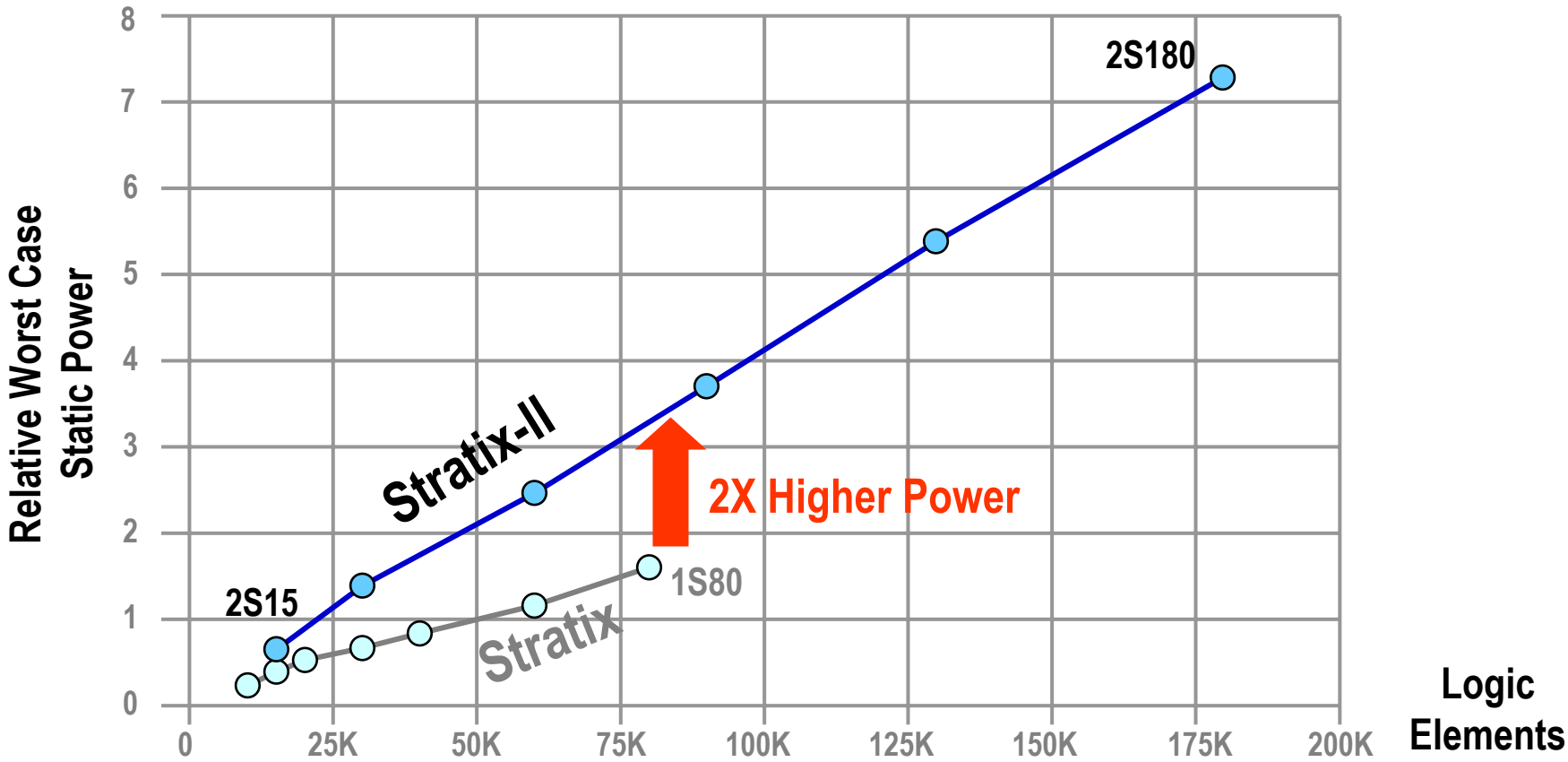


Triple-oxide Technology Cuts Static Power



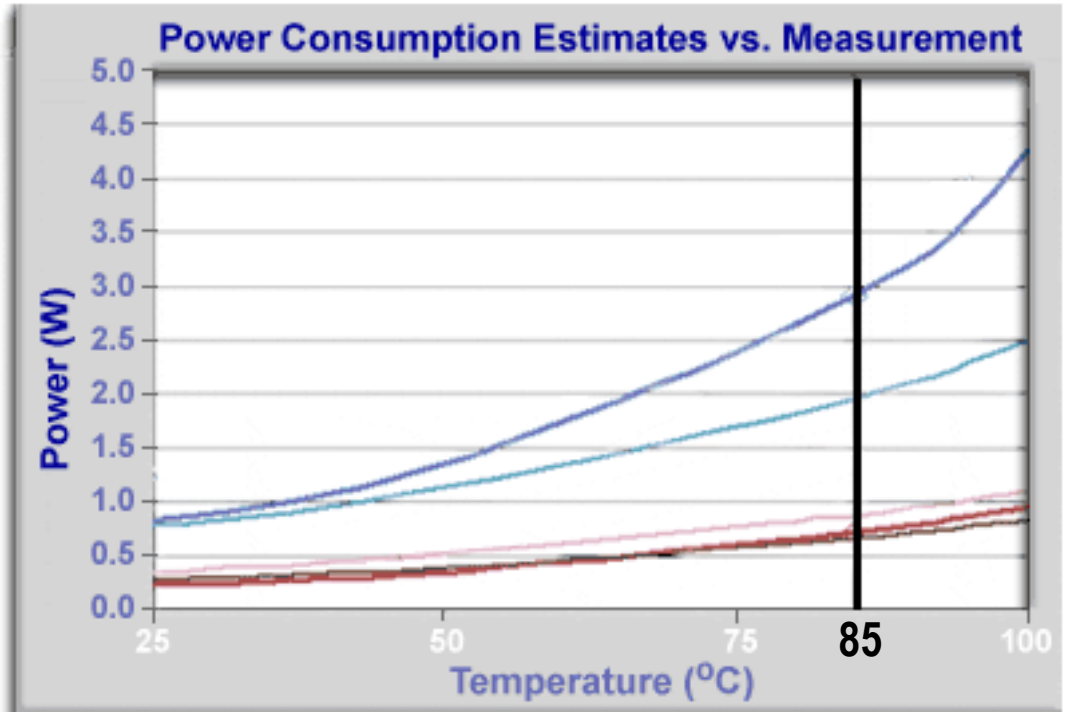
Virtex-4 has 50% lower static power than Virtex-II Pro

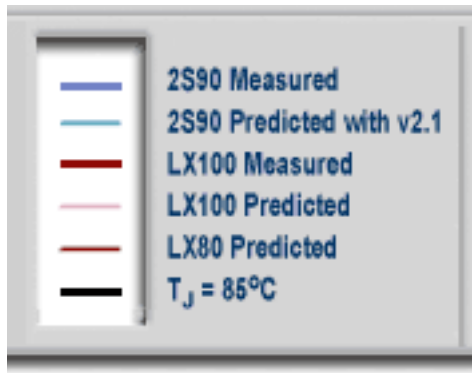
Altera's 90nm Problem
Increase in Static Power



90nm Stratix II suffers >2X higher power consumption than 130nm Stratix

Predictions vs. Measurements





Virtex-4 measures less than predicted. Stratix II consumes more power than predicted