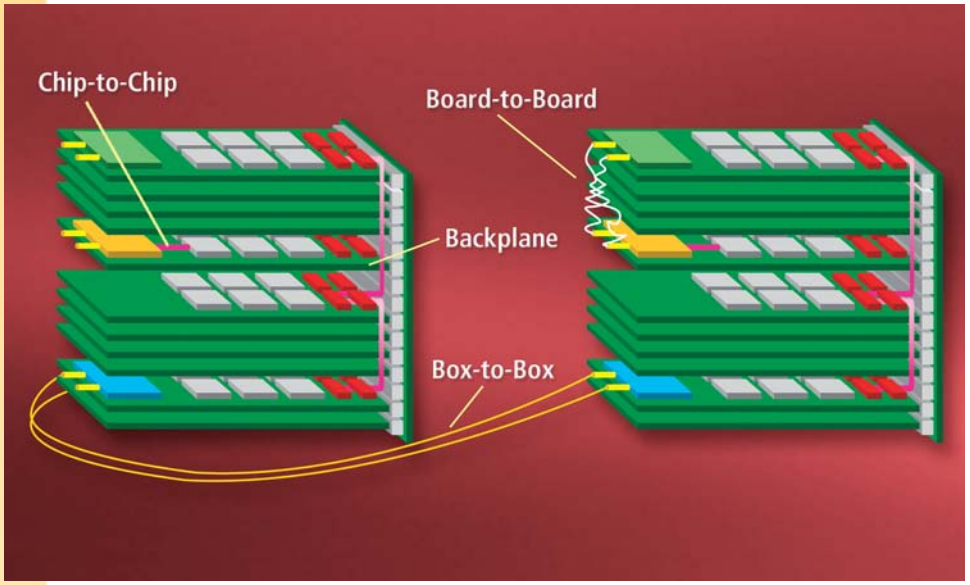
Platform FPGA System Connectivity Solution

Connect Chips, Boards, Backplane and Boxes Quickly and Easily

As processor speeds continue to increase, newer, higher-bandwidth system connectivity architectures are being defined to keep up. Using these newer technologies in your products requires a combination of flexible, high-performance physical I/O and support for implementing upper layers of the protocol.

The Xilinx connectivity solution provides everything you need to solve your system I/O challenges and reduce cost. Now, you can re-use legacy designs by bridging between new and existing connectivity standards without worrying about interface mismatches.

The Xilinx connectivity solution fully addresses all aspects of system-connectivity in high-performance designs. Our proven, third-generation RocketIO™ multi-gigabit serial transceivers and SelectIO™-Ultra parallel I/Os, combined with IP and reference designs, enable you to build flexible, adaptable, reliable, and interoperable solutions for interfacing to major serial or parallel standards.

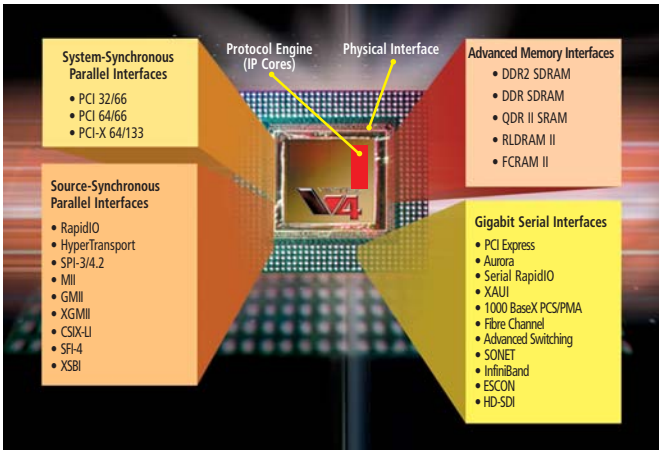


Meet Any Standard

Xilinx provides the most comprehensive system connectivity solution to address your interface needs ranging from "inside-the-box" to "box-to-box" applications. The benefits include:

- **Highest Performance** — The Xilinx proven third-generation multi-gigabit RocketIO programmable serial transceiver can now support all chip-to-chip, chip-to-optics, legacy, and new backplane applications from 600 Mbps to 11.1 Gbps. SelectIO-Ultra programmable parallel I/Os with ChipSync™ technology let you design up to 1 Gbps LVDS systems with ease. Plus, the industry's fastest FPGA fabric gives you the performance you need to implement the required specifications.
- **Reduced System Cost** — You have access to a wide variety of pre-verified, standards-compliant IP cores that you can drop into your designs, saving you development time and cost. With the latest Virtex-4™ EasyPath™ solutions, you can lower your system cost even more when going to production.
- **Reduced Risk** — Your design is fully programmable to keep up with the rapidly changing standards landscape, and there are no additional NRE or mask costs to deal with. If your requirements change in the middle of your design cycle, you can quickly and easily accommodate the changes without incurring a large penalty.
- **Proven Interoperability** — We ensure that our IP cores and reference designs are tested for standards compliance and interoperability with other standard products at industry-recognized forums such as the PCI Express plugfest held by the PCI SIG and the UNH Interoperability lab for Ethernet.

XILINX®



Xilinx Platform FPGA Connectivity Solution

Take the Next Step

For more details on the Xilinx system connectivity solution, as well as other high-speed design resources, visit the Connectivity Central website at **www.xilinx.com/connectivity**. Contact your Xilinx sales representative for IP/Reference Design availability dates.

Connectivity IP/Reference Design Summary

Solution	Standard	Raw Bandwidth	I/O	Devices Supported
SPI-3 (POS-PHY L3)	OIF-SPI3-01.0 Saturn POS-PHY L3	2.48 Gbps	32-bit, 104 MHz SelectIO LVCMOS	Virtex-II™ Series, Virtex-4™, Spartan-IIE™, Spartan-3™
SPI-4.2 (POS-PHY L4)	OIF-SPI4-02.0 Saturn POS-PHY L4	16 Gbps	16-bit, up to 1 Gbps DDR SelectIO LVDS	Virtex-II Series, Virtex-4*
SPI-4.2 to Quad SPI-3 Bridge Reference Design	OIF-SPI3-01.0 OIF-SPI4-02.0	10 Gbps	32-bit, 104 MHz SelectIO LVCMOS 16-bit, up to 1 Gbps DDR SelectIO LVDS	Virtex-II Series, Virtex-4*
GFP Mapper	ITU-T G.7041/Y.1303	2.5 Gbps or 10 Gbps	32-bit, 78 MHz Internal I/O 64-bit, 156 MHz Internal I/O	Virtex-II Series, Virtex-4*
10GE MAC w/ XAUI	IEEE 802.3ae 2002	12.5 Gbps	Four RocketIO Transceivers @ 3.125 Gbps	Virtex-II Pro, Virtex-4 FX*
XAUI Only (no MAC)	IEEE 802.3ae 2002	12.5 Gbps	Four RocketIO Transceivers @ 3.125 Gbps	Virtex-II Pro, Virtex-4 FX*
10GE MAC w/ XGMII	IEEE 802.3ae 2002	10 Gbps	32-bit, 156.25 MHz DDR SelectIO XGMII HSTL	Virtex-II Series, Virtex-4*
XGMII Reference Design	IEEE 802.3ae 2002	10 Gbps	32-bit, 156.25 MHz DDR SelectIO XGMII HSTL	Virtex-II Series, Virtex-4*
XSBI Reference Design	IEEE 802.3ae 2002 (XSBI)	10 Gbps	16-bit, 644 MHz SelectIO LVDS	Virtex-II Pro, Virtex-4*
SFI-4 Reference Design	OIF-SFI4-01.0	10 Gbps	16-bit, 622 MHz SelectIO LVDS	Virtex-II Pro, Virtex-4*
GbE MAC w/ GMII	IEEE 802.3-2002	1 Gbps	8-bit, 125 MHz SelectIO GMII	Virtex-II Series, Virtex-4*, Spartan-IIE
Tri-mode Ethernet MAC w/ MII & GMII	IEEE 802.3-2002 IEEE 802.3	10/100/1001000 Mbps	8-bit, 125 MHz SelectIO GMII 16-bit, 25 MHz SelectIO MII	Virtex-II Series, Virtex-4*
1000 BaseX PCS/PMA Only (no MAC)	IEEE 802.3-2002	1.25 Gbps	One RocketIO Transceiver @ 1.25 Gbps	Virtex-II Pro, Virtex-4 FX*
Ethernet Aggregation Reference Design	IEEE 802.3-2002 OIF-SPI4-02.0	Up to 10 Gbps	One RocketIO Transceiver @ 1.25 Gbps 16-bit, up to 1 Gbps DDR SelectIO LVDS	Virtex-II Pro, Virtex-4 FX*
1G/2G Fibre Channel	ANSI INCITS X3-230-1994 (R1999), X3-297-1997 (R2002), X3-303-1998 FC-PH, T11-FC-FS, and T11-FC-SW-3	1.0625 Gbps or 2.125 Gbps	One or Two RocketIO Transceivers @ Up To 2.5 Gbps	Virtex-II Pro, Virtex-4 FX*
Configurable Physical Coding Sublayer Reference Design for 1G/2G Fibre Channel, 1000 BaseX Ethernet and ESCON	ANSI X3.230 (1994) FC-PH clause 12, IEEE802.3-2002 clause 36 and 37, ANSI X3.296 (1997) SBCON clause 7	2.125 Gbps or 1.0625 Gbps or 1.25 Gbps or 200 Mbps	One RocketIO Transceiver @ Up To 2.5 Gbps	Virtex-II Pro, Virtex-4 FX*
Aurora Reference Designs	Aurora Protocol Specification v1.2	Up to 264 Gbps	One to 24 RocketIO Transceivers @ 11.1 Gbps	Virtex-II Pro, Virtex-4 FX*
PCI Express Endpoint	PCI Express Base Specification v1.1	Up to 10 Gbps	One or Four RocketIO Transceivers @ 2.5 Gbps	Virtex-II Pro, Virtex-4 FX*
Advanced Switching Endpoint	Advanced Switching Specification v1.0	Up to 10 Gbps	One or Four RocketIO Transceivers @ 2.5 Gbps	Virtex-II Pro, Virtex-4 FX*
Serial RapidIO Endpoint	RapidIO Interconnect Specification v1.3	Up to 12.5 Gbps	One or Four RocketIO Transceivers @ 3.125 Gbps	Virtex-II Pro, Virtex-4 FX*
Parallel RapidIO Endpoint	RapidIO Interconnect Specification v1.3	4 Gbps	8-bit, 500 Mbps DDR SelectIO LVDS	Virtex-II Series, Virtex-4*
PCI 33	PCI v3.0	Up to 2 Gbps	32-bit or 64-bit, 33 MHz SelectIO PCI	Virtex-II Series, Virtex-4*, Spartan-IIE, Spartan-3
PCI 66	PCI v3.0	Up to 4 Gbps	32-bit or 64-bit, 66 MHz SelectIO PCI	Virtex-II Series, Virtex-4*, Spartan-IIE
PCI-X 133	PCI-X v2.0 Mode 1	Up to 8 Gbps	64-bit, 133 MHz SelectIO PCI-X	Virtex-II Series, Virtex-4*
CSIX Reference Design	CSIX-L1 HSTL	6.4 Gbps	32-bit, 200 MHz SelectIO	Virtex-II Series
HyperTransport Single-Ended Slave	HyperTransport v2.1	6.4 Gbps	8-bit, 800 Mbps DDR SelectIO HyperTransport	Virtex-II Series
10/100 Ethernet MAC	IEEE 802.3	10/100 Mbps	16-bit, 25 MHz SelectIO MII	Virtex-II Series, Spartan-IIE, Spartan-3

** Please contact your sales representative for IP/Reference Design availability dates*

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