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Challenges and opportunities for FPGA platforms

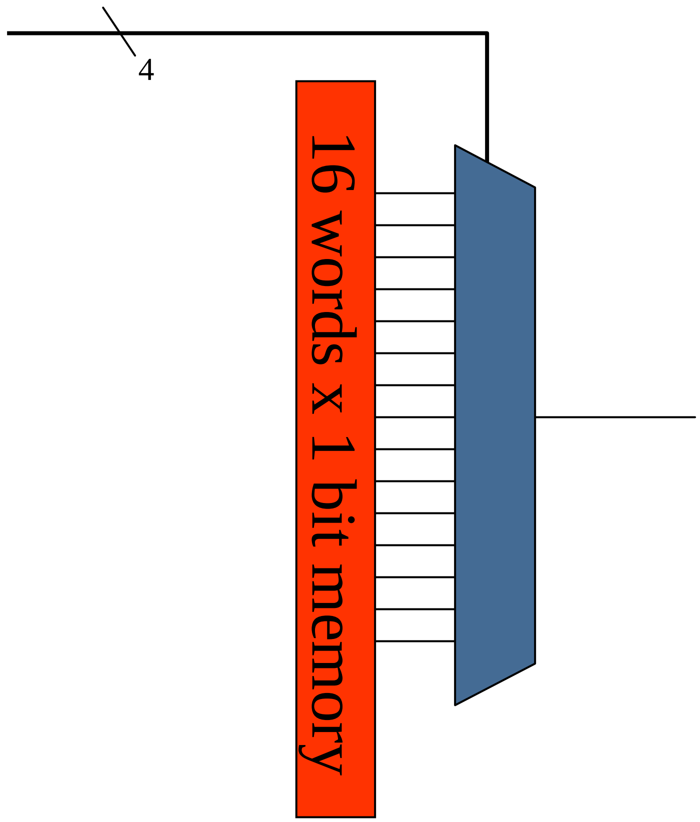
Ivo Bolsens

Xilinx Research Labs

Outline

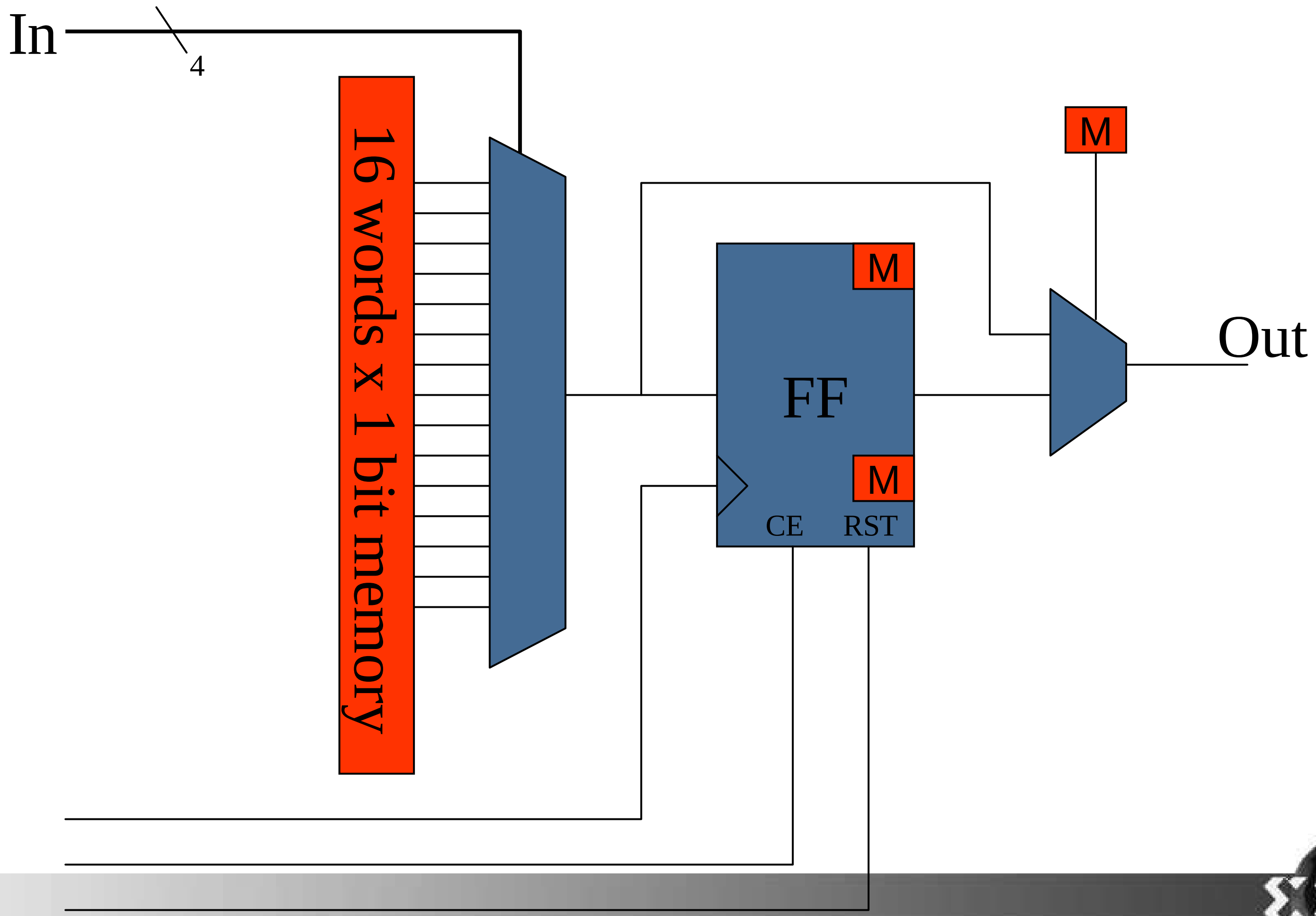
- Intro
- ASICs buck the tide
- FPGA ride the tide
- Programmable system platform
- Future

Programmable Logic

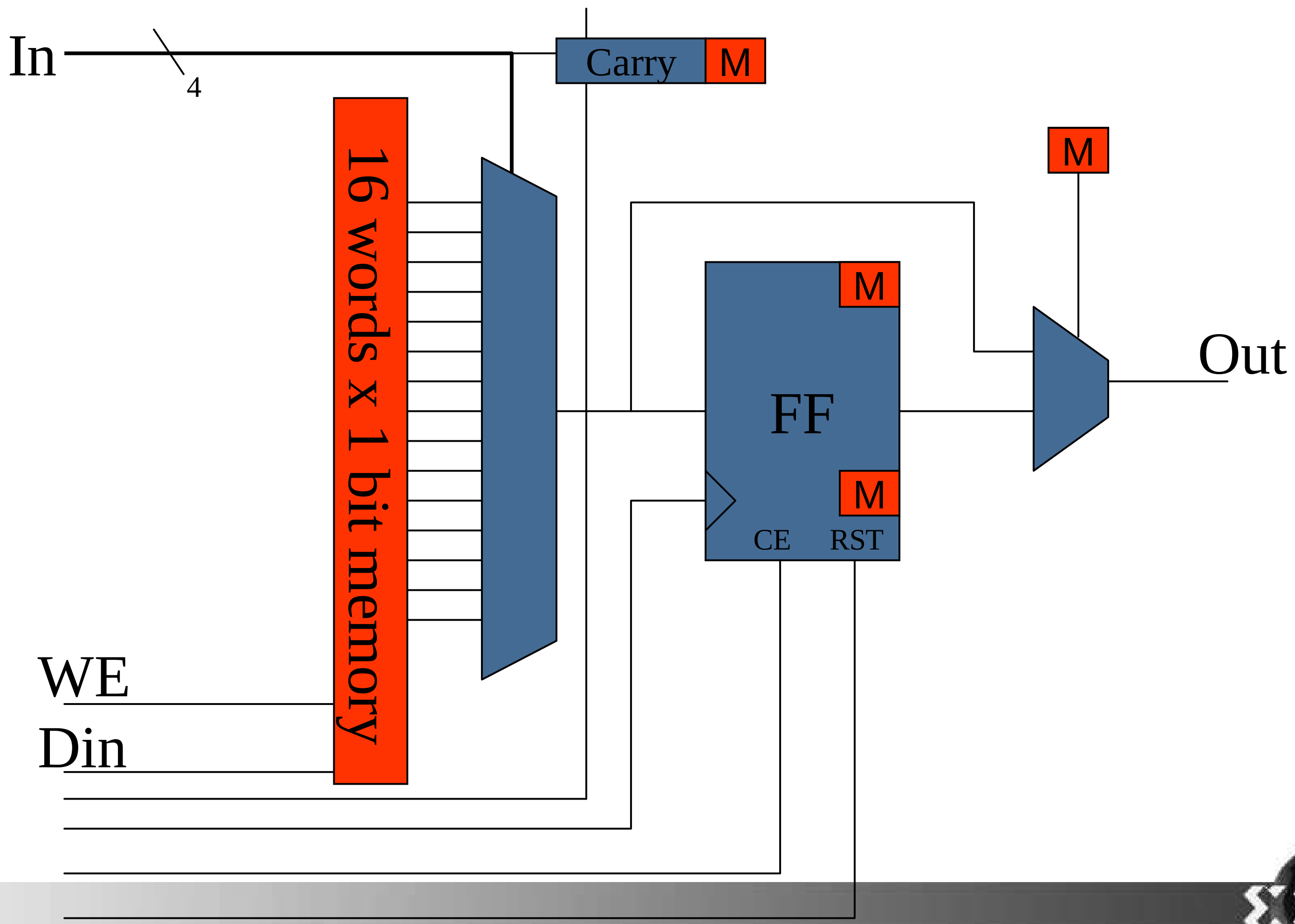


A LookUp Table (LUT)
any function of 4 inputs

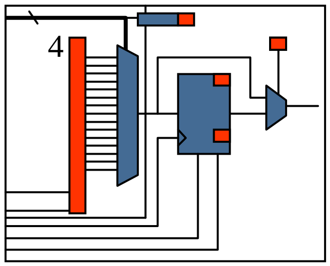
Add a register to make a Logic Cell



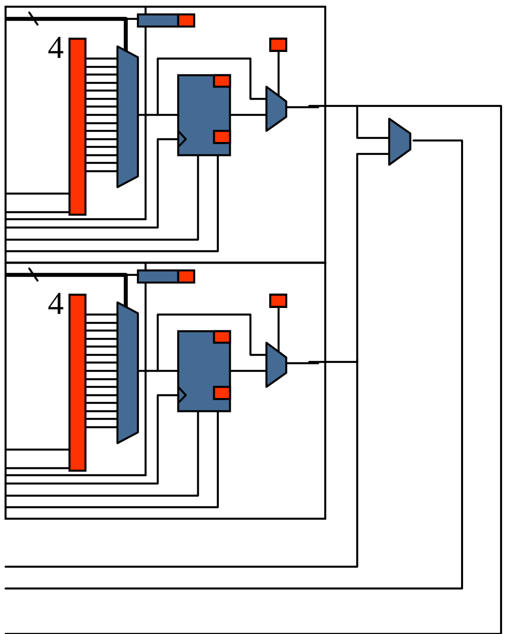
Memory and Arithmetic



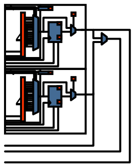
A Slice …



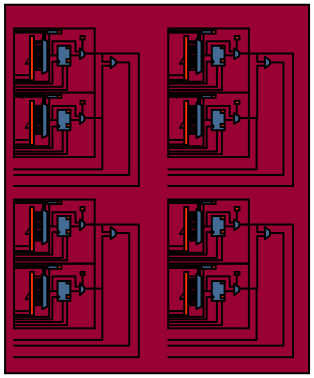
A Slice: 2 Logic Cells + F(5) ...



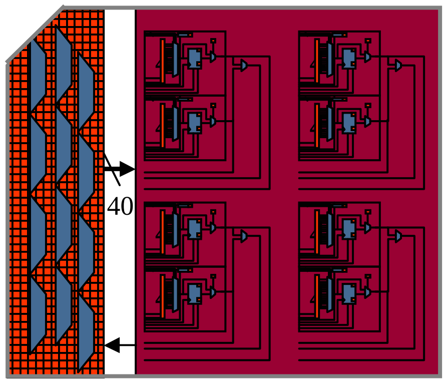
A CLB: 4 Slices + …



A CLB: 4 Slices



A CLB: 4 Slices + Input/Output



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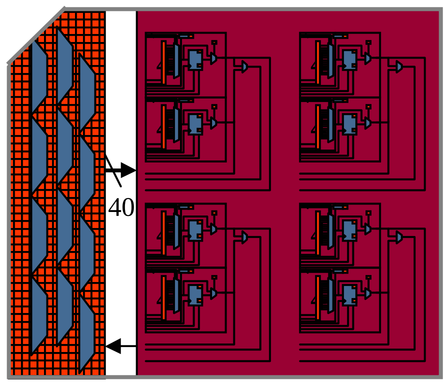

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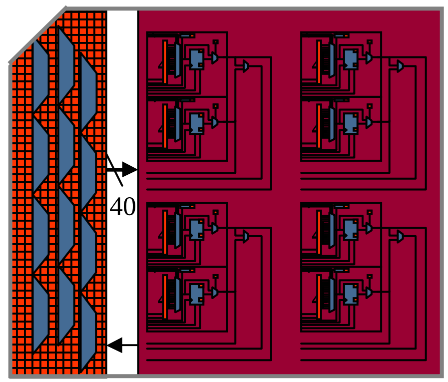

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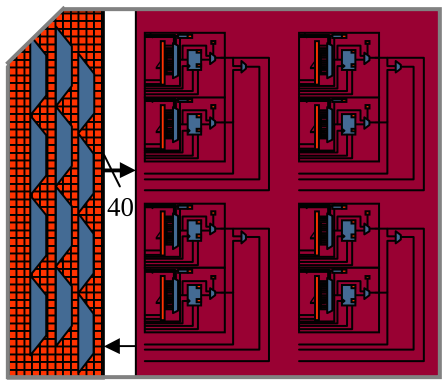
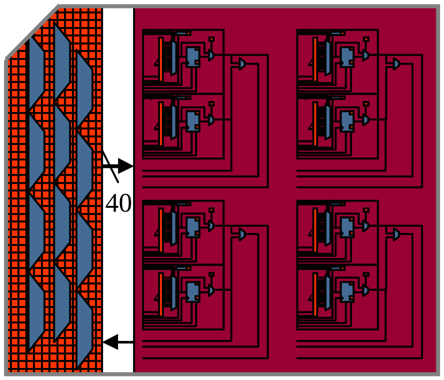
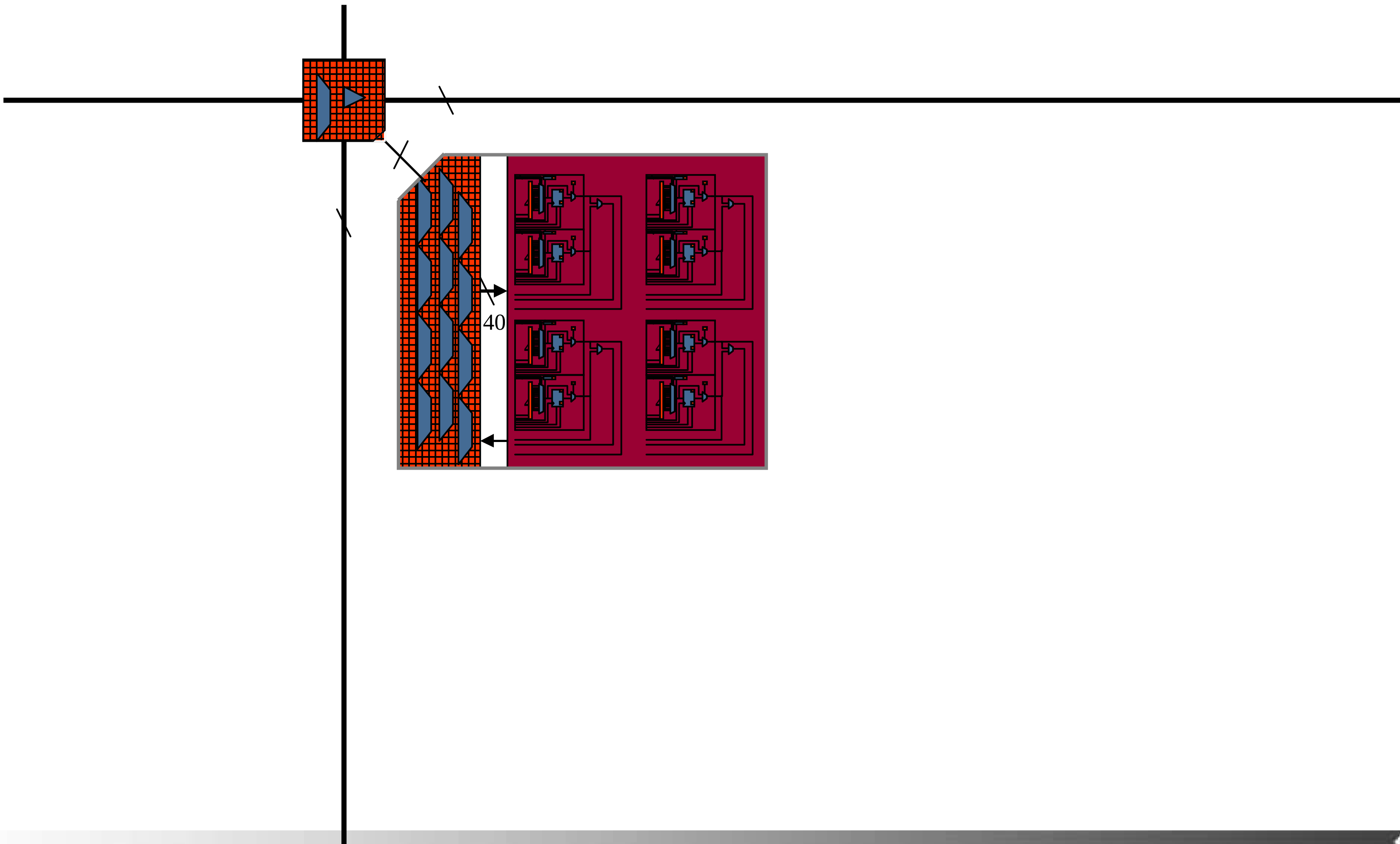


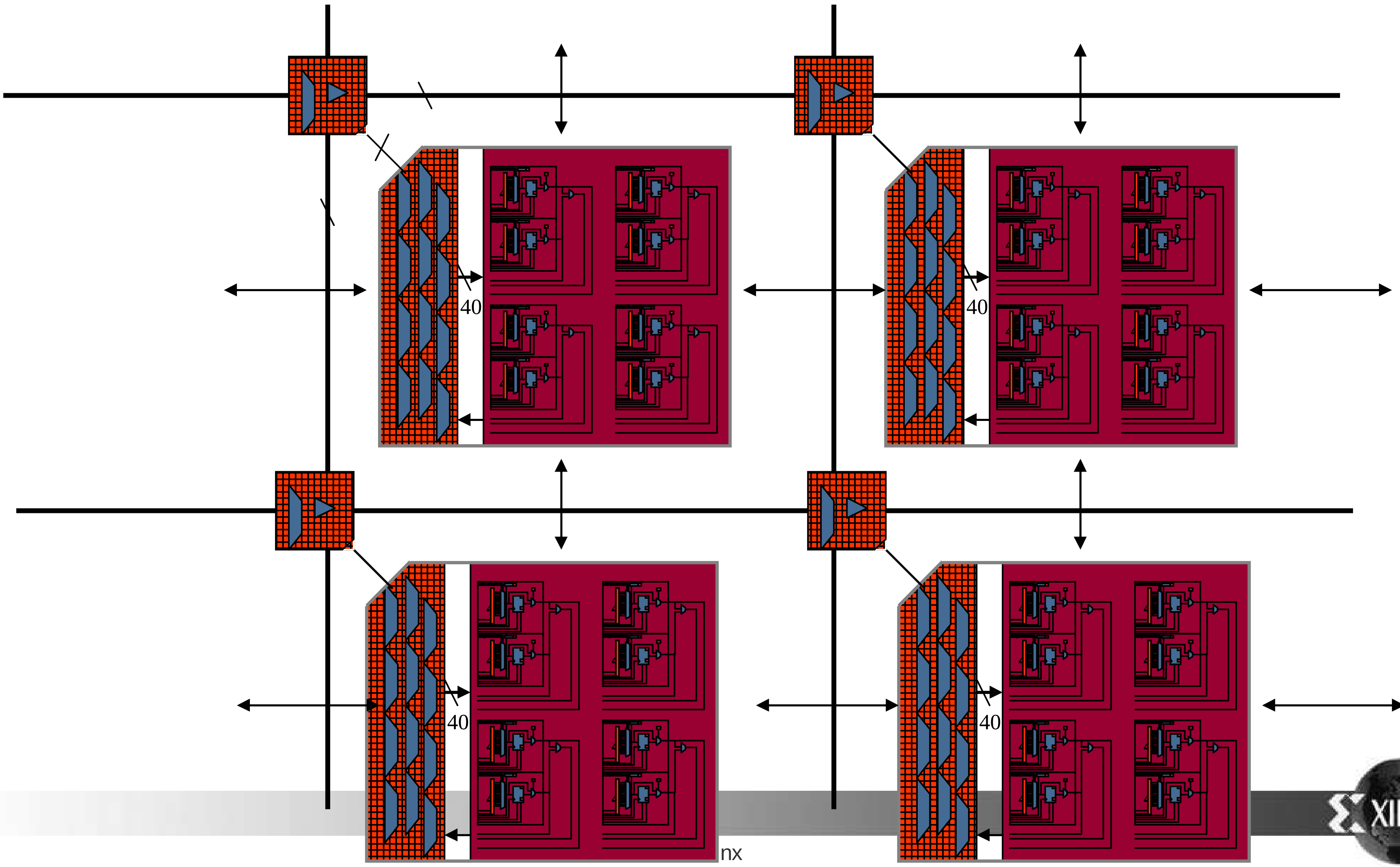
A CLB: 4 Slices + Input/Output



Add Interconnect



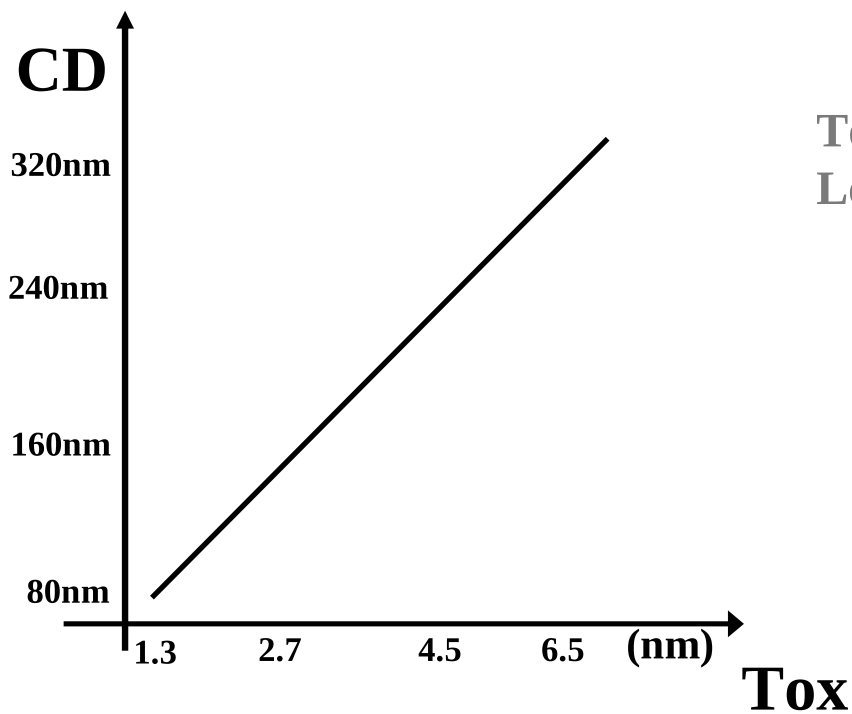
Build an Array

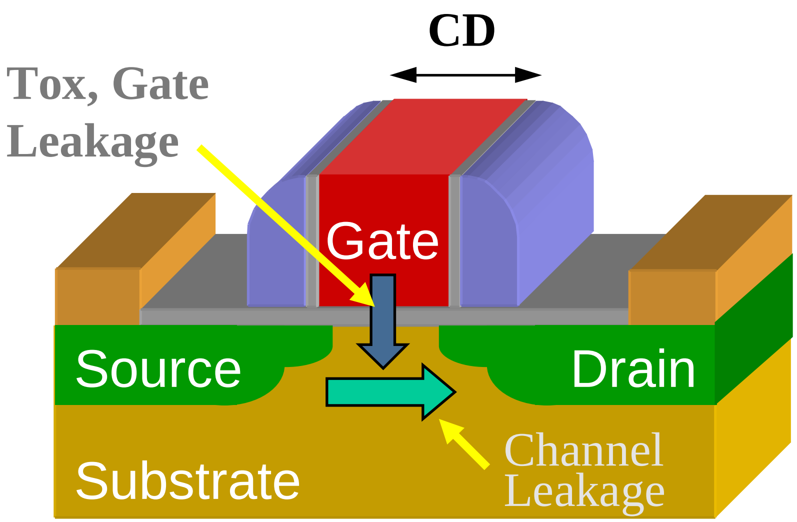


ASICs buck the tide, FPGAs ride the tide

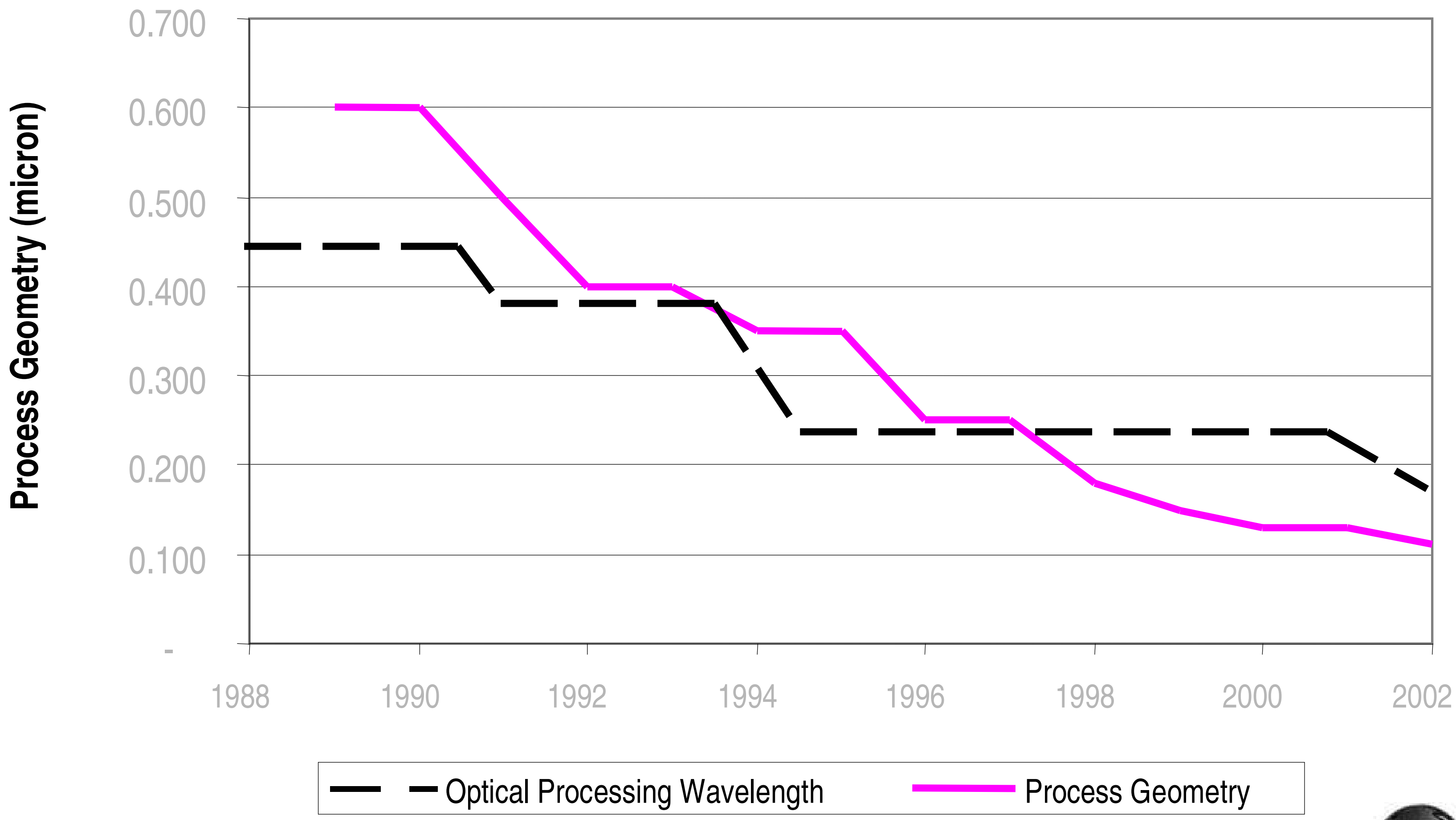
Moore’s Law

A tale of two numbers

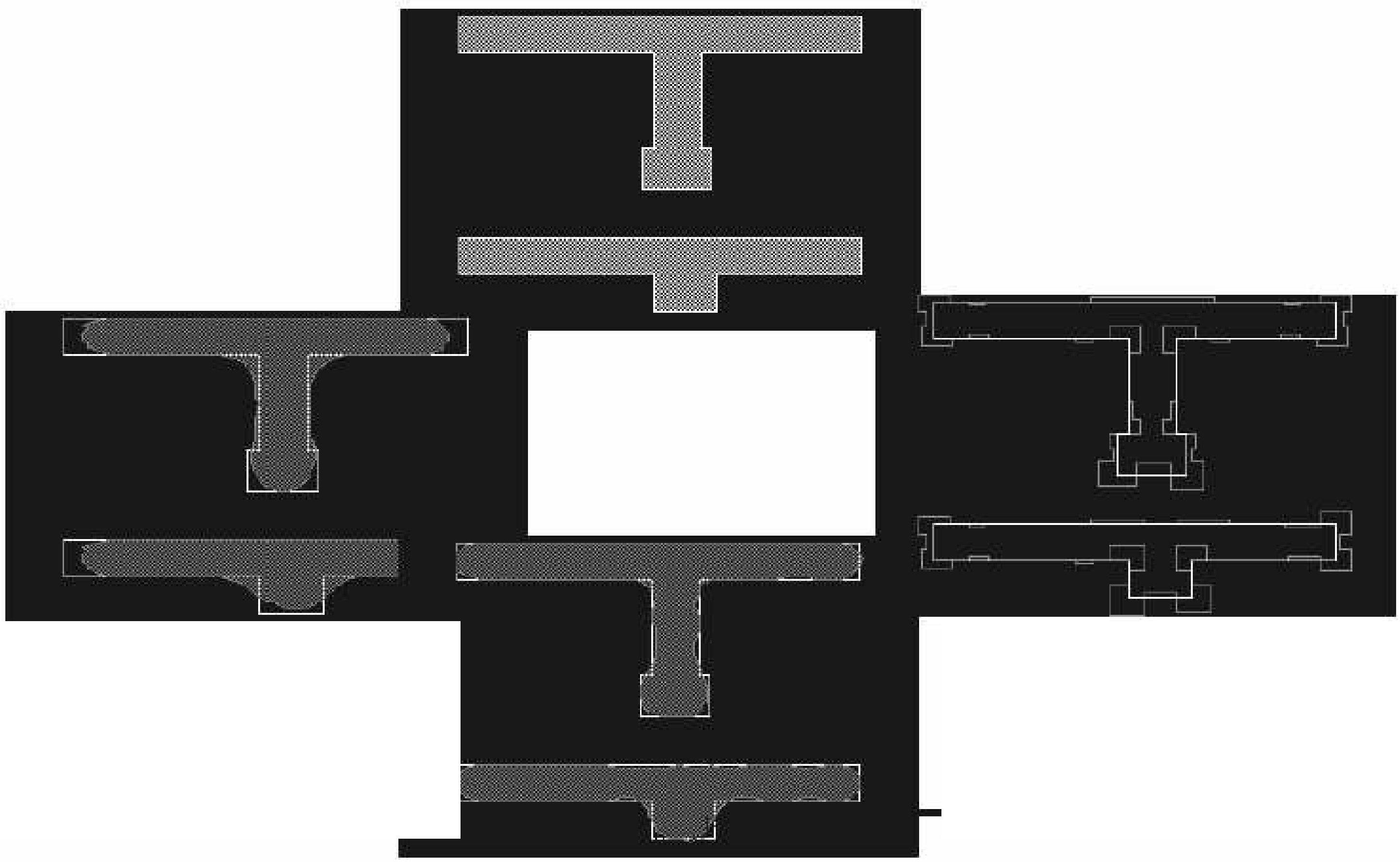




Trend: Line Widths Smaller Than the Wavelength of Light

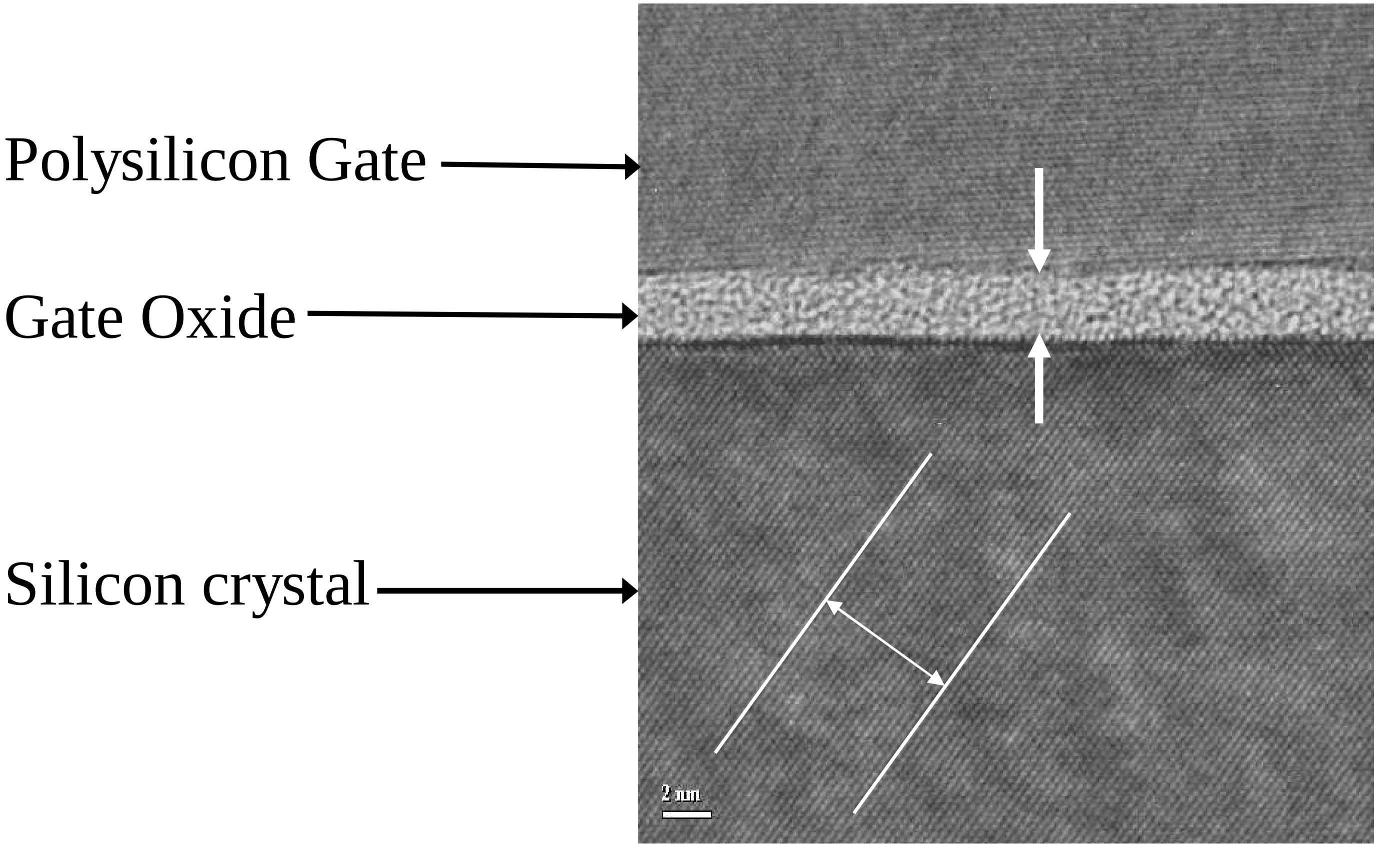


Painting a one cm line with a three cm brush…



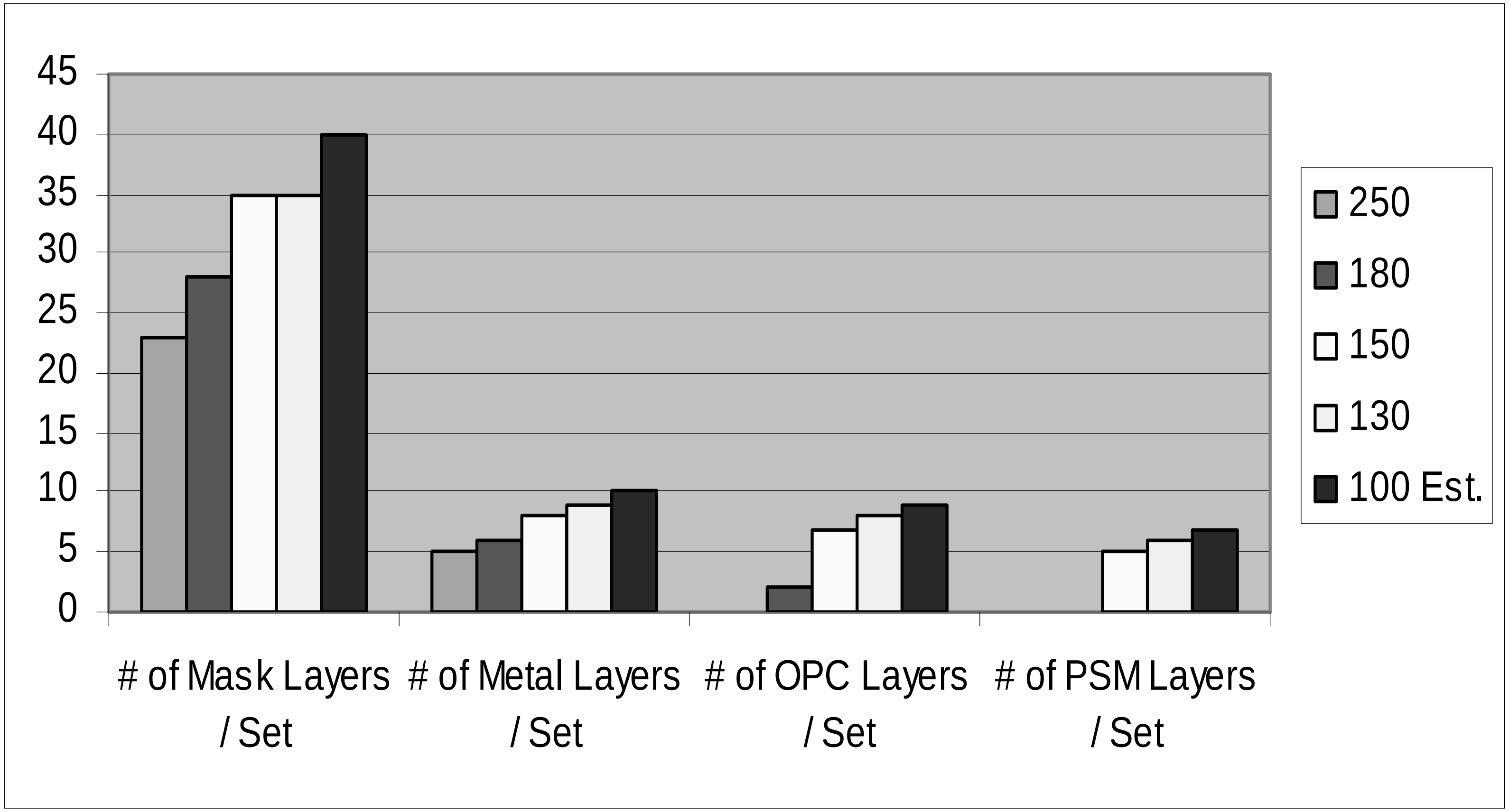
Courtesy : IBM

Gate Oxide

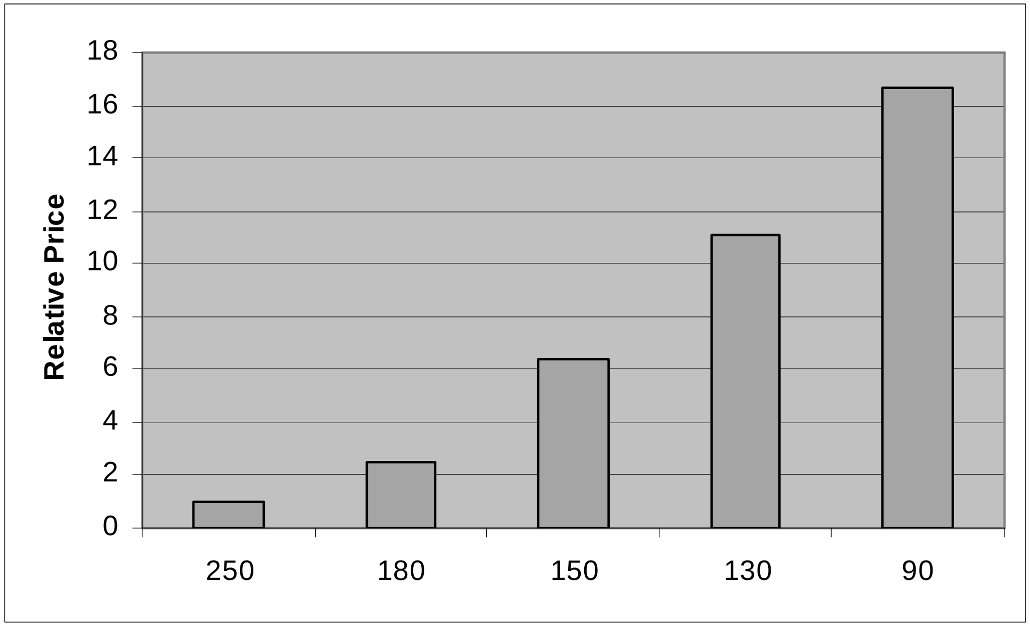


- About 10 molecular layers of SiO_2 for this 150nm example
- 90nm technology is about half the thickness

Mask Layers per Mask Set

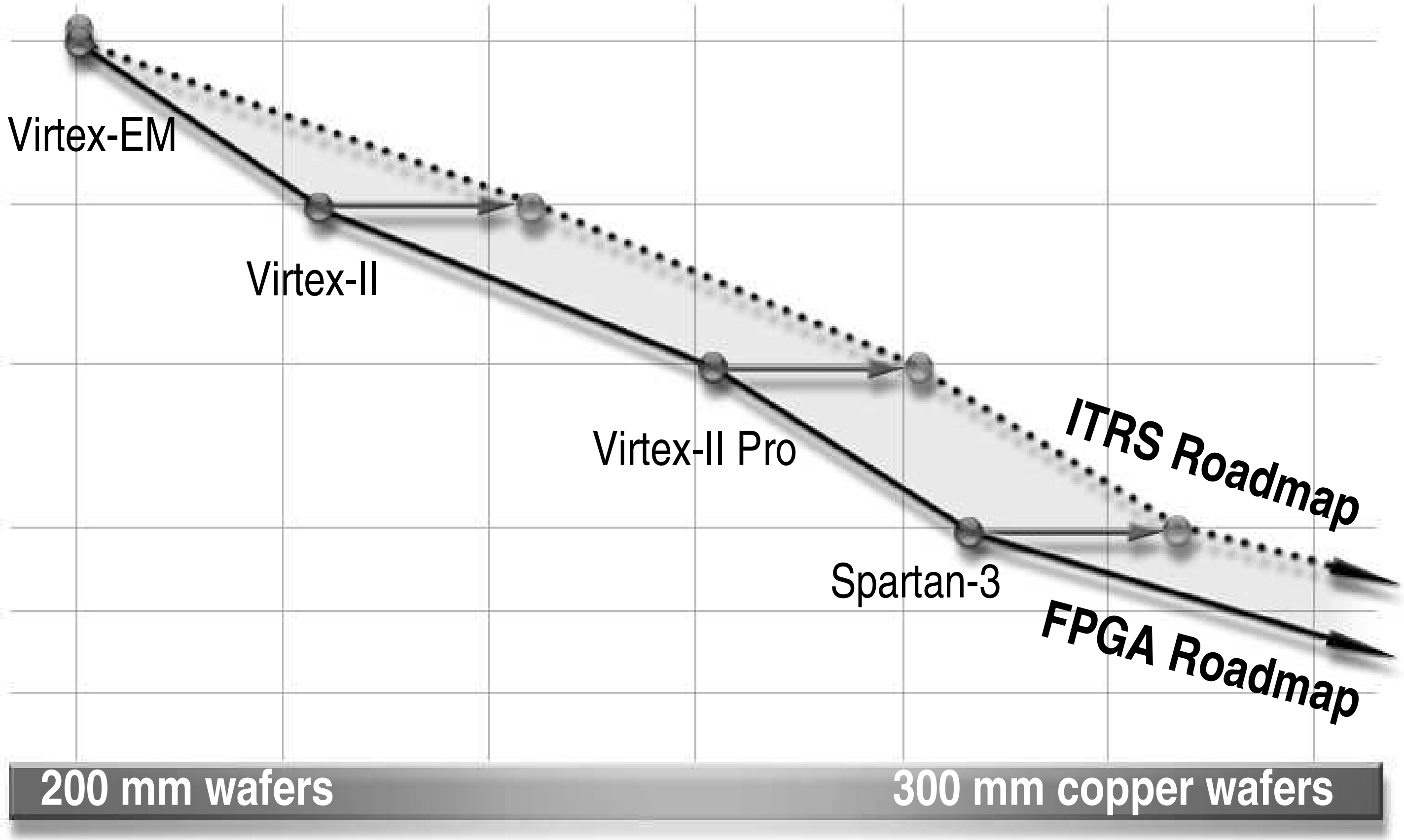


Mask Set Price Trend vs. Technology



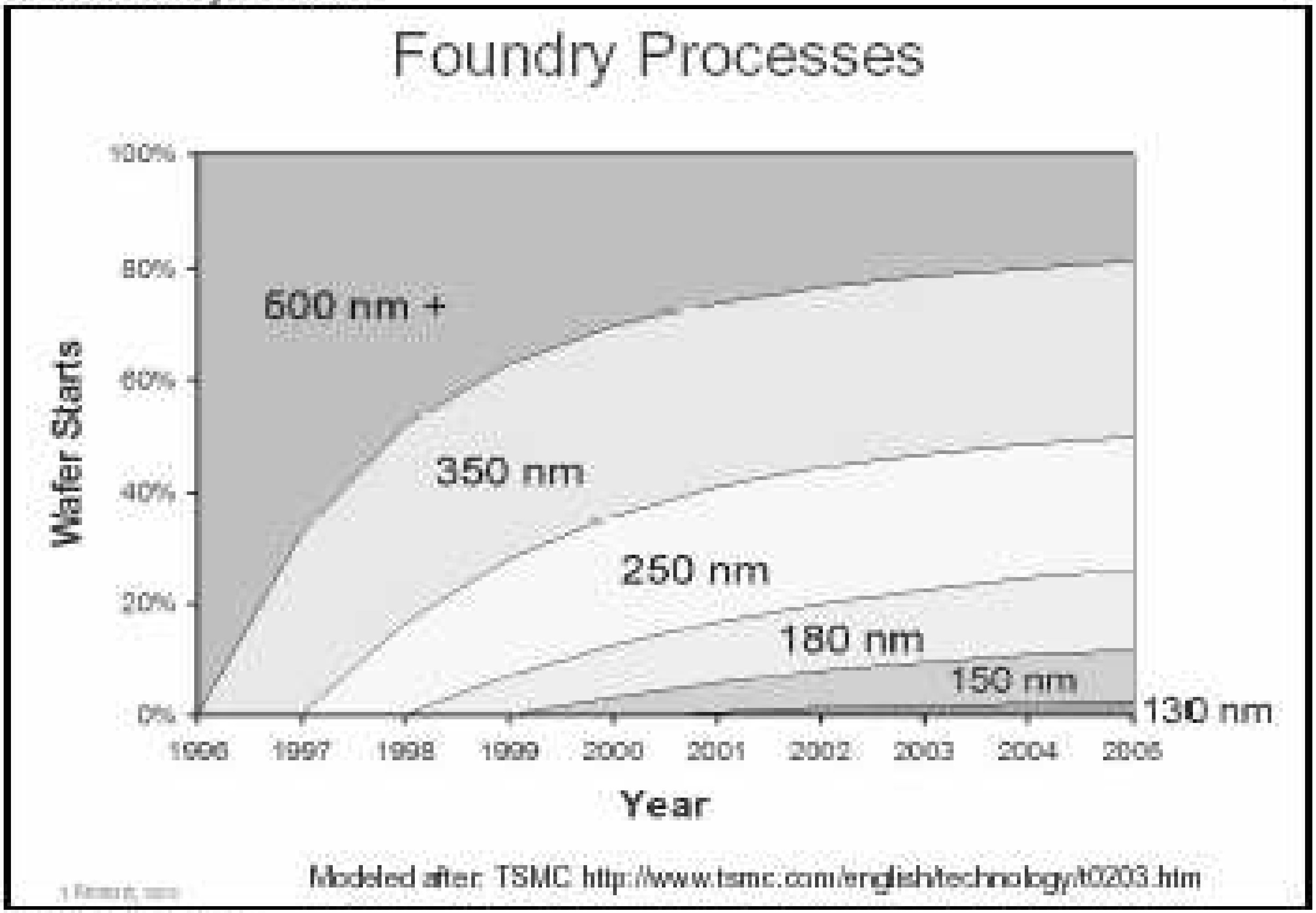
Technology Node [nm]

FPGAs in The Forefront of The Technology Curve



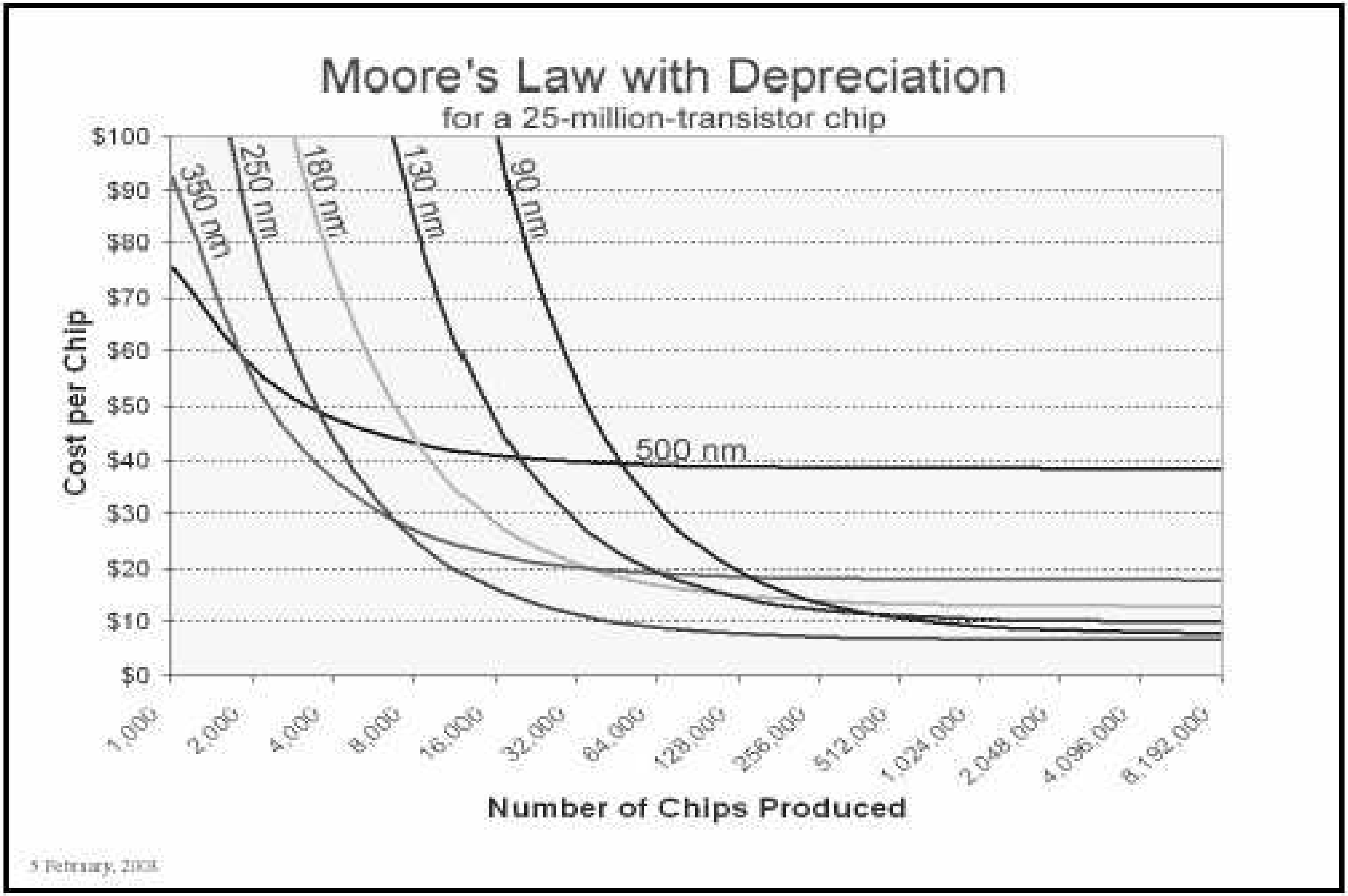
Wafer Starts

Chart 2: Foundry Processes



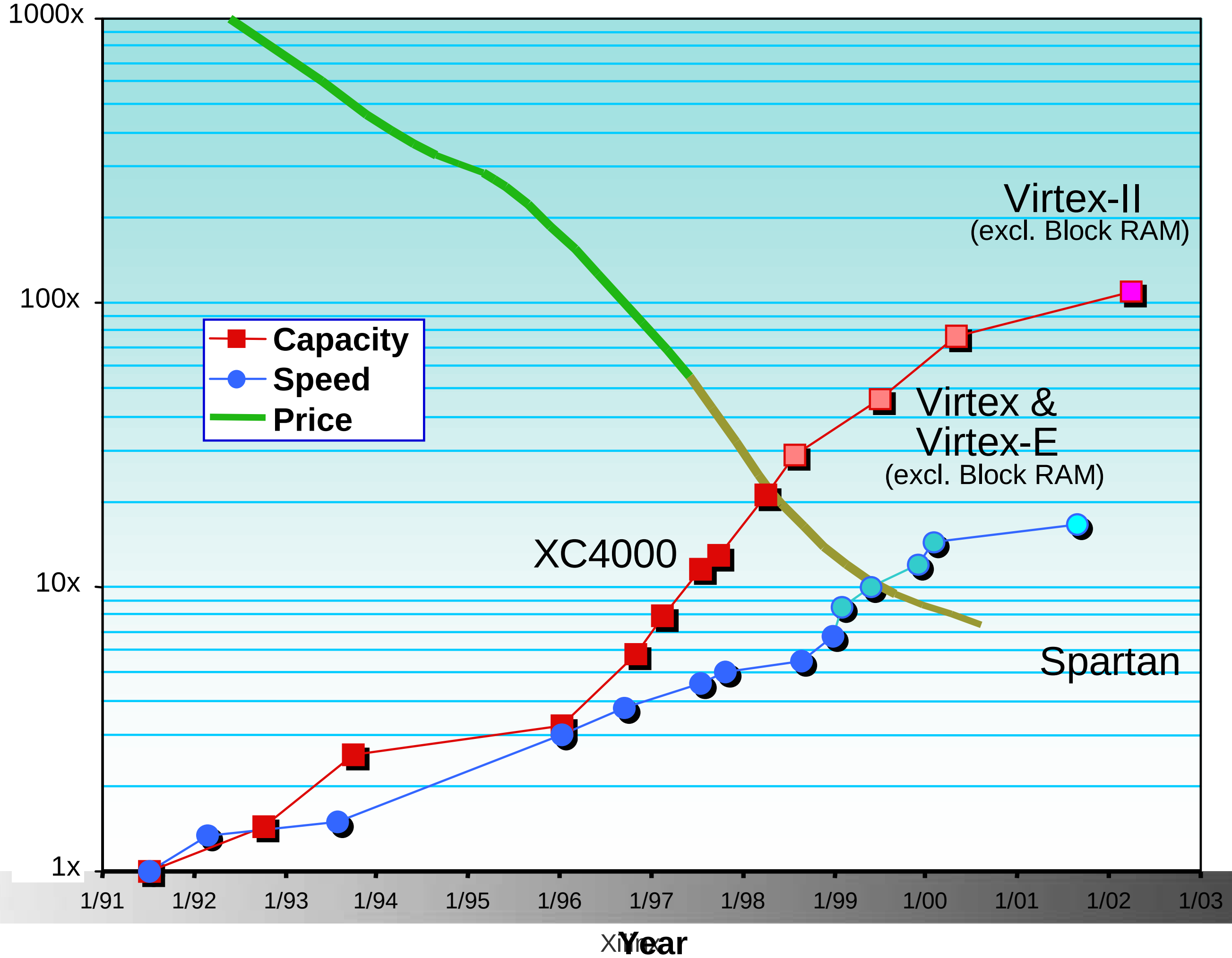
Source: Nick Tredennick

Economy of 'Scale'

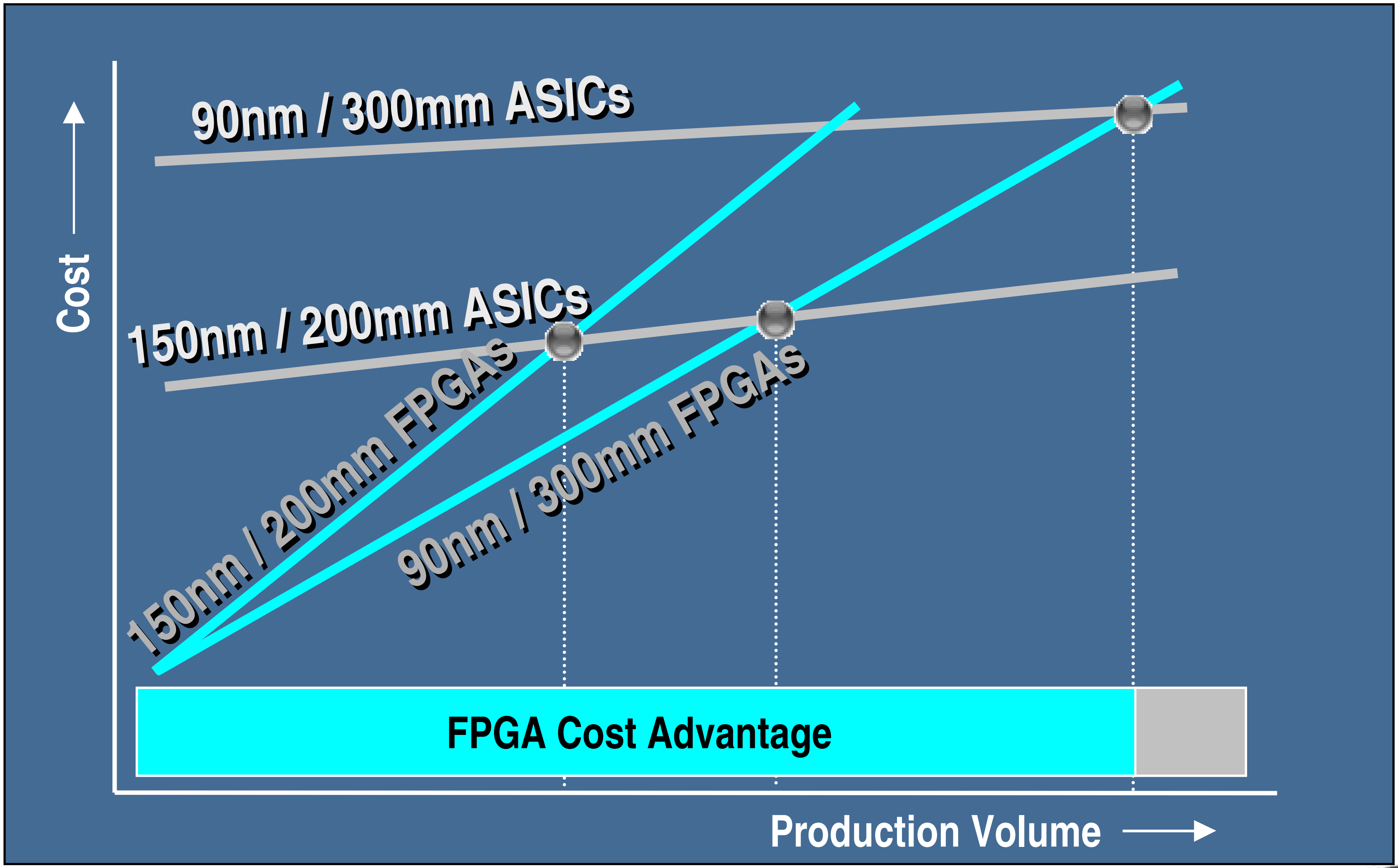


Source: Nick Tredennick

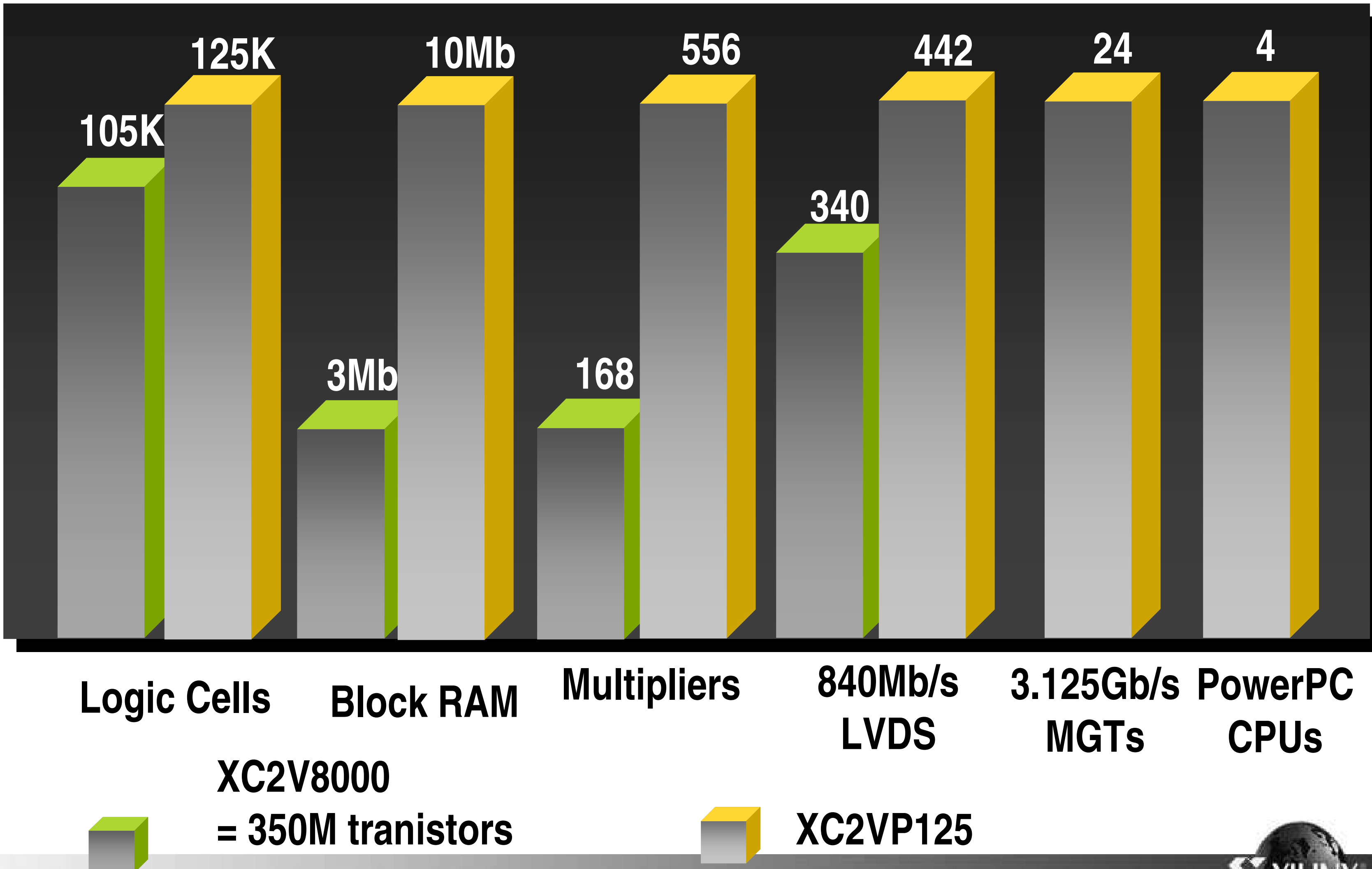
A decade of progress



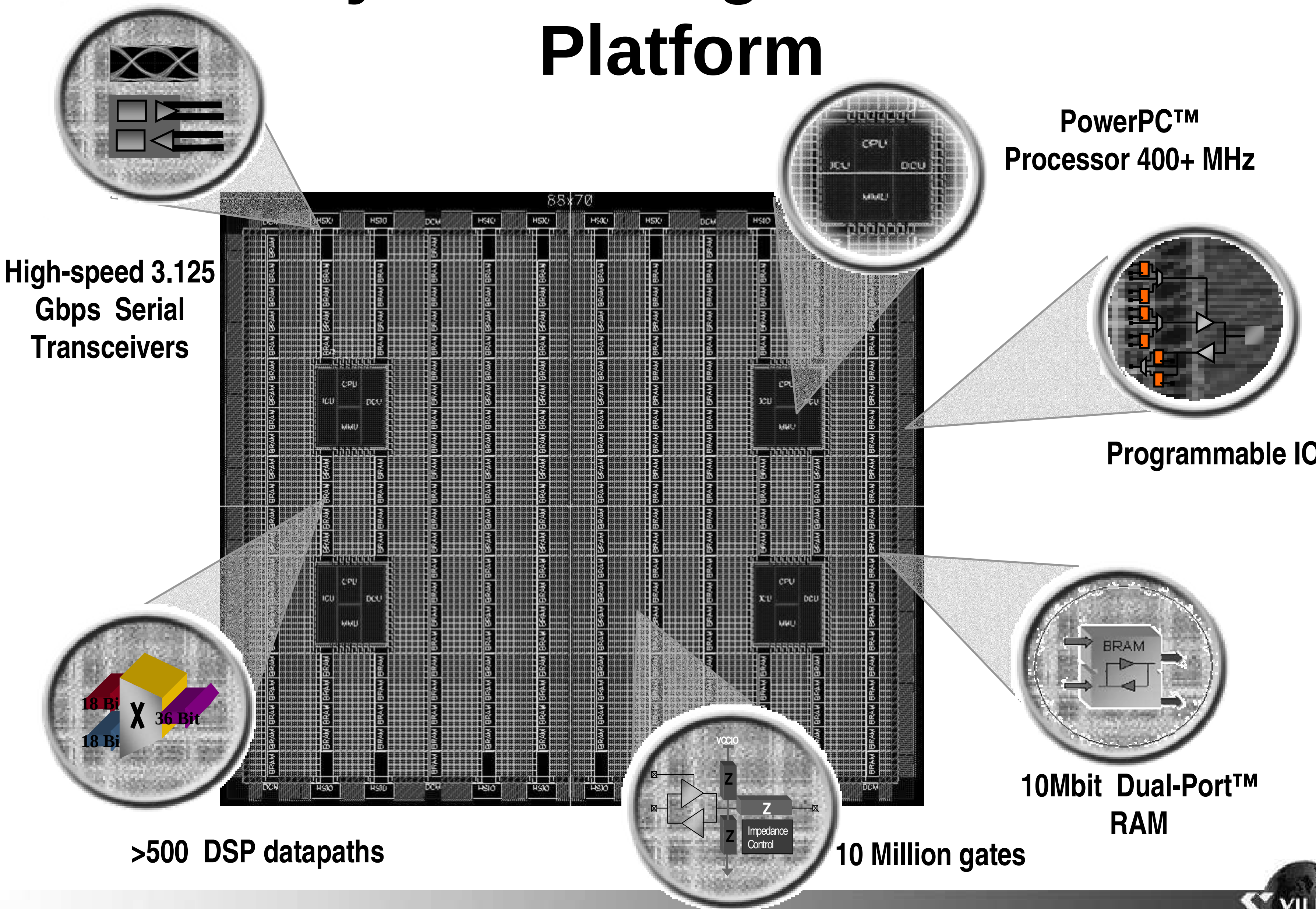
FPGA/ASIC Crossover Changes



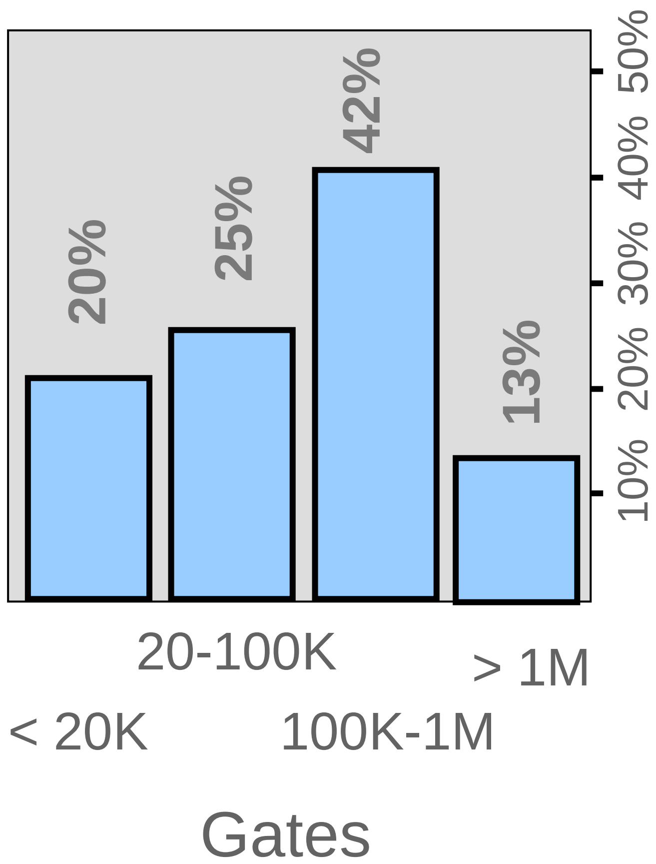
Where are we today

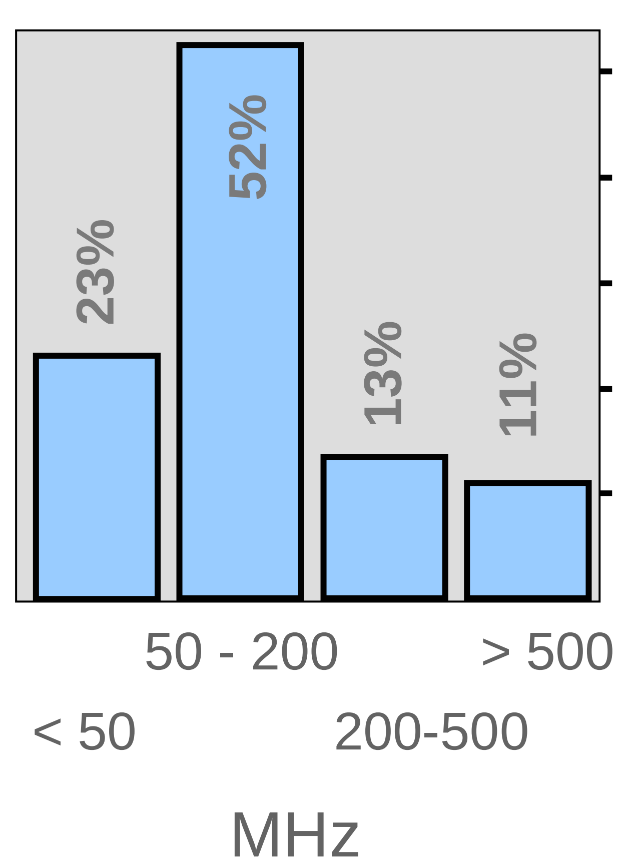


Today's Reconfigurable FPGA Platform



Design Capability: FPGAs Meet Most Requirements



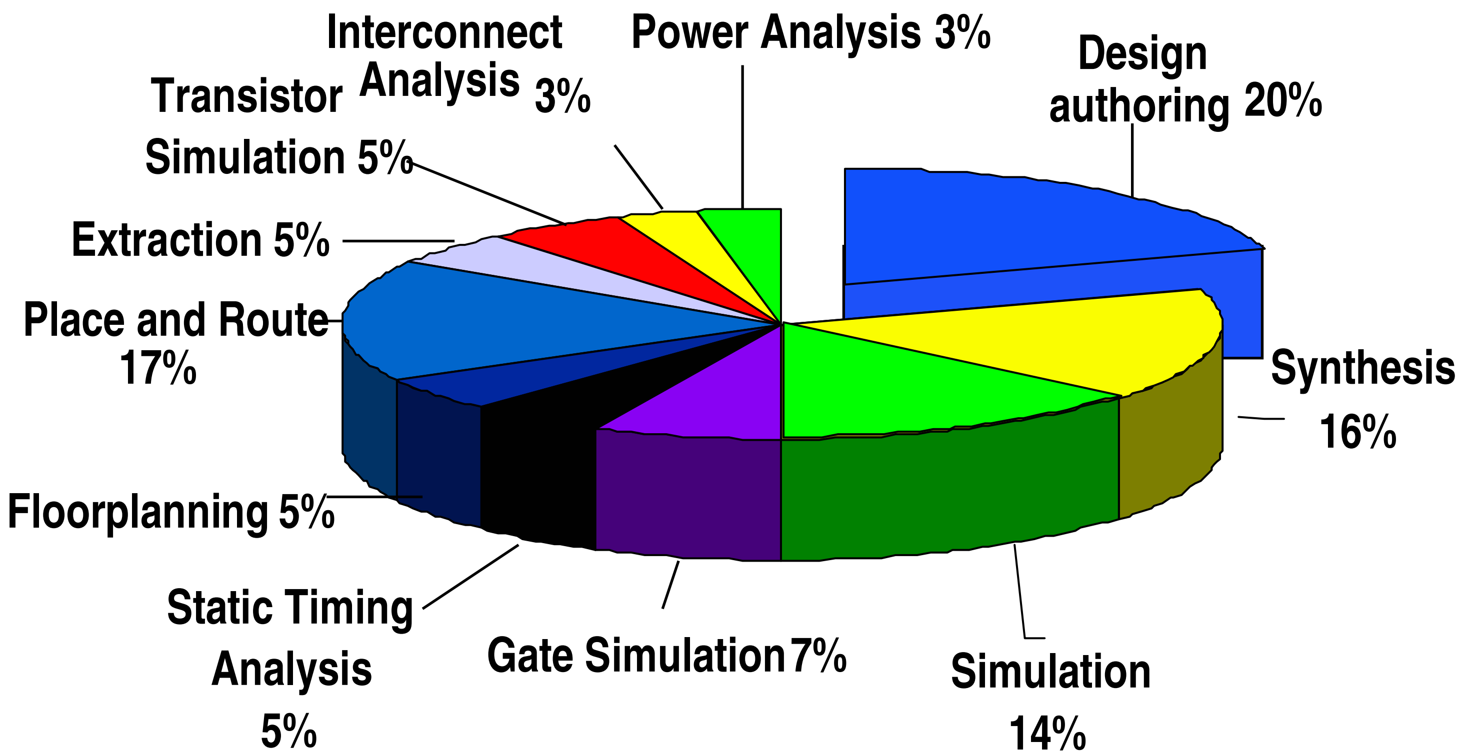


Source: Gartner Dataquest

FPGA Sweats the Details

- Xilinx programmable system platform gives designers the benefits of deep submicron
- Rather than focusing on getting the silicon to work, you can focus on getting the design to work

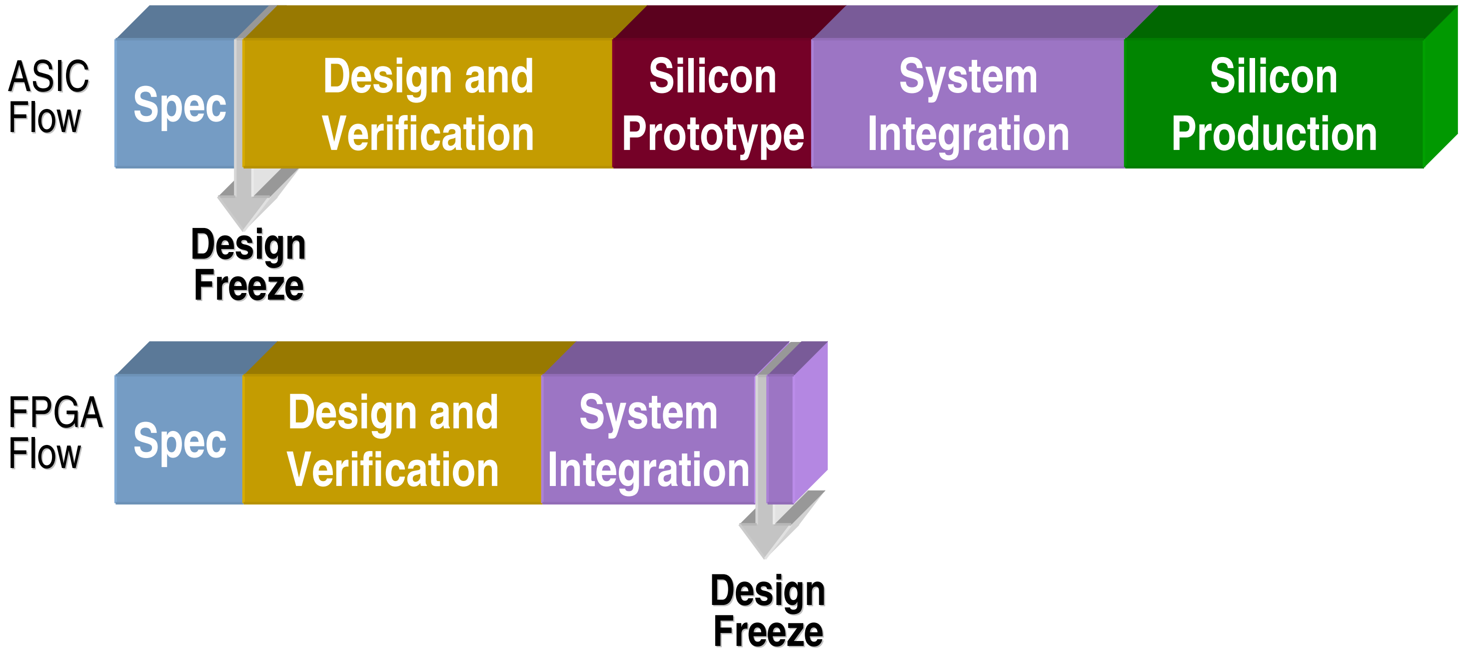
Complex ASIC Design
The Shrinking Window of Innovation



- Average iterations between design and layout = 20

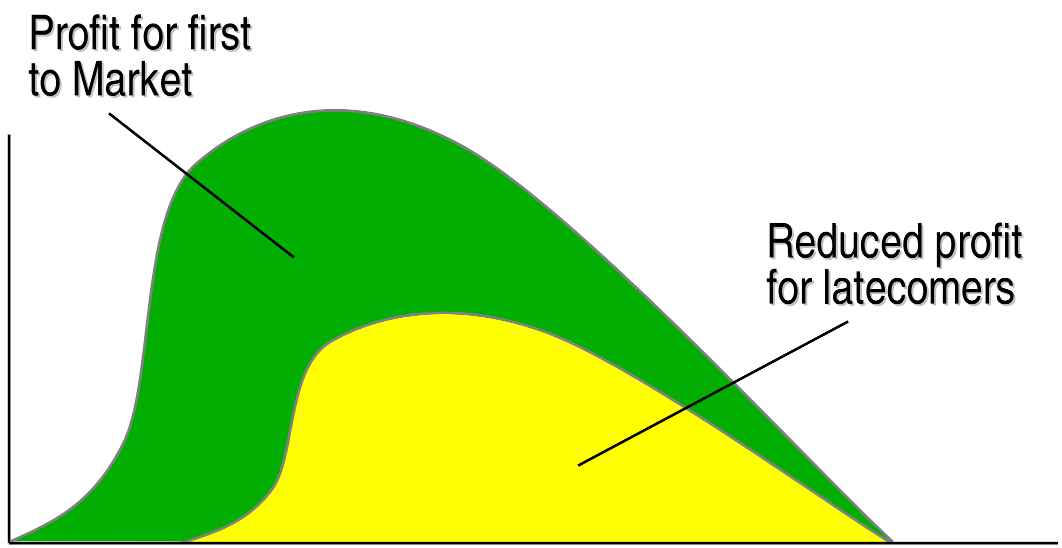
(Source Electronic Systems Jan 99)

Simpler/Faster Design Flows



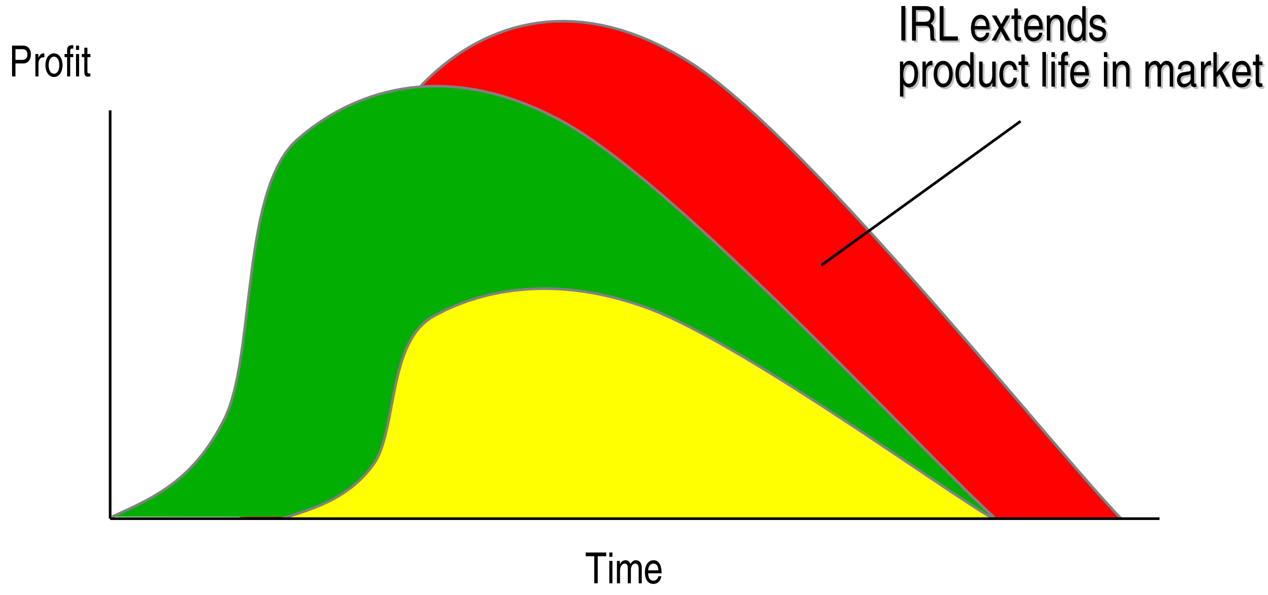
- 2:1 proven Time-to-Market Advantage
- No silicon design or verification steps
- More design flexibility through later design freeze

Today’s Product Lifecycle



- 37% of new digital products were late to market
- Entering the market first can result in up to a 40% greater total profit contribution over the product’s life vs. the #2 entrant

Today's Product Lifecycle



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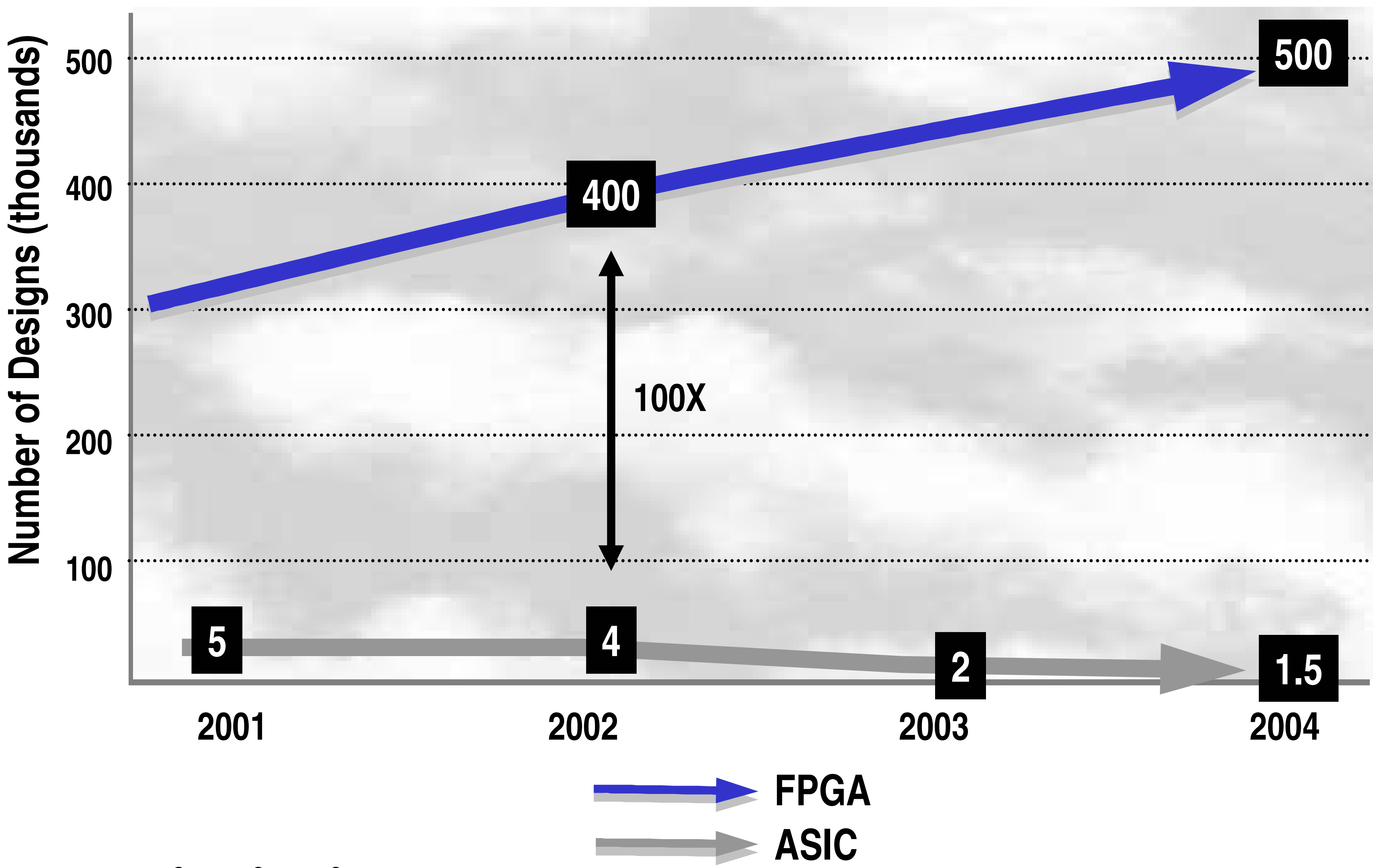
Design Starts: FPGAs Rule



Source: Gartner Group

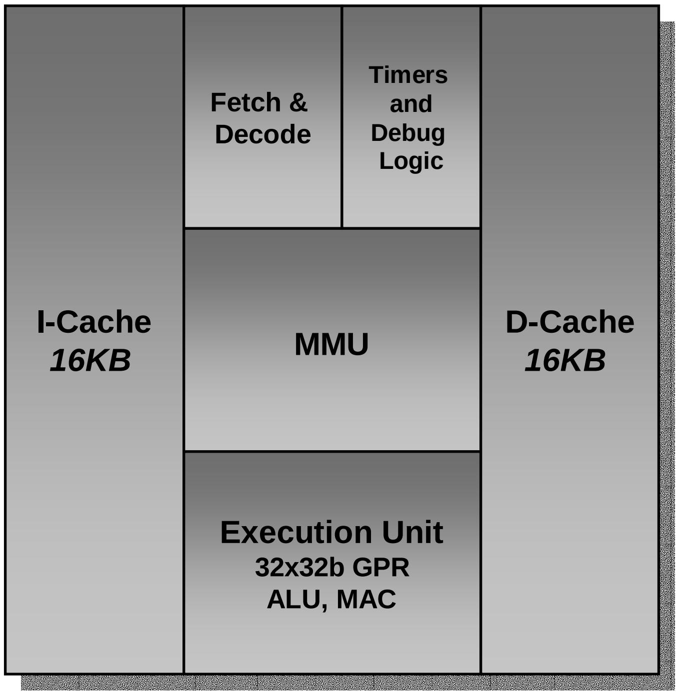
FPGAs rise to the system-level design challenge

- **PLATFORM**
- FPGA
  - Logic, Routing & I/O
- Soft CPUs
- Hard CPUs
- Bus hierarchies
- Memory hierarchies multipliers
- Gigabit I/Os
- RTOS, drivers, network protocol stacks, embedded real-time s/w

- **APPLICATIONS**
- Streaming multimedia
- Network processing
- Software defined radio
- Third+ generation base stations
- Storage area networks

- **DISCIPLINES & DESIGNERS**
- Systems architects, hardware & software engineers, DSP & communications specialists

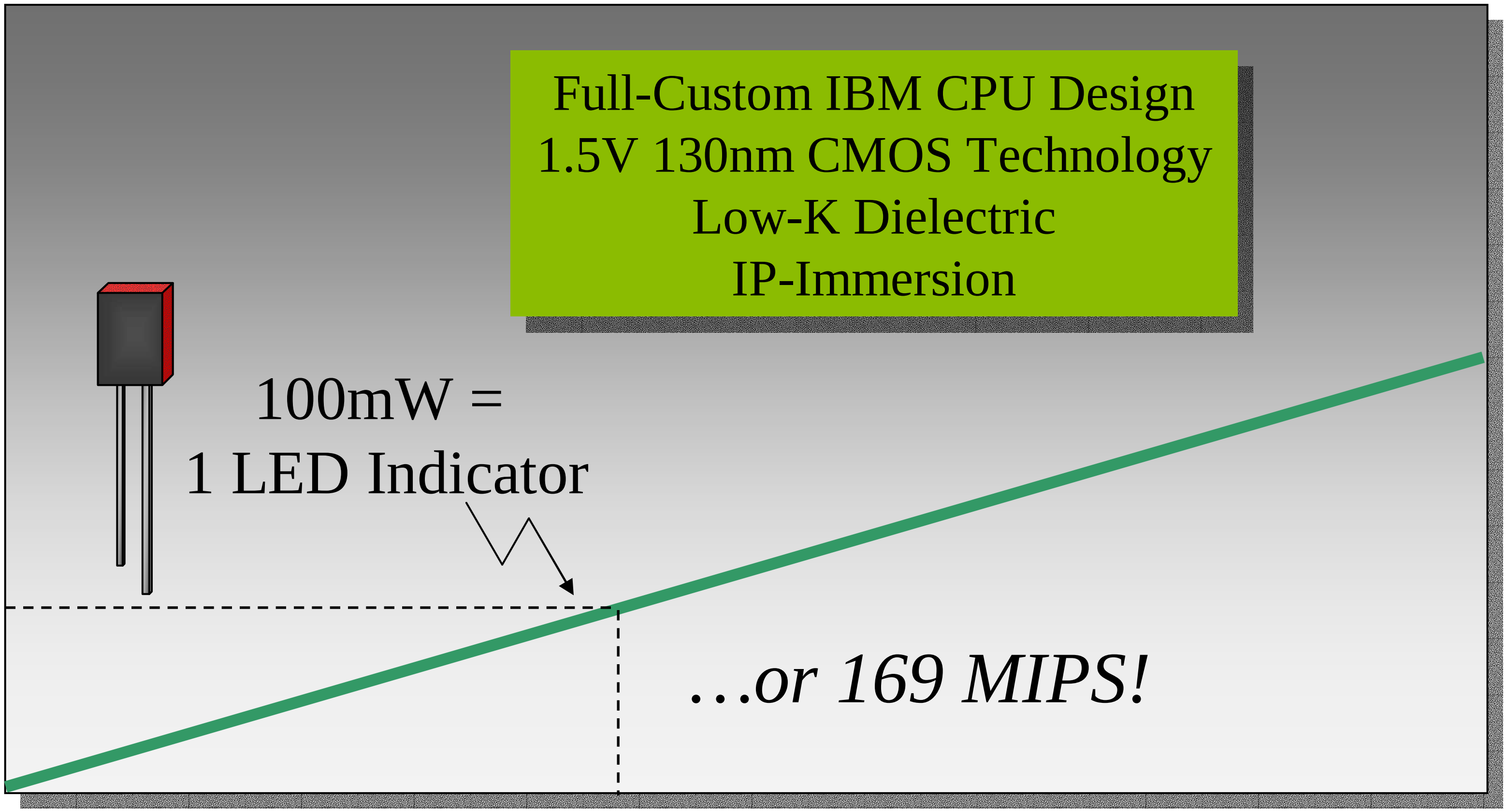
Towards programmable platforms



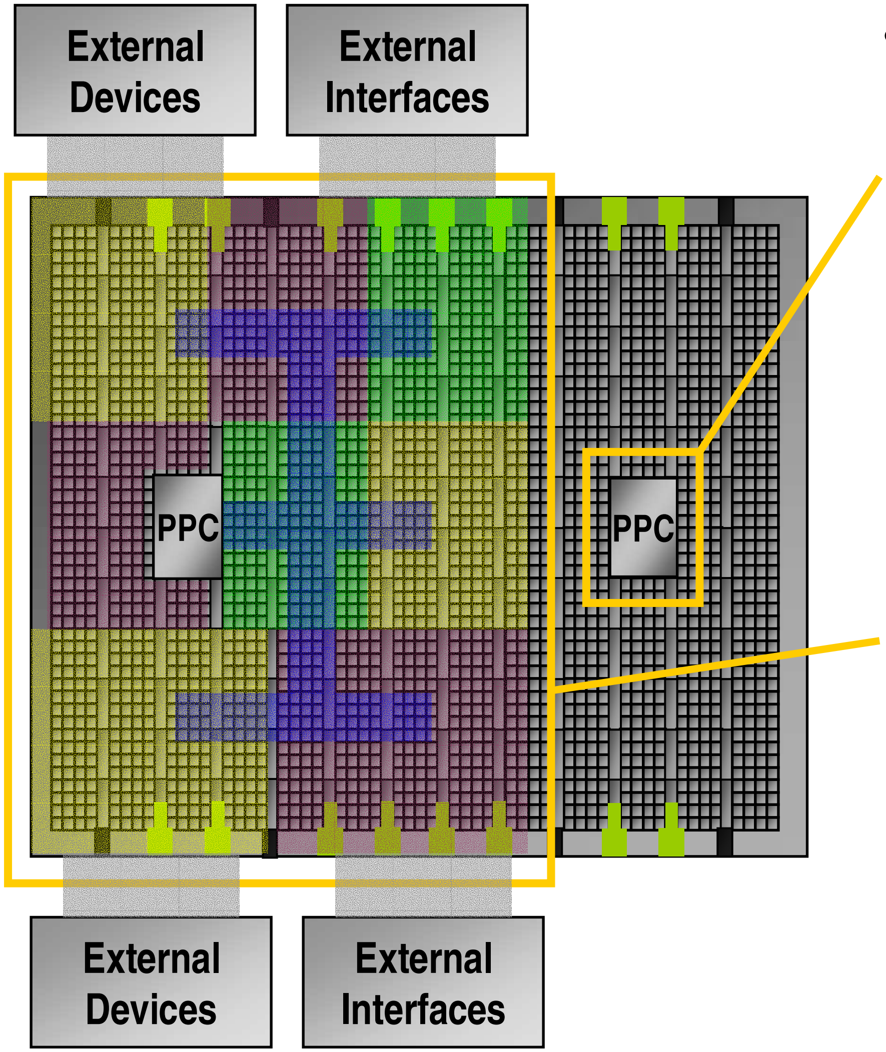
- 32-bit RISC CPU, Harvard Architecture
- 130nm CMOS with 1.5V Operation
- 456 Dhrystone MIPS at 300MHz
- 32 x 32-bit General Purpose Registers
- Hardware Multiply / Divide
- 5-Stage Execution Pipeline
- 16KB D-Cache, 16KB I-Cache
- Memory Management Unit (MMU)
- High-Bandwidth Interface to Logic
- Built-In Hardware Timers
- Built-In JTAG Debug and Trace support

3.8 sq mm = 1% of 2VP100

"Low PowerPC": 0.59mW/MIPS



System Architecture Options

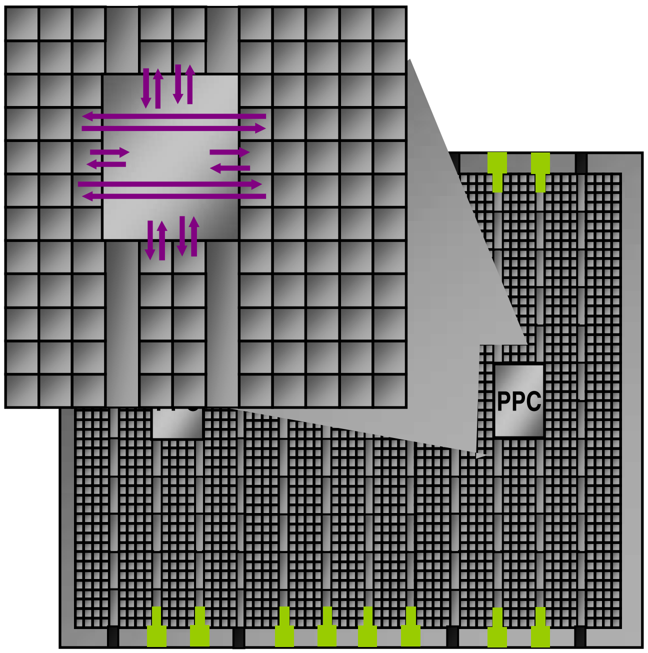


- "Logic-Centric Architecture"
  - PowerPC Executes Entirely out of Cache
  - No FPGA Logic, Memory, or I/O Used
  - 10-20 Pages of C-Code or More
  - Use as Complex Algorithmic Engine
    - Web Server
    - Encryption/Decryption
    - Packet Processor
- "CPU-Centric Architecture"
  - PowerPC forms Heart of Embedded System
  - On & Off-Chip Peripherals
  - External Interfaces
    - e.g. PCI, 3GIO, Gb Ethernet, ZBT SRAM
  - CoreConnect™ On-Chip Bus
    - *Ties System Together*
  - Peripherals implemented in FPGA Logic
  - Typically Runs Embedded OS

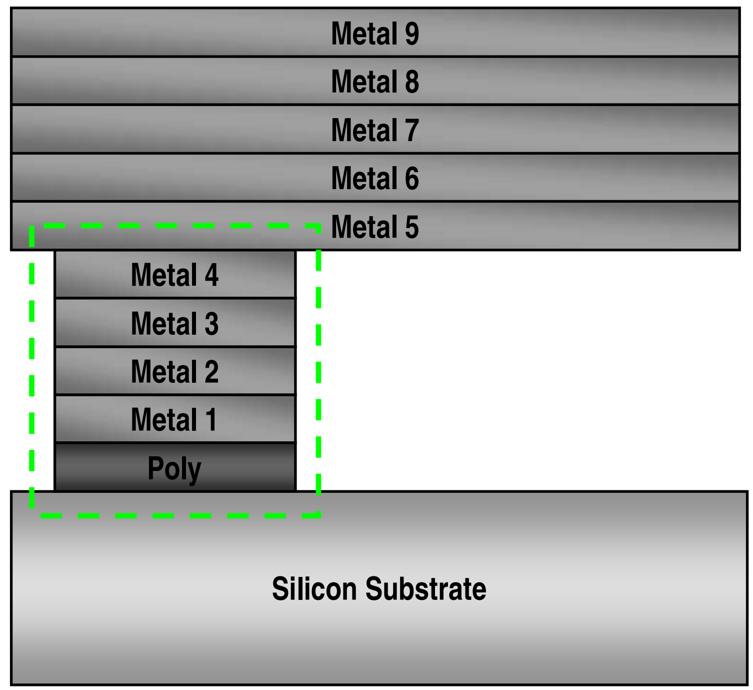
IP-Immersion

Embed multiple IP blocks of arbitrary shape with high-bandwidth connectivity to FPGA core logic, memory & I/O

Technologies Enabling IP-Immersion

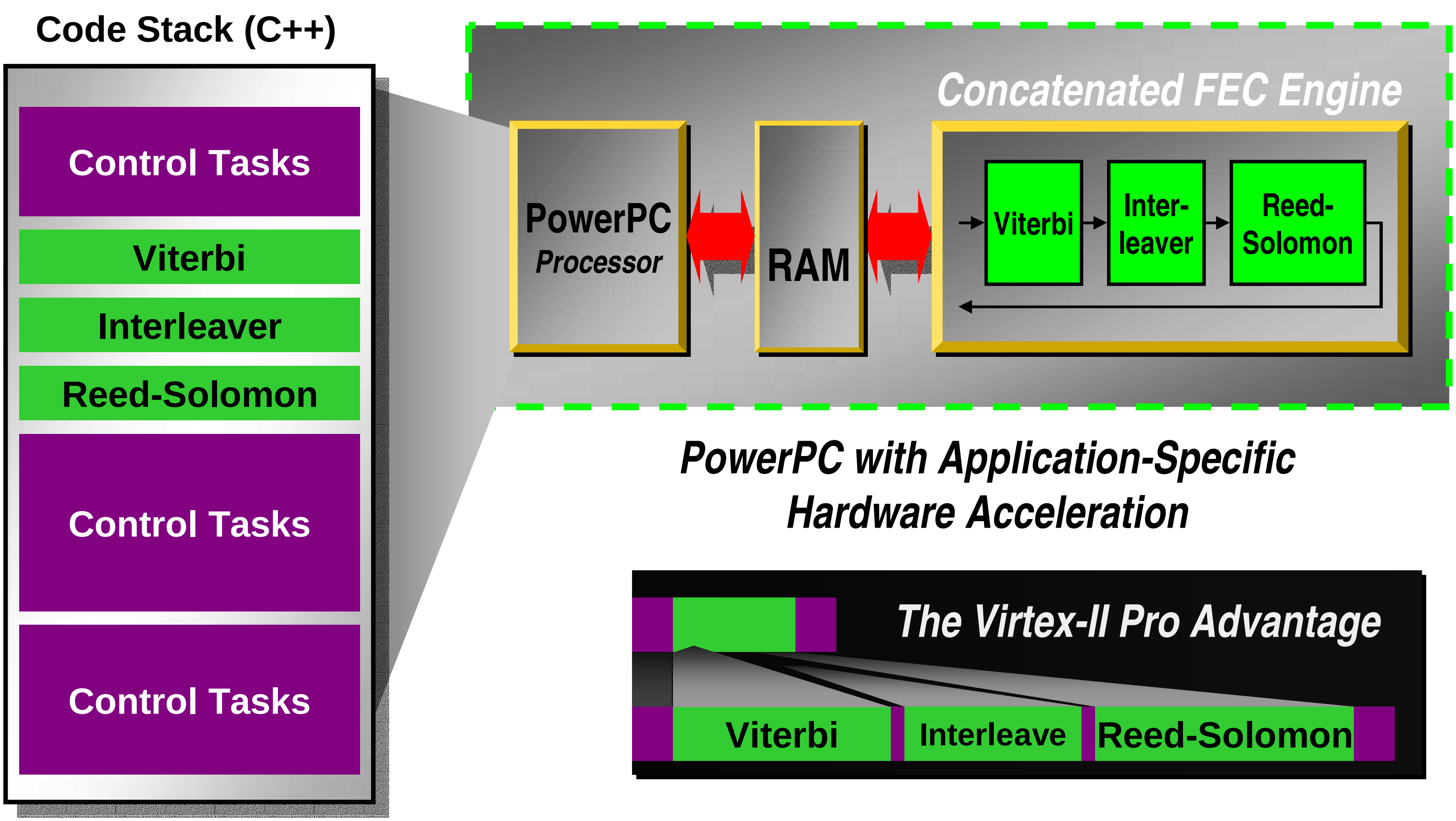


Active Interconnect™
Segmented Routing

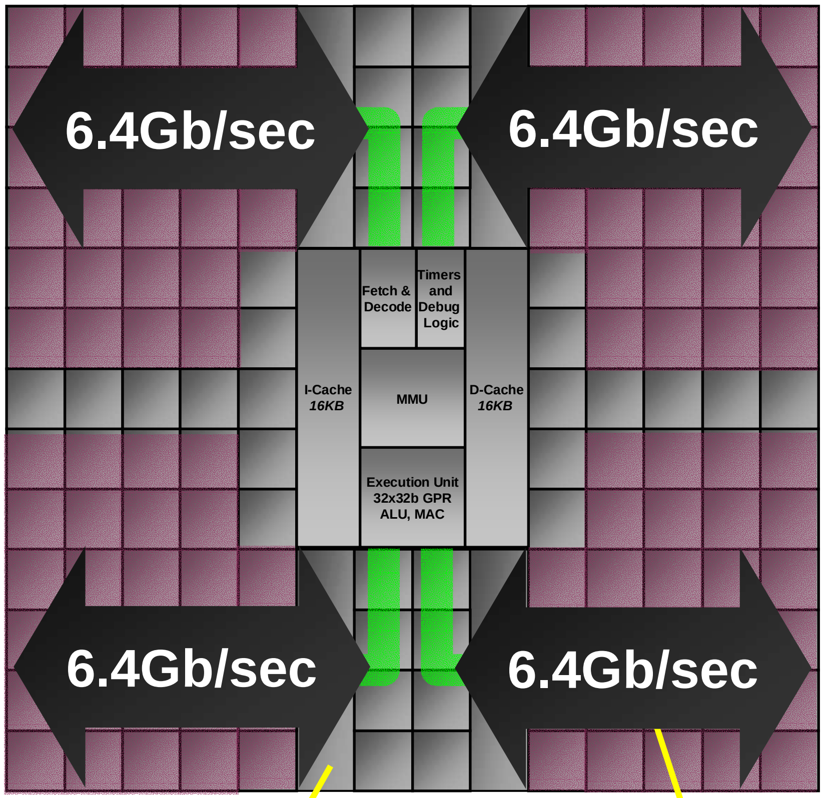


Metal 'Headroom'

HW acceleration



HW/SW Interfacing



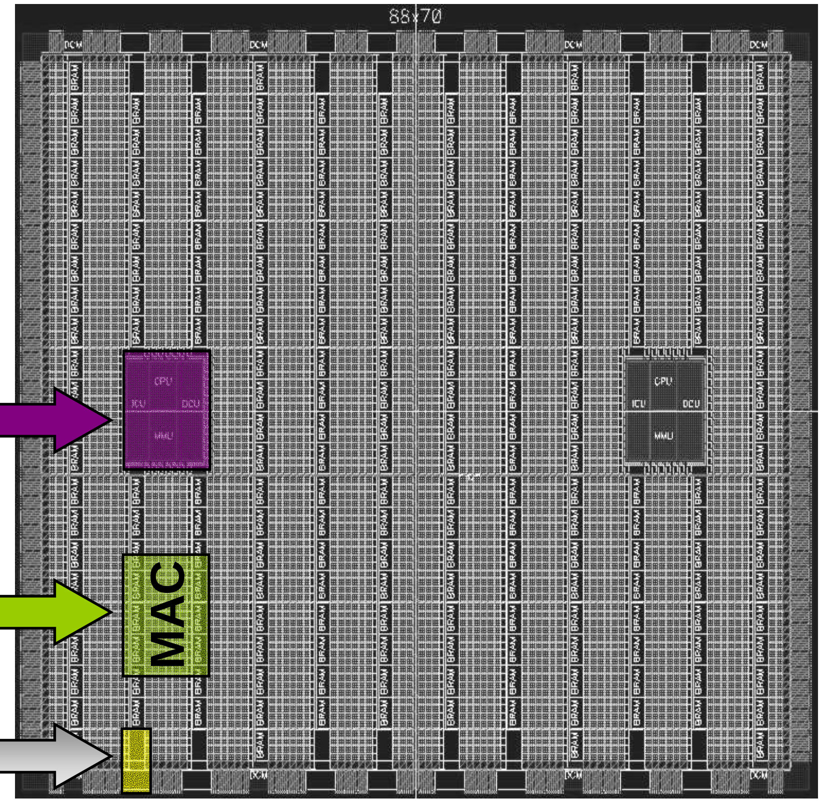
Acceleration Logic

BlockRAMs

- Provides Specialized Connectivity Between PowerPC & FPGA Logic
- Dual-Port BlockRAM Memory
  - CPU & Logic Each Own 1 Port
- High-Bandwidth
  - 6.4Gb/sec
- Low-Latency
- Non-Caching
  - Designed for Communications Data Processing
- Enables PowerPC & FPGA Logic to Work together on Complex Problems

Creating Complete Communications Solutions

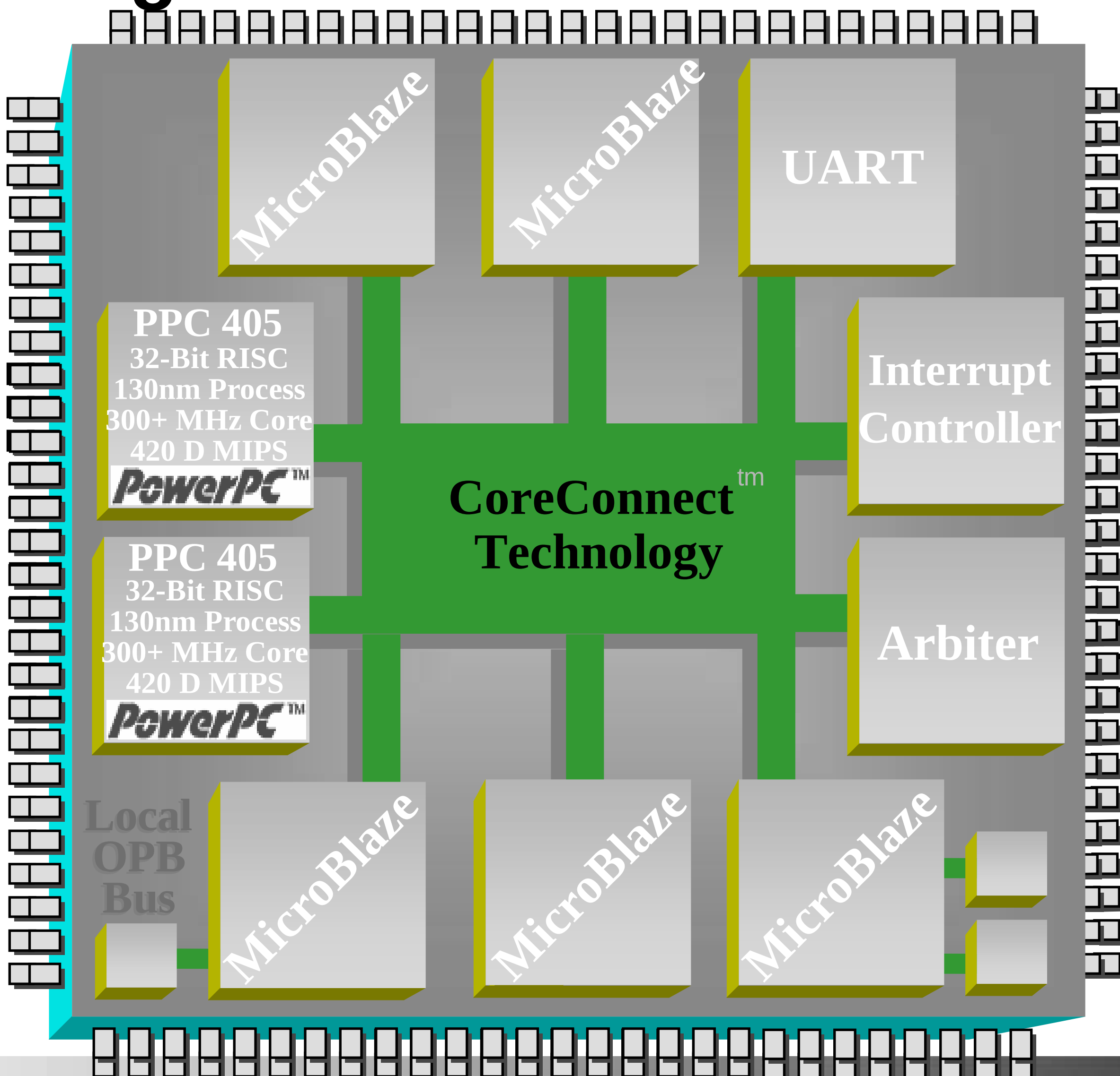
TCP/IP	
ftp telnet rlogin mail etc	**Upper Layers on PowerPC**
TCP IP	**TCP/IP Stack on PowerPC**
MAC	**Link Layer in FPGA Logic (GbE MAC)**
PHY	**RocketIO is PHY (1000Base-SX/LX)**



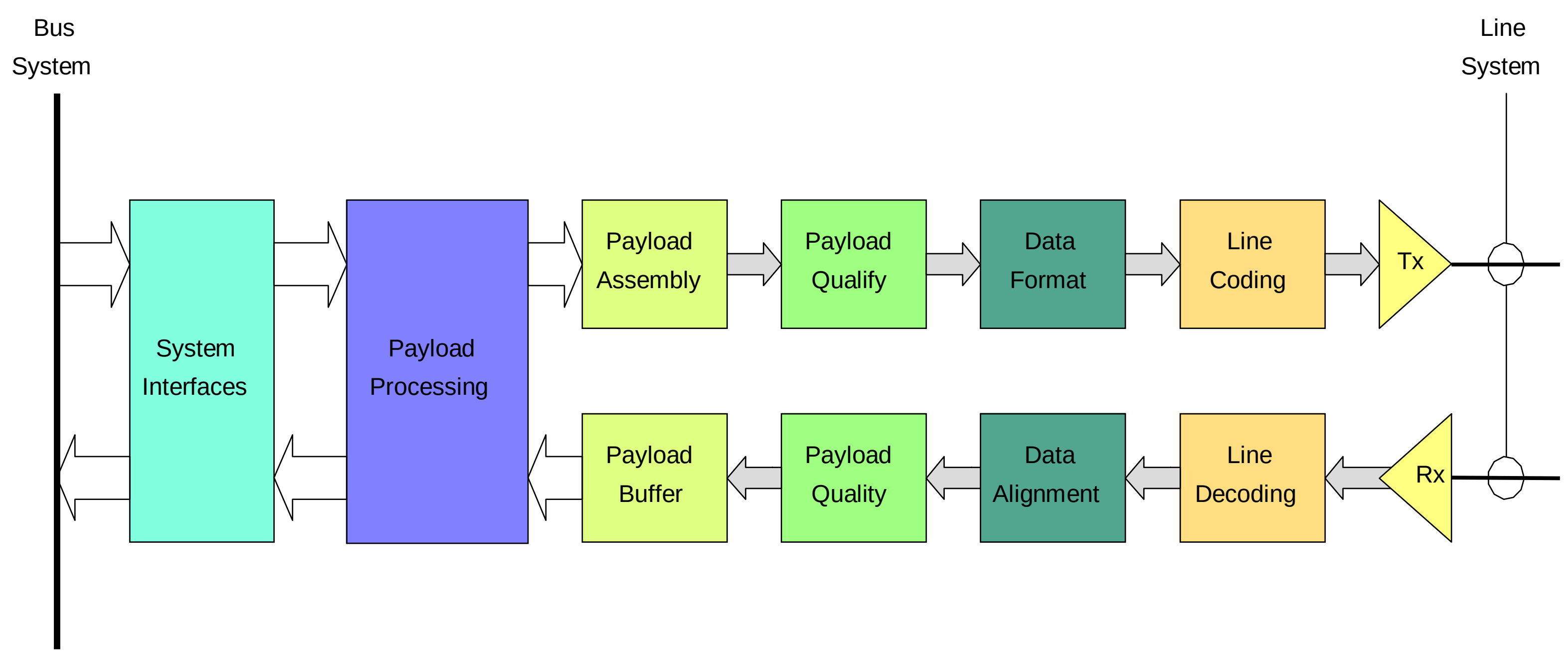
Gb Ethernet (1000BaseLX/SX/CX)

TCP/IP

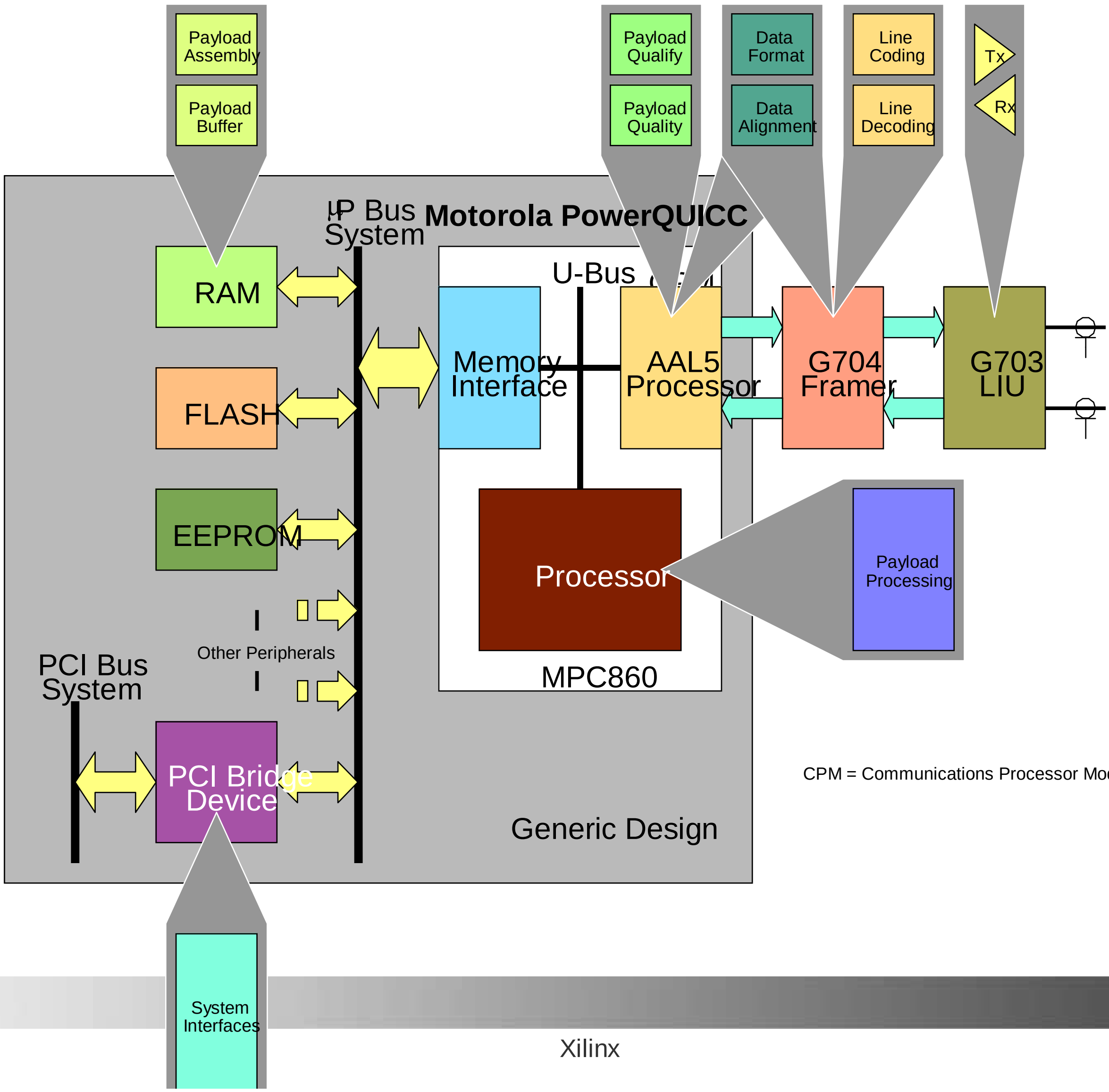
The MicroBlaze™
High Performance Soft CPU



System Exploration in Platform FPGA

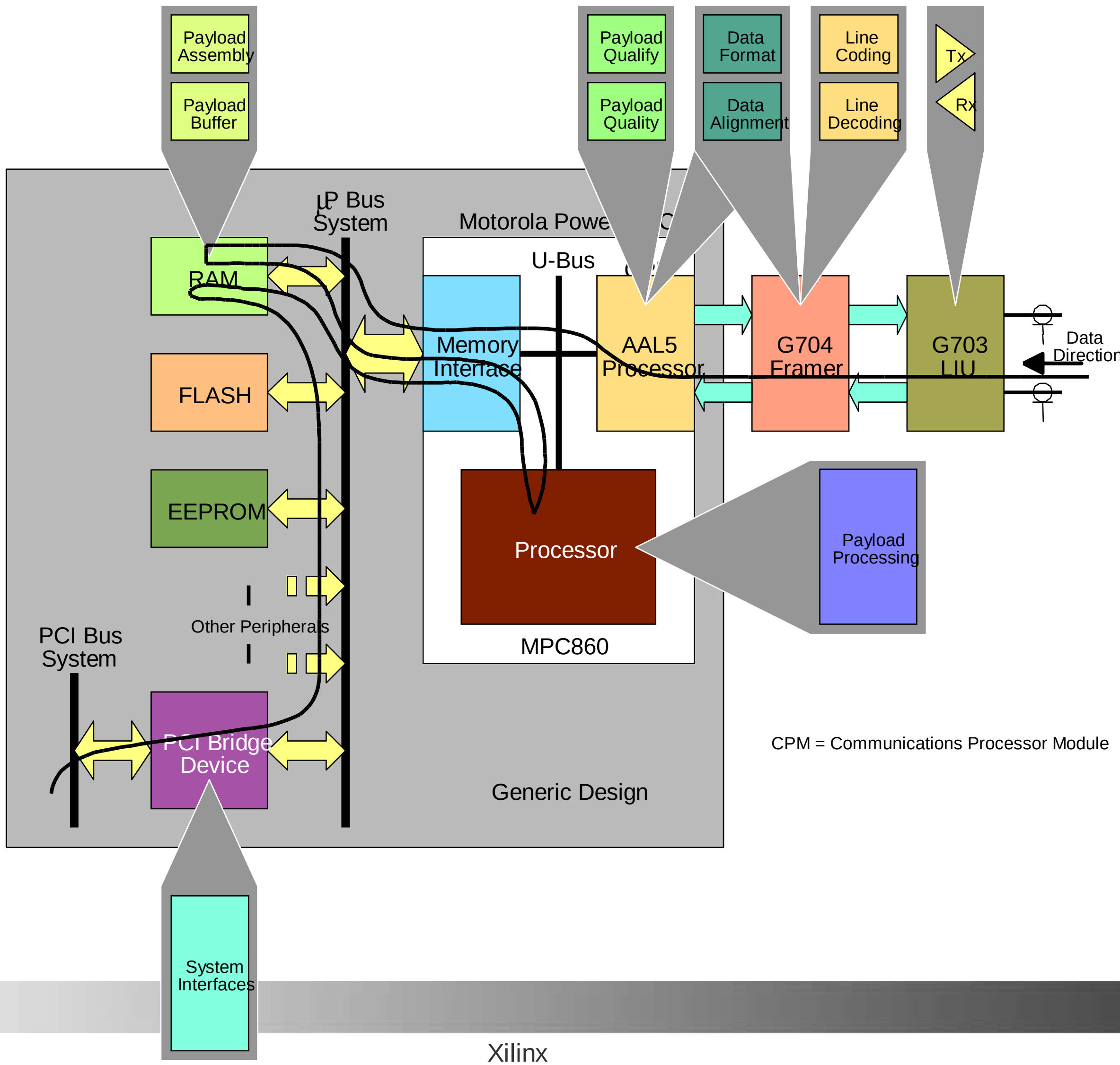


Traditional Architecture

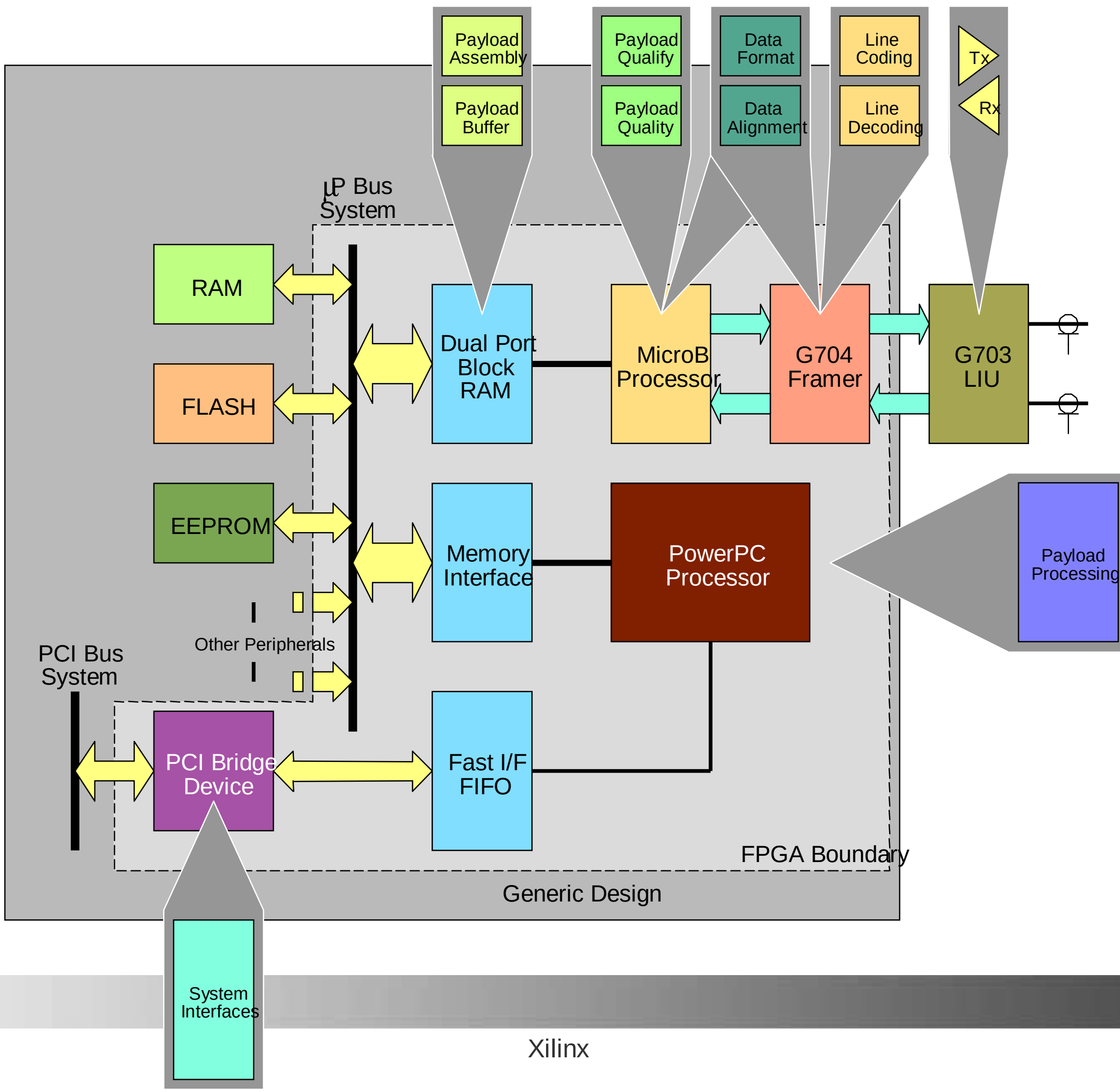


CPM = Communications Processor Module

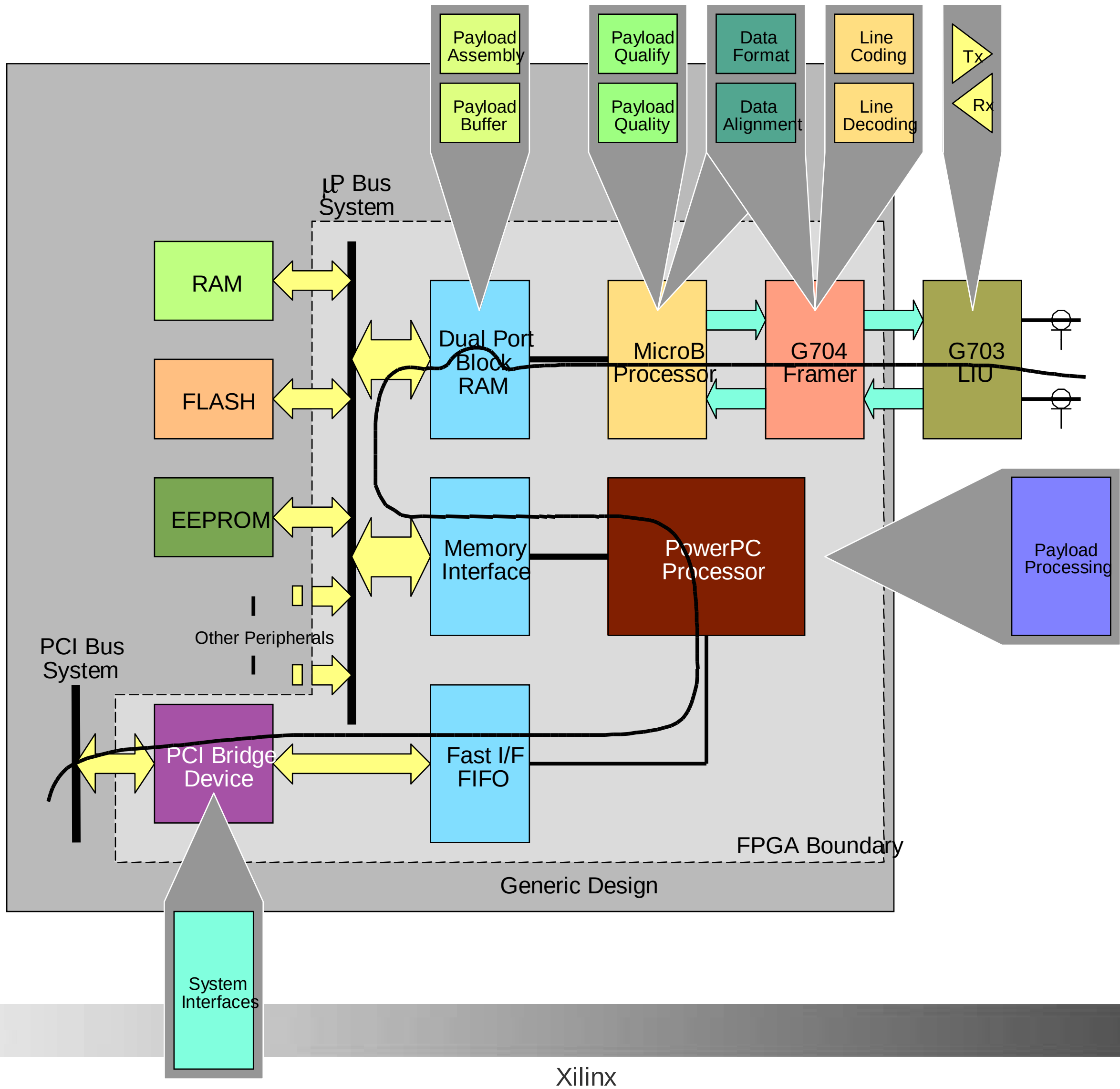
Traditional Architecture



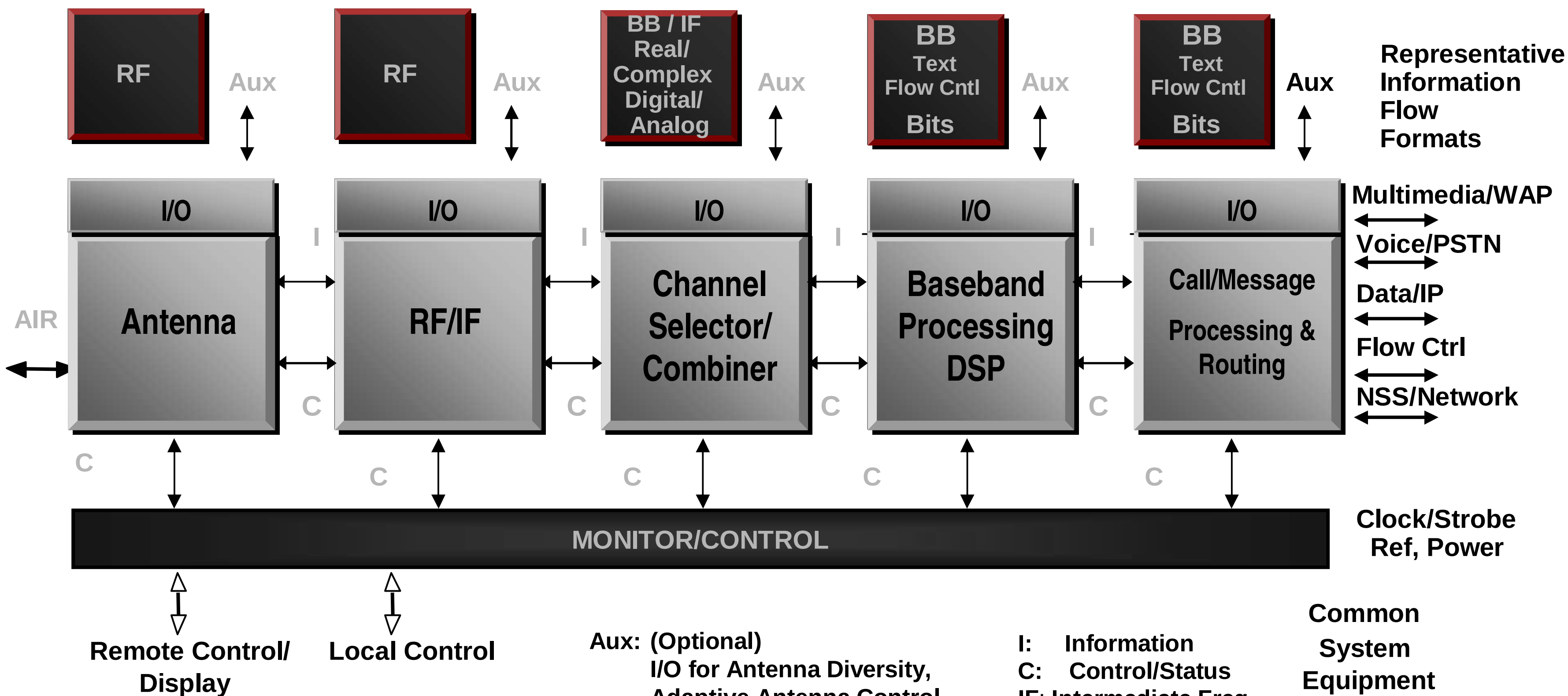
Optimized Architecture



Optimized Architecture



Software Radio Architecture



Aux: (Optional)
I/O for Antenna Diversity,
Adaptive Antenna Control
Selective Encryption, etc.
Link Processing Control
PSTN: Public Service Telephone
Network

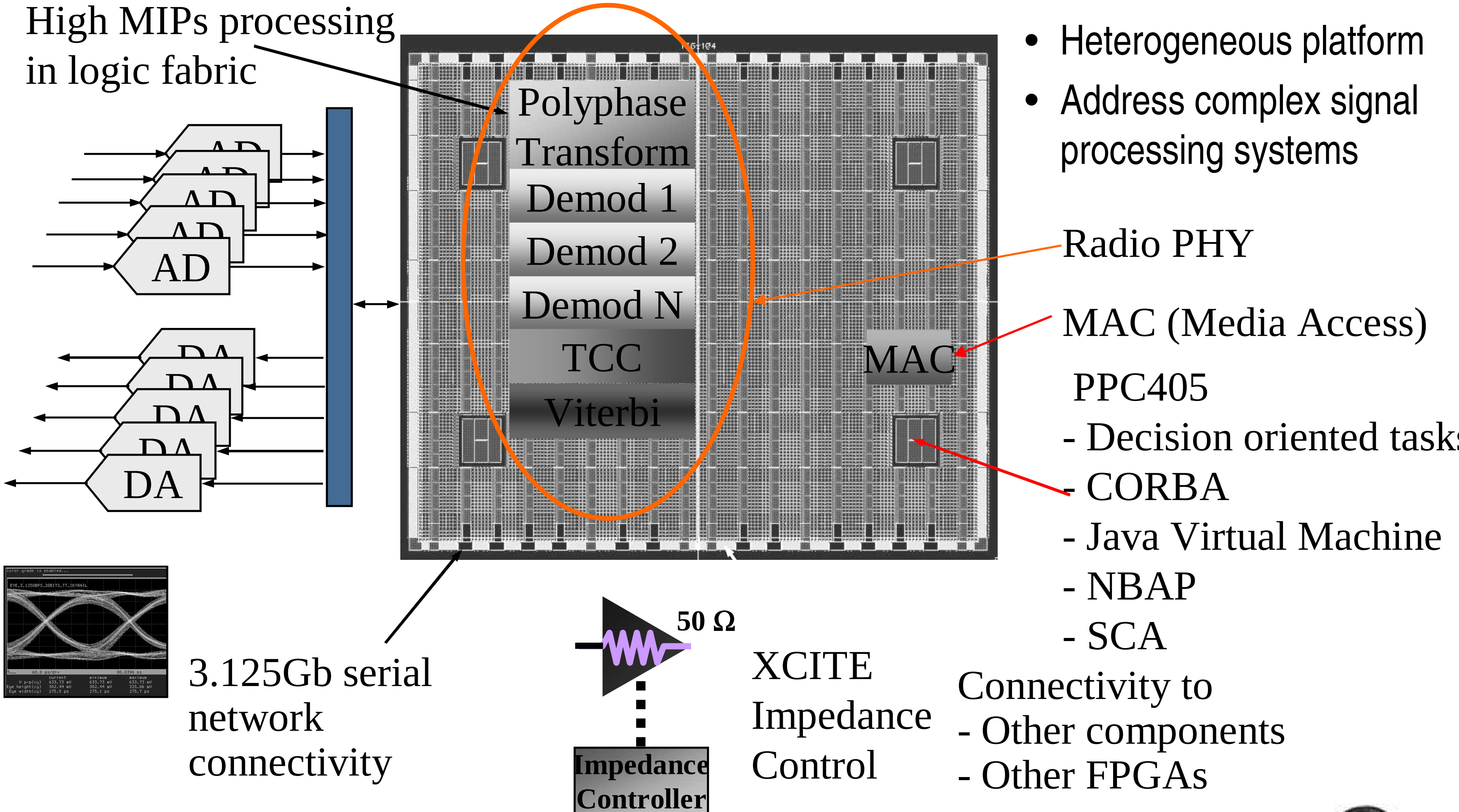
I: Information
C: Control/Status
IF: Intermediate Freq
NSS: Network
Switching
System
BB: Baseband

Common
System
Equipment

Ext. Ref

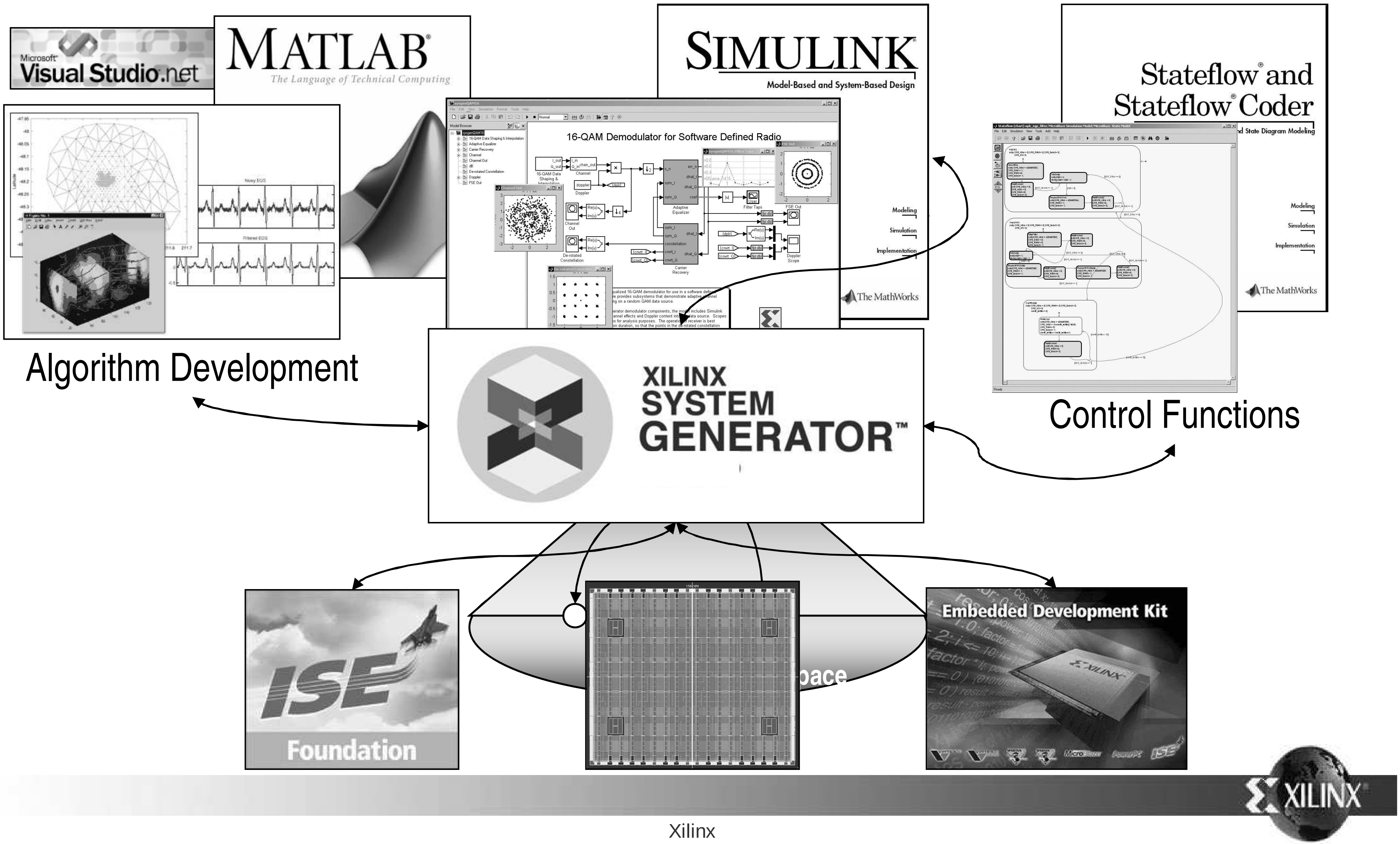
Re-invent the Signal Processing Platform

- Heterogeneous platform
- Address complex signal processing systems



Connectivity to
- Other components
- Other FPGAs

Platform-Based Design

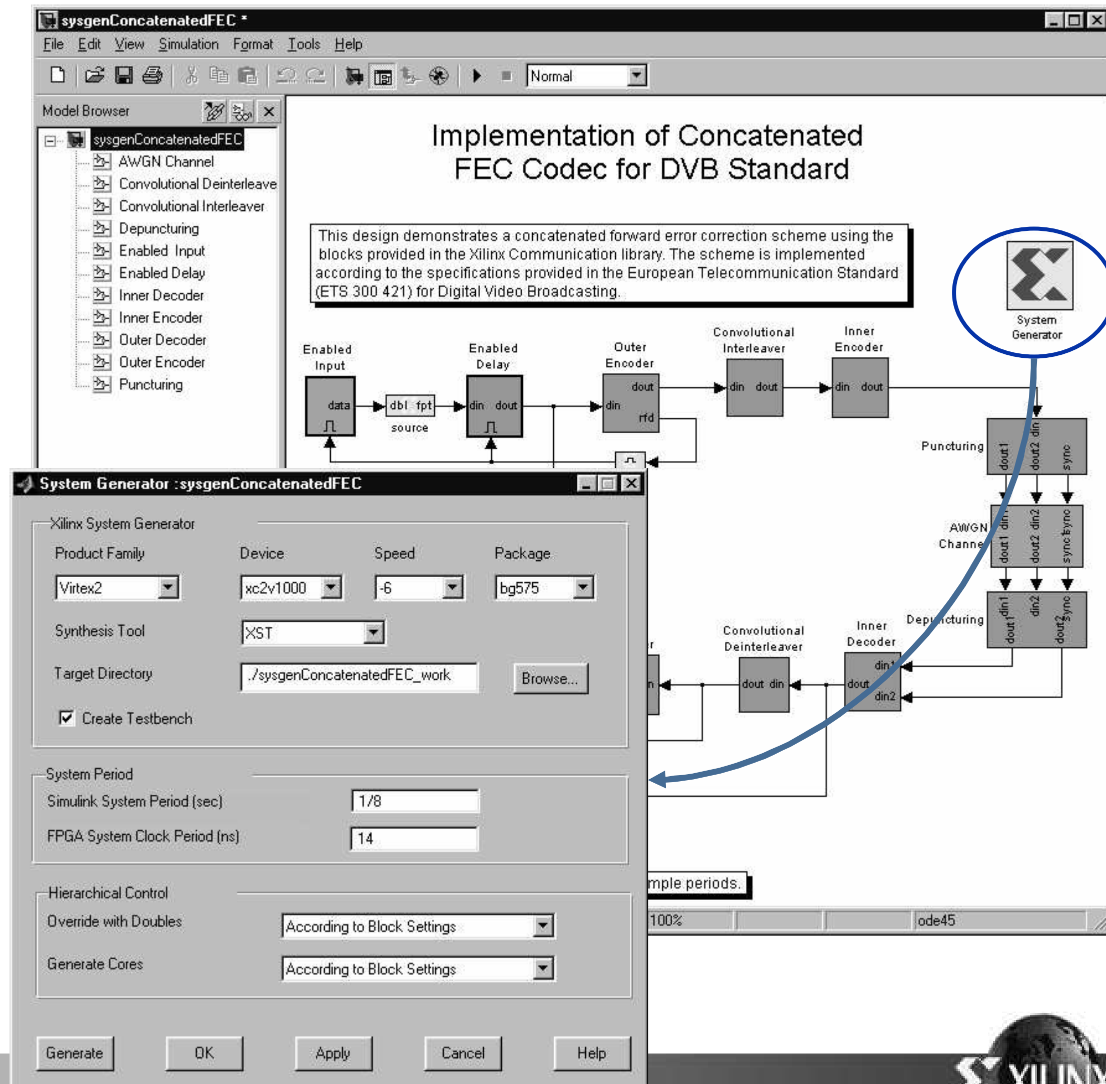


System Generator for DSP

- Visual data flow paradigm
- Polymorphic block libraries
- Arbitrary precision fixed-point
- Bit and cycle true modeling

- Seamlessly integrated with Simulink and MATLAB
  – Test bench and data analysis

- Automatic code generation
  – Synthesizable VHDL
  – IP cores
  – HDL test bench
  – Project and constraint files



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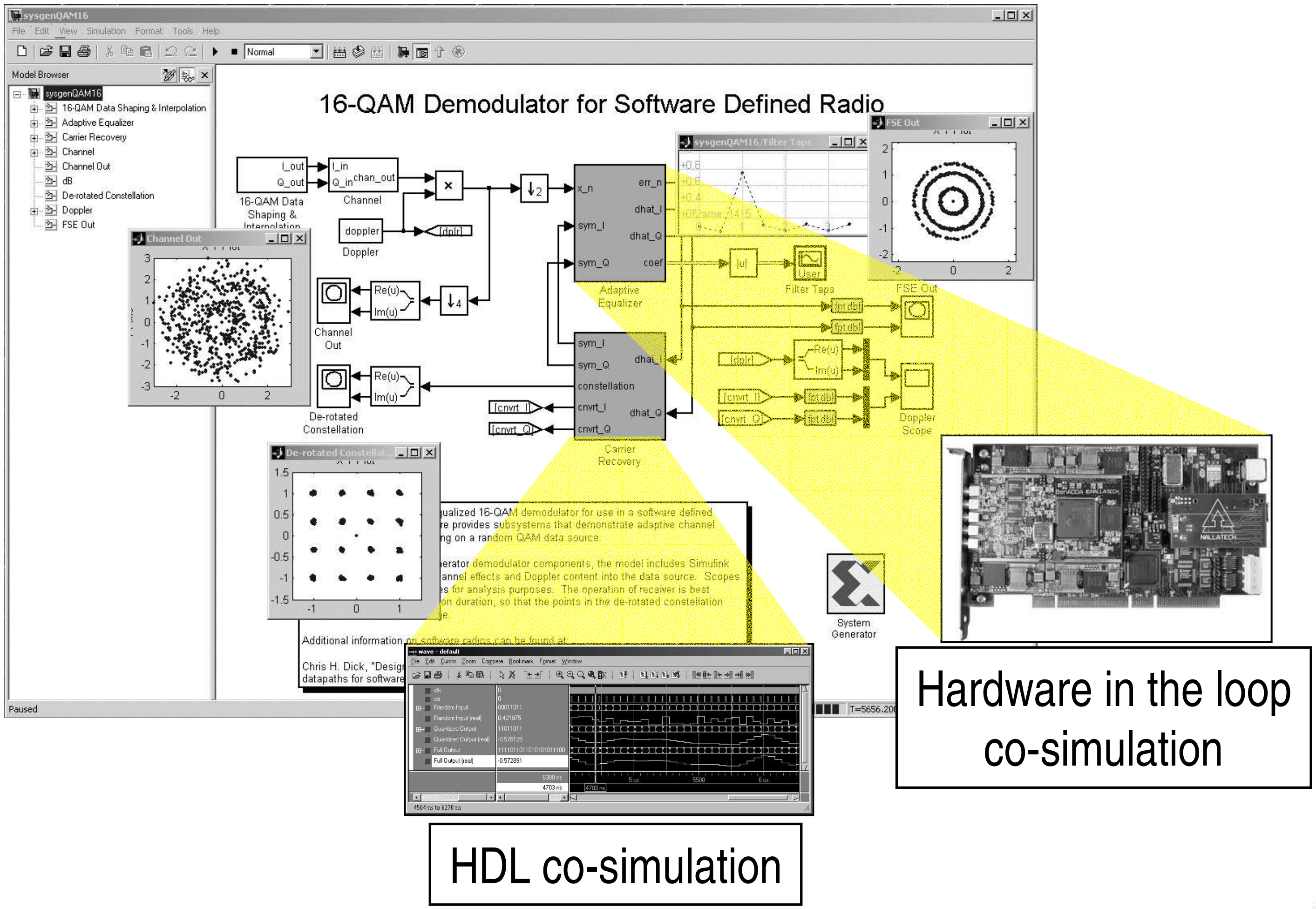
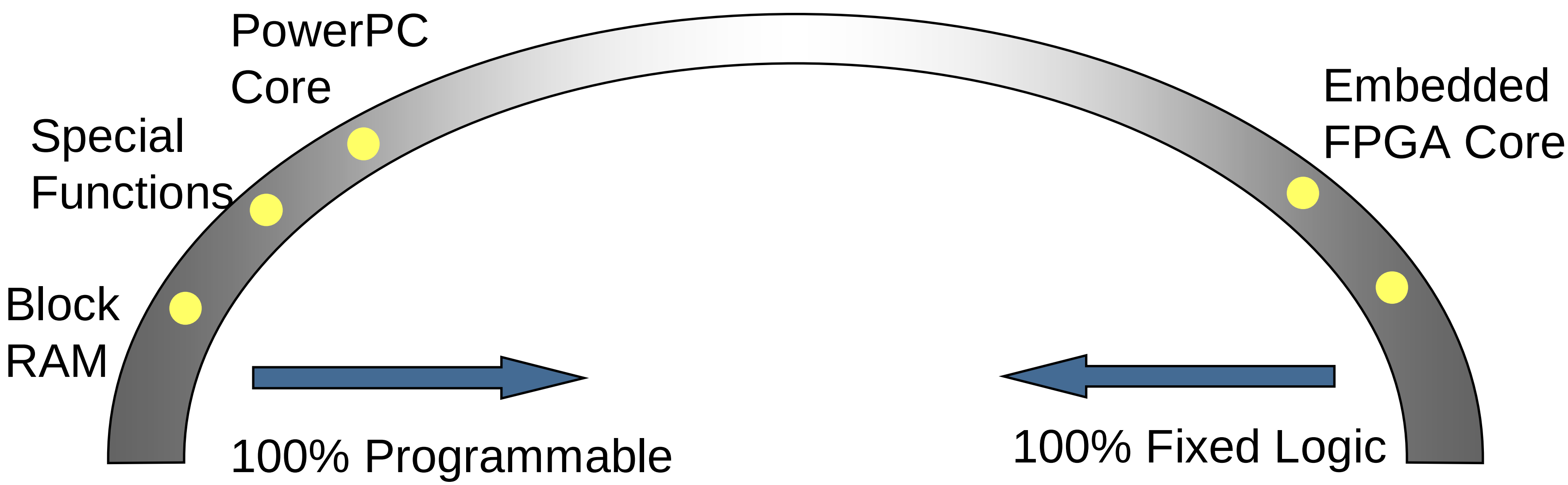
Heterogenous Implementation



Where We Are Going
FPGA 2005

Process Technology	65 nm, 10 layers Cu
Transistors	1B
Logic Cells	200K
Block RAM	15Mb
IO Speed	10Gb/s
Embedded Processors	Many
Embedded DSP Blocks	Very Many
Embedded Mixed Signal Blocks	Yes

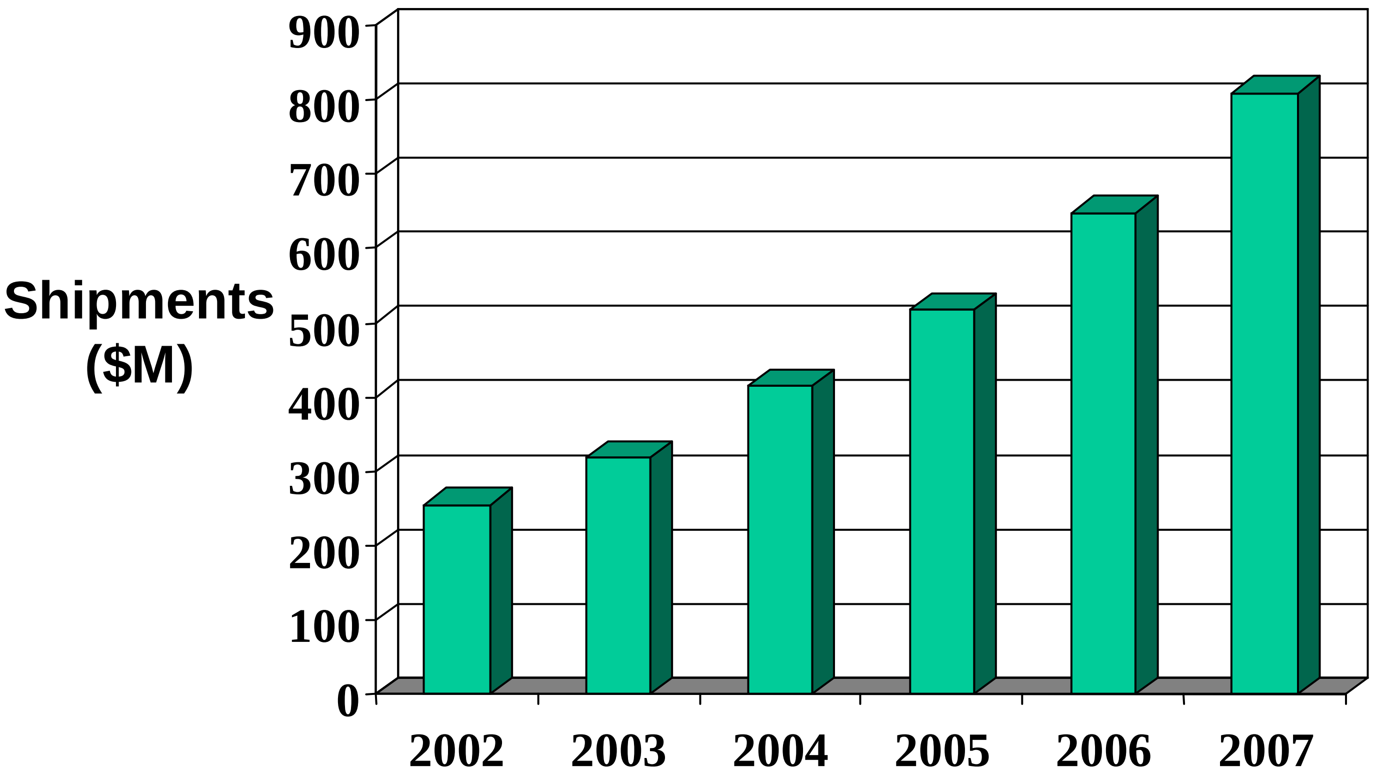
Combining the Best of FPGA and ASIC



Traditional FPGA Market

- Flexible, but expensive

Reconfigurable Chips for Digital Signal Processing
(FPGAs, PLDs, Reconfig. Data Paths)

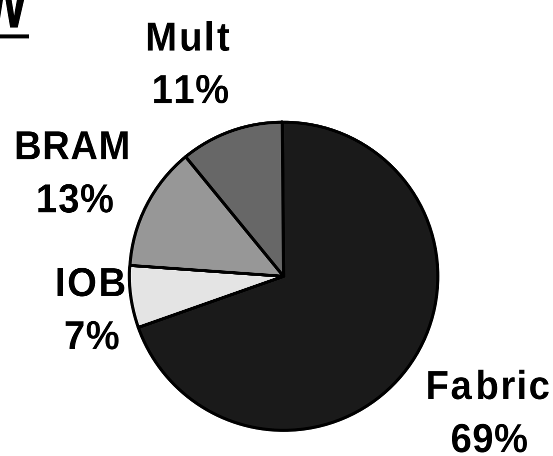


2002-2007 CAGR of 26.0%

Source:
Forward Concepts
February, 2003

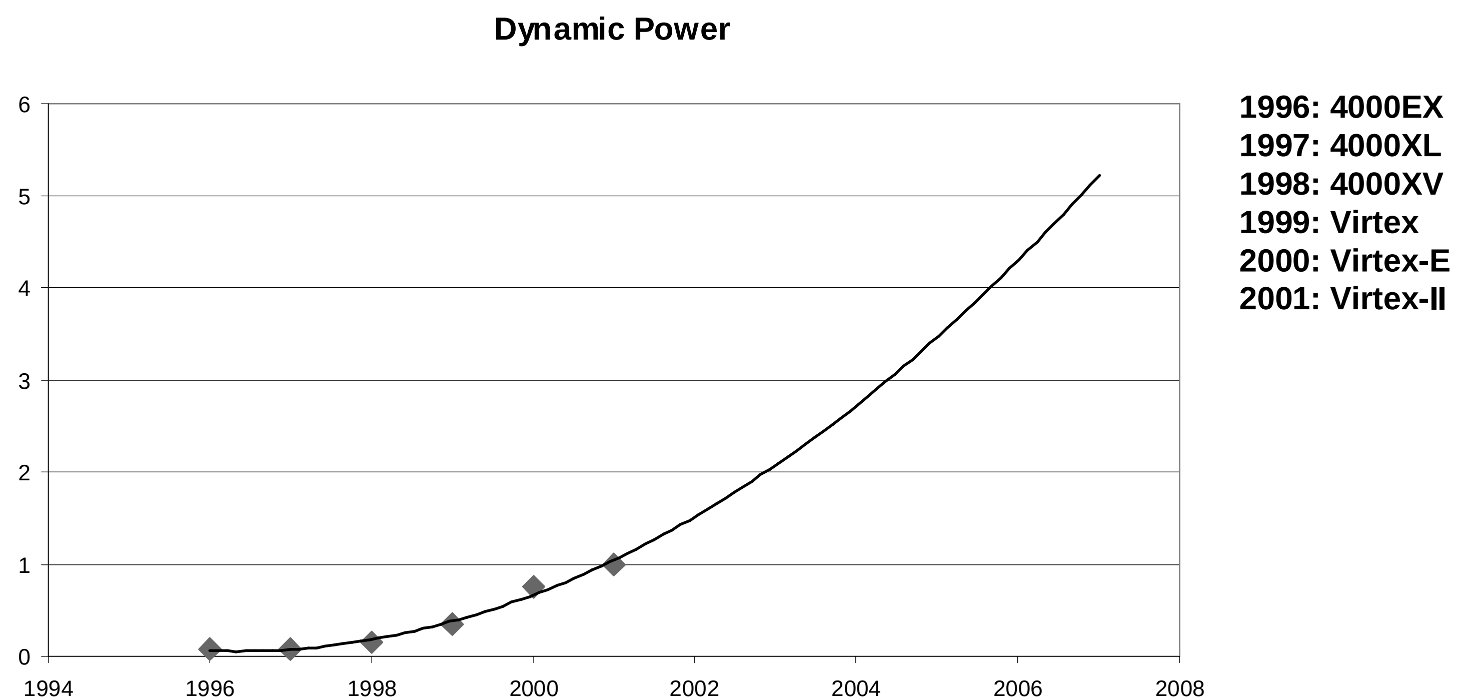
Power Analysis

- Typical design
  - 5.9uW/CLB/MHz [FPGA00]
  - Fabric power is ~69% of total power
  - 2V6000 = 5.9uW/CLB/MHz · 8448CLBs · 100MHz ÷ 69% = **7.5W**



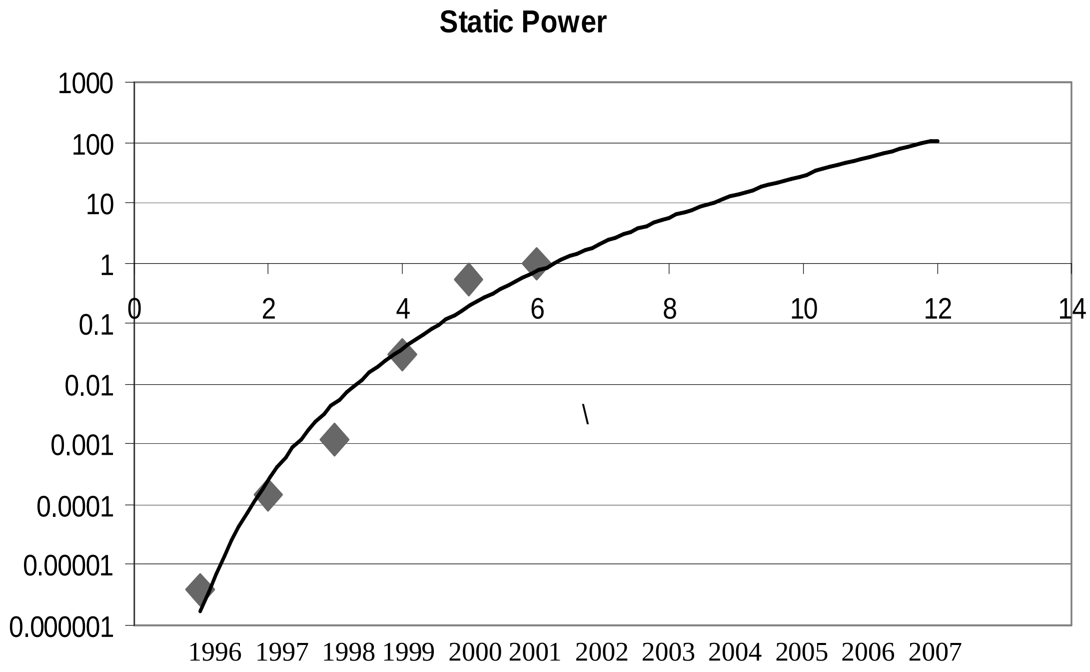
Dynamic Power

- Normalized to 2001
  - Best fit is a quadratic trend line
  - Predicts 5X by 2007

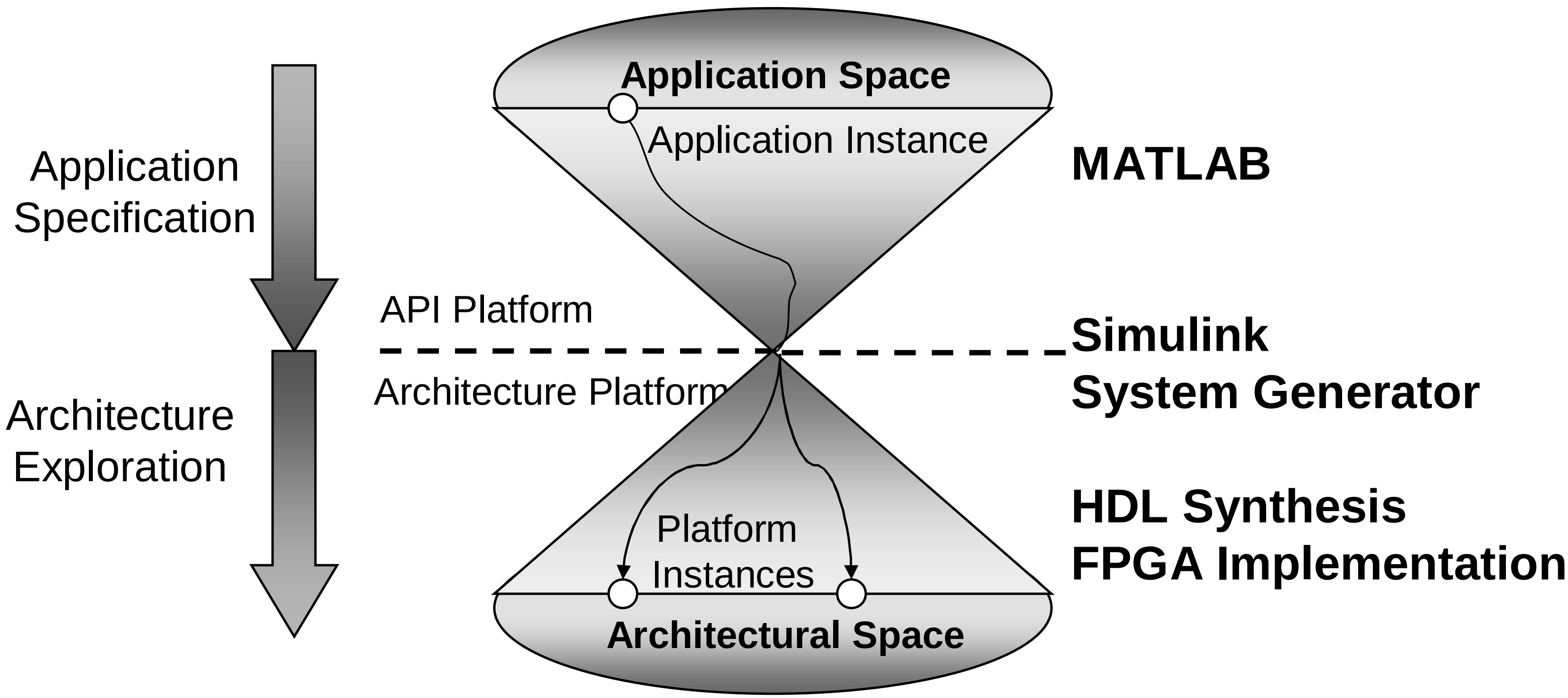


Static Power

- Normalized to 2001
  - Best fit is a power trend
  - Predicts 100X by 2007

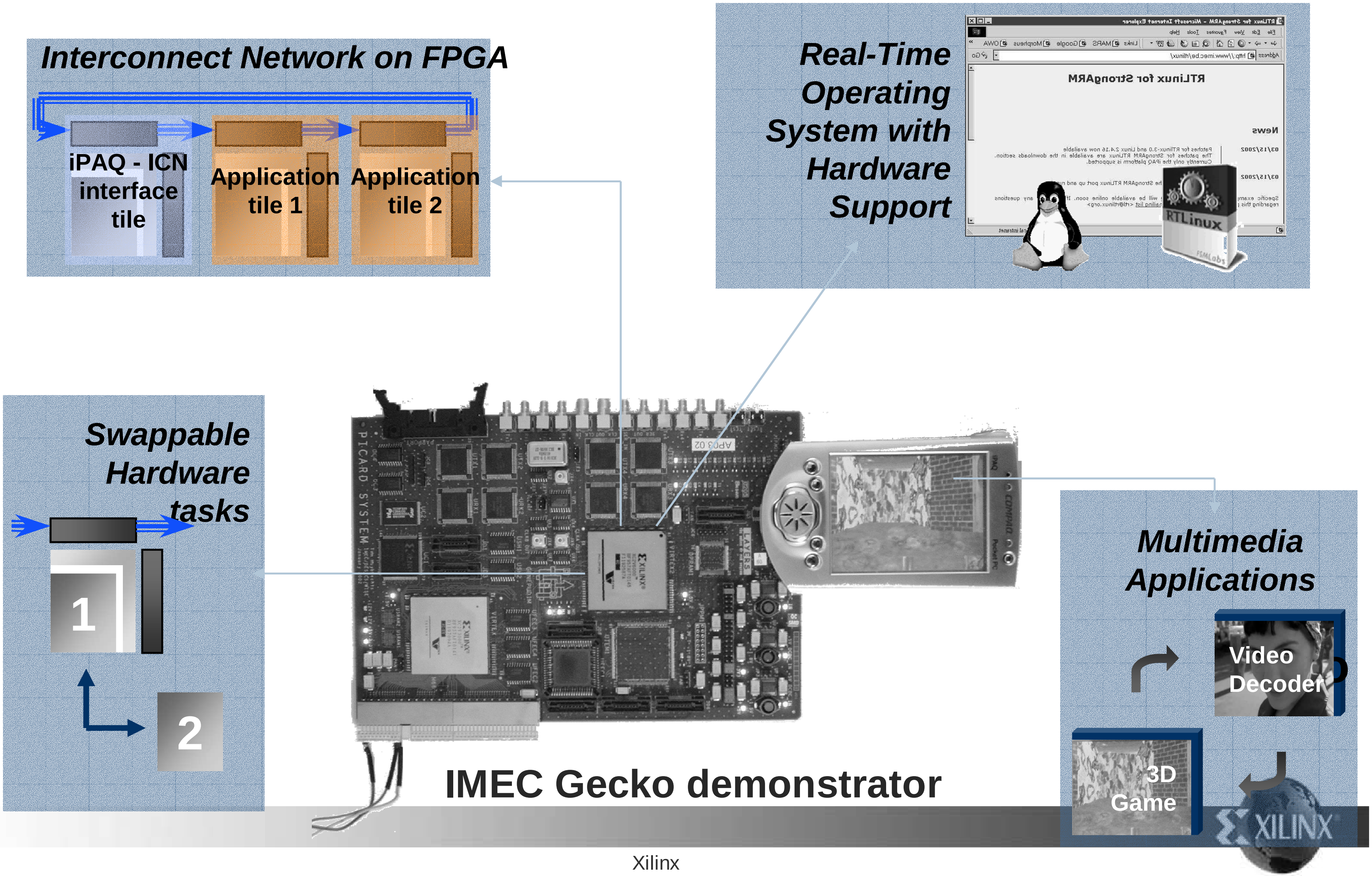


Platform-Based DSP Design

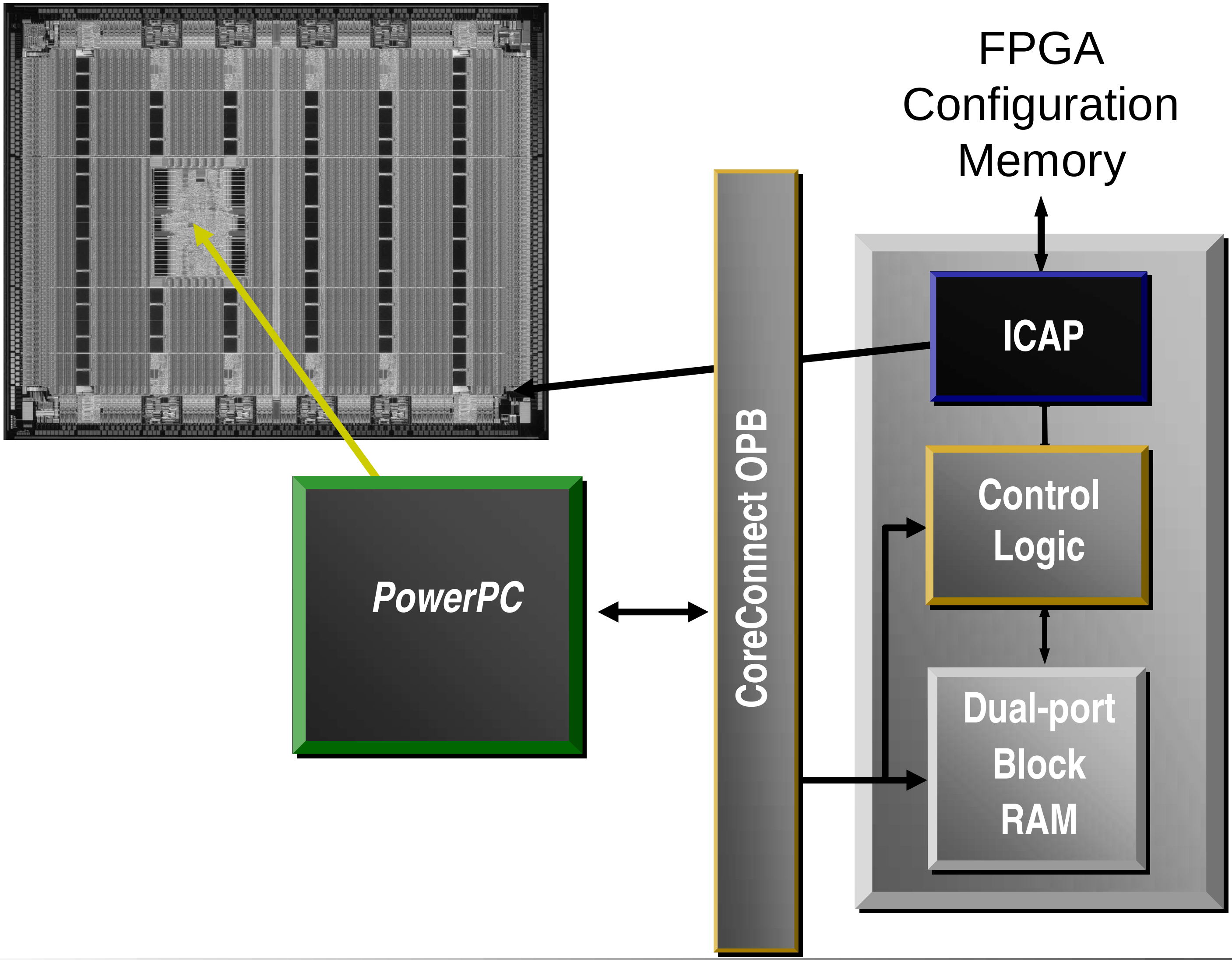


Goal: Provide a *software platform* to support the Platform FPGA

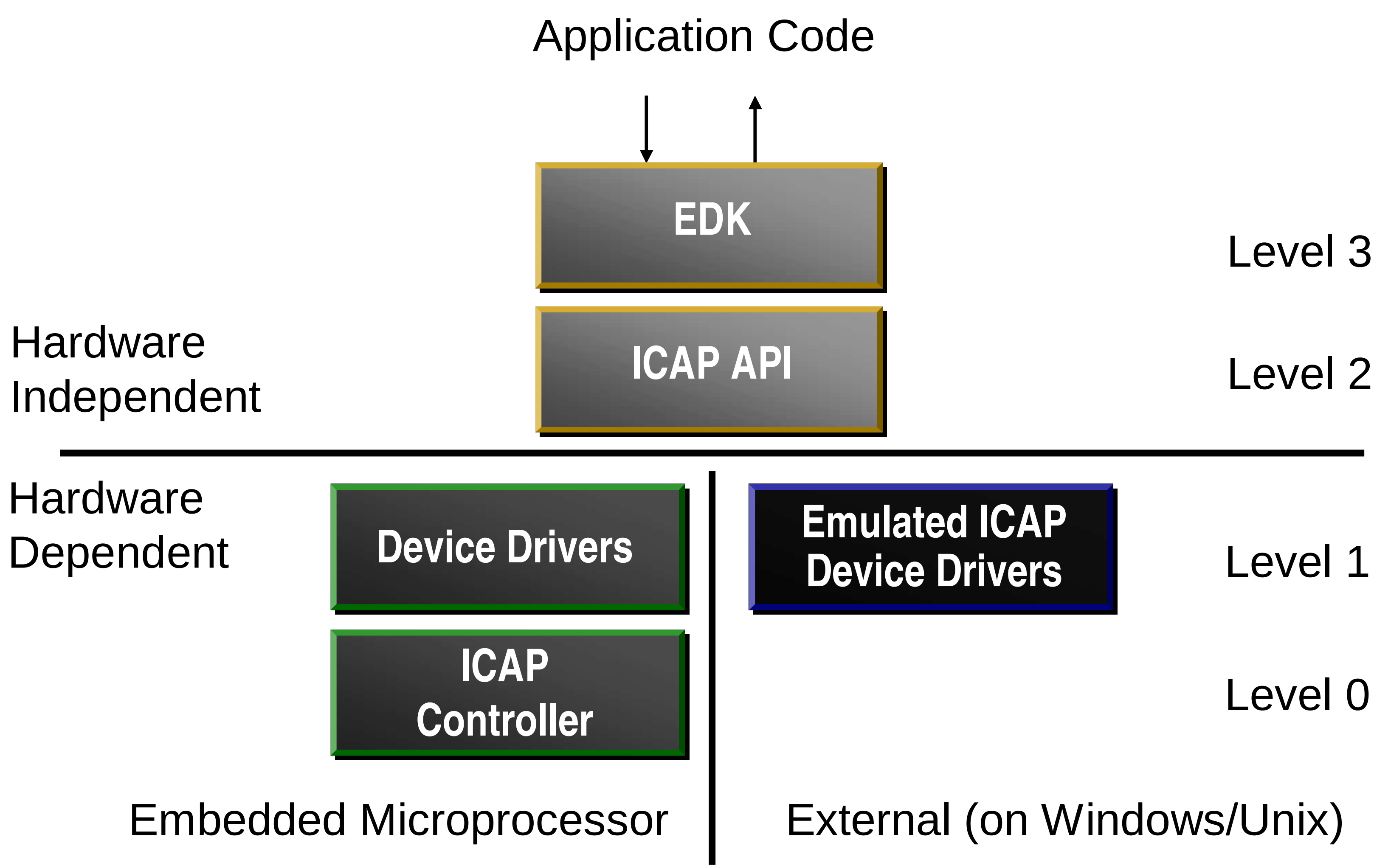
Future use model



Partial Runtime Reconfiguration



Software Stack



Self Reconfiguration Under LINUX

linux - HyperTerminal

File Edit View Call Transfer Help

```
$./lut_test
setxilinx_icap: ioremap 2ffe2000 to c901d000 with size 810
ting device ...
open /dev/xilinx_icap/0
got fd 3
claim icap
result 0
setting the device parameters
Target LUT: row: 40, col: 19, slice: 1

 set LUT contents: val: 0 0 0 0 0 0 0 0 0 0 0 0 0
read LUT contents: val: 0 0 0 0 0 0 0 0 0 0 0 0 0

 set LUT contents: val: 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
read LUT contents: val: 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

 set LUT contents: val: 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
read LUT contents: val: 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

 set LUT contents: val: 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
read LUT contents: val: 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

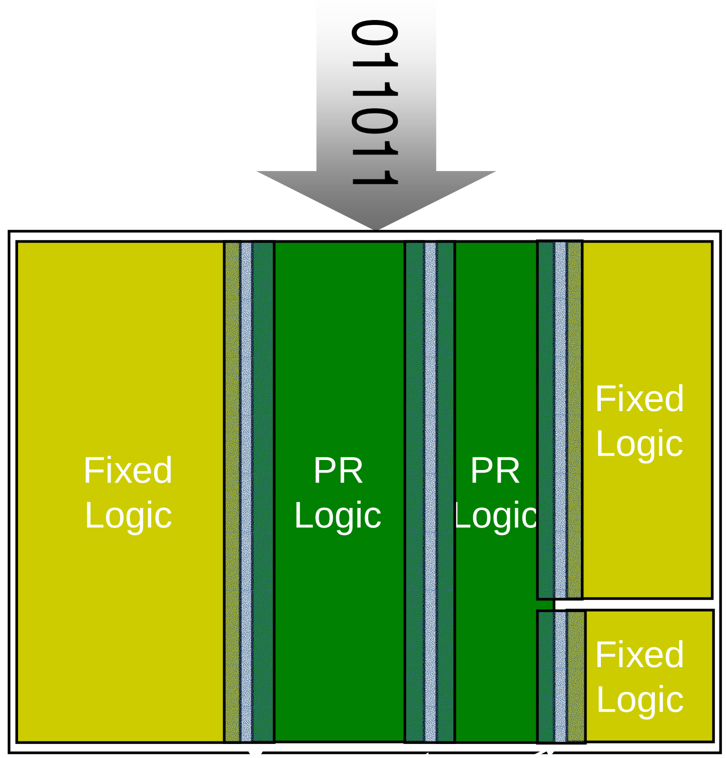
Request & claim ICAP device driver

Configure & readback LUTs

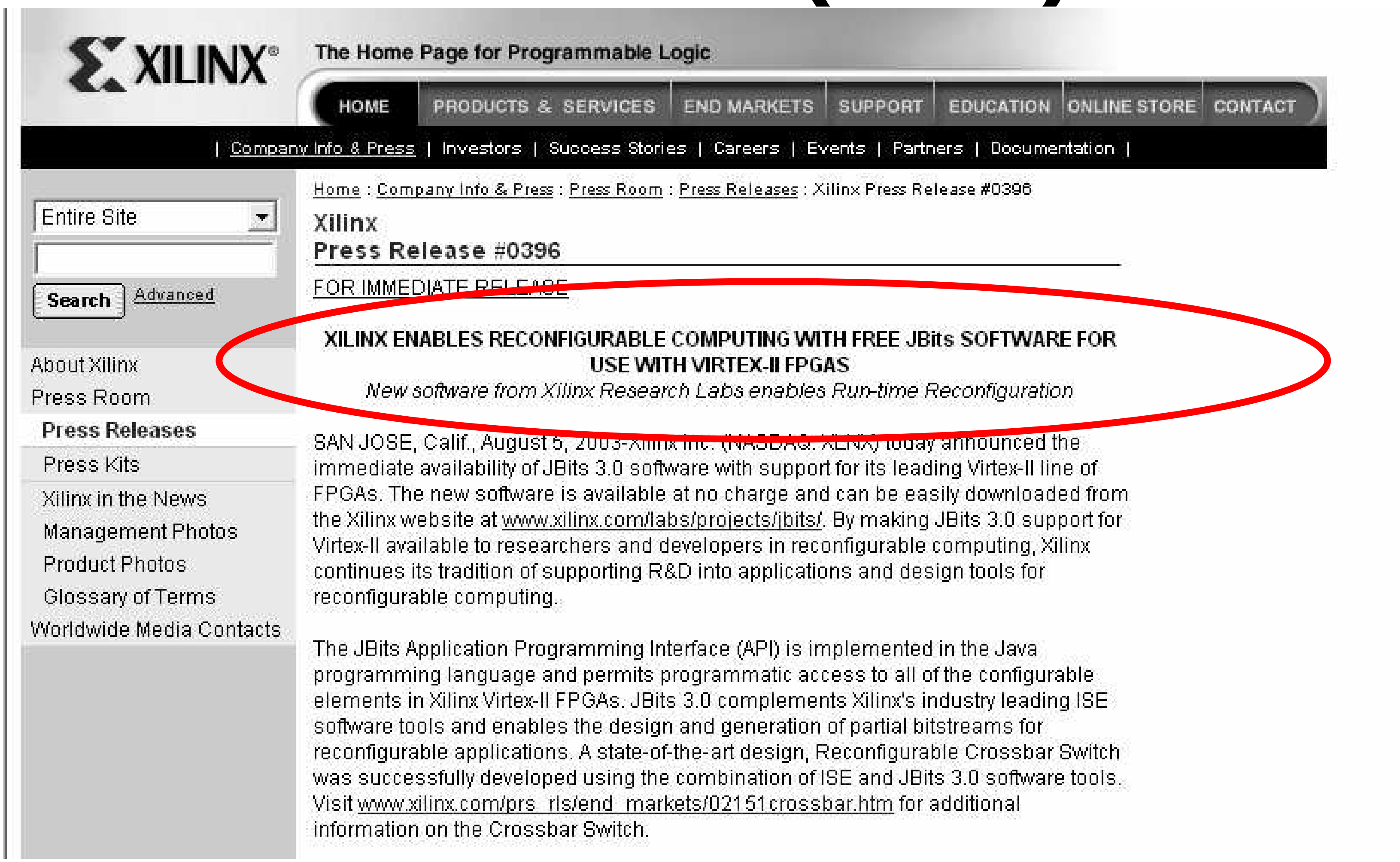
Partial Reconfigurability

FPGA Flexibility for the Field

- Re-program part of an FPGA while it's still running



JBits 3.0 for Virtex II is available (FOC)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FOR IMMEDIATE RELEASE

XILINX ENABLES RECONFIGURABLE COMPUTING WITH FREE JBits SOFTWARE FOR USE WITH VIRTEX-II FPGAS

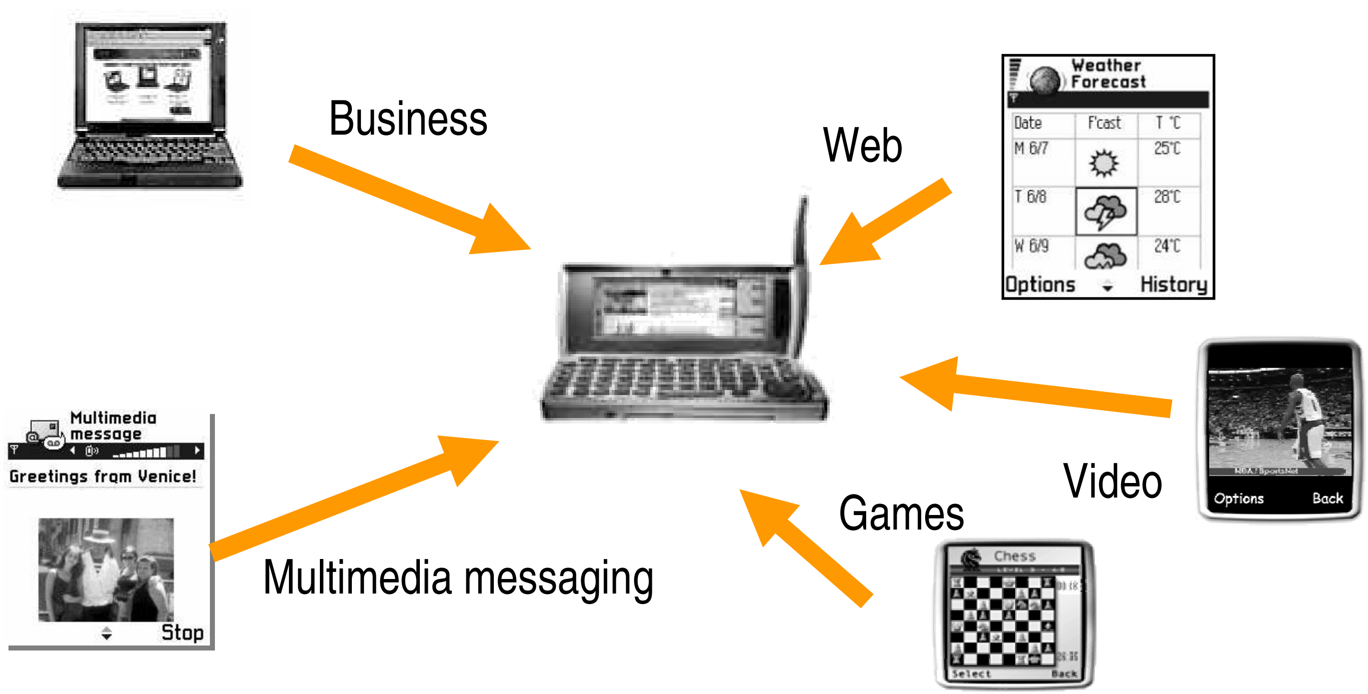
New software from Xilinx Research Labs enables Run-time Reconfiguration

SAN JOSE, Calif., August 5, 2003-Xilinx Inc. (NASDAQ: XLNX) today announced the immediate availability of JBits 3.0 software with support for its leading Virtex-II line of FPGAs. The new software is available at no charge and can be easily downloaded from the Xilinx website at www.xilinx.com/labs/projects/jbits/. By making JBits 3.0 support for Virtex-II available to researchers and developers in reconfigurable computing, Xilinx continues its tradition of supporting R&D into applications and design tools for reconfigurable computing.

The JBits Application Programming Interface (API) is implemented in the Java programming language and permits programmatic access to all of the configurable elements in Xilinx Virtex-II FPGAs. JBits 3.0 complements Xilinx's industry leading ISE software tools and enables the design and generation of partial bitstreams for reconfigurable applications. A state-of-the-art design, Reconfigurable Crossbar Switch was successfully developed using the combination of ISE and JBits 3.0 software tools. Visit www.xilinx.com/prs_rls/end_markets/02151crossbar.htm for additional information on the Crossbar Switch.

Market requirements

A mass market for one person…



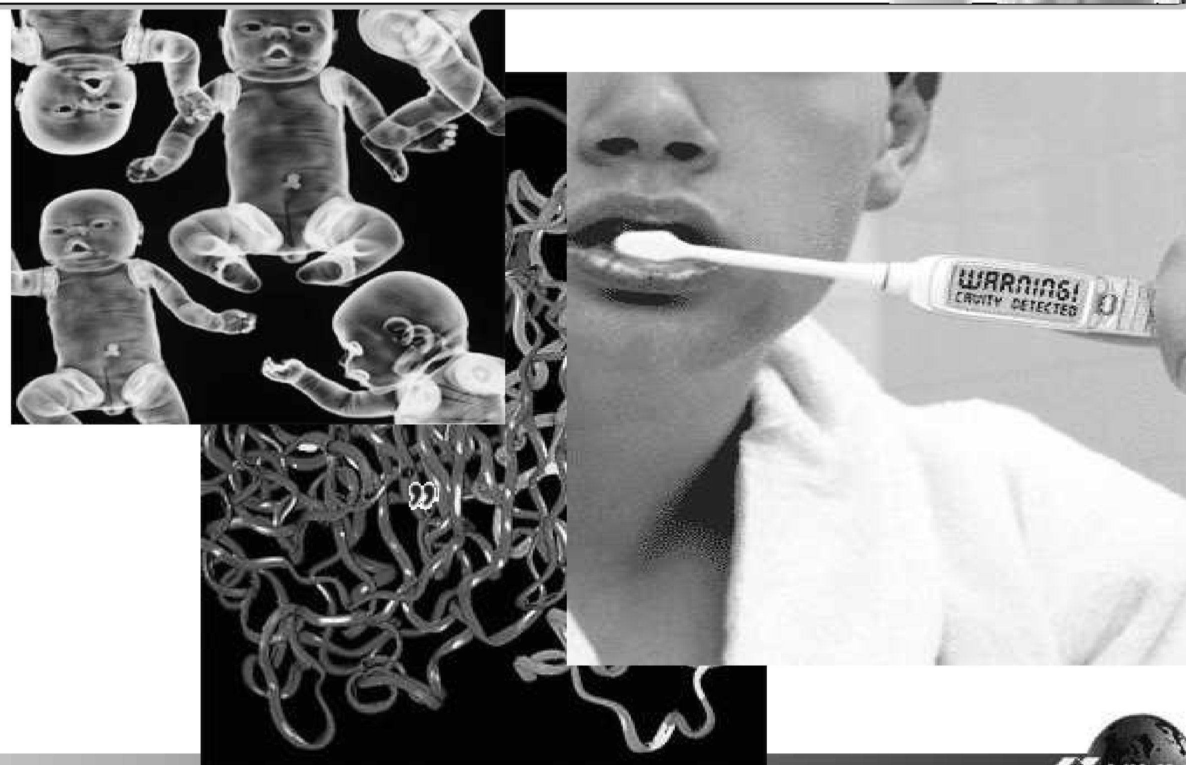
▶ FPGA is reconfigurable

Technology That Will Change People’s Lives

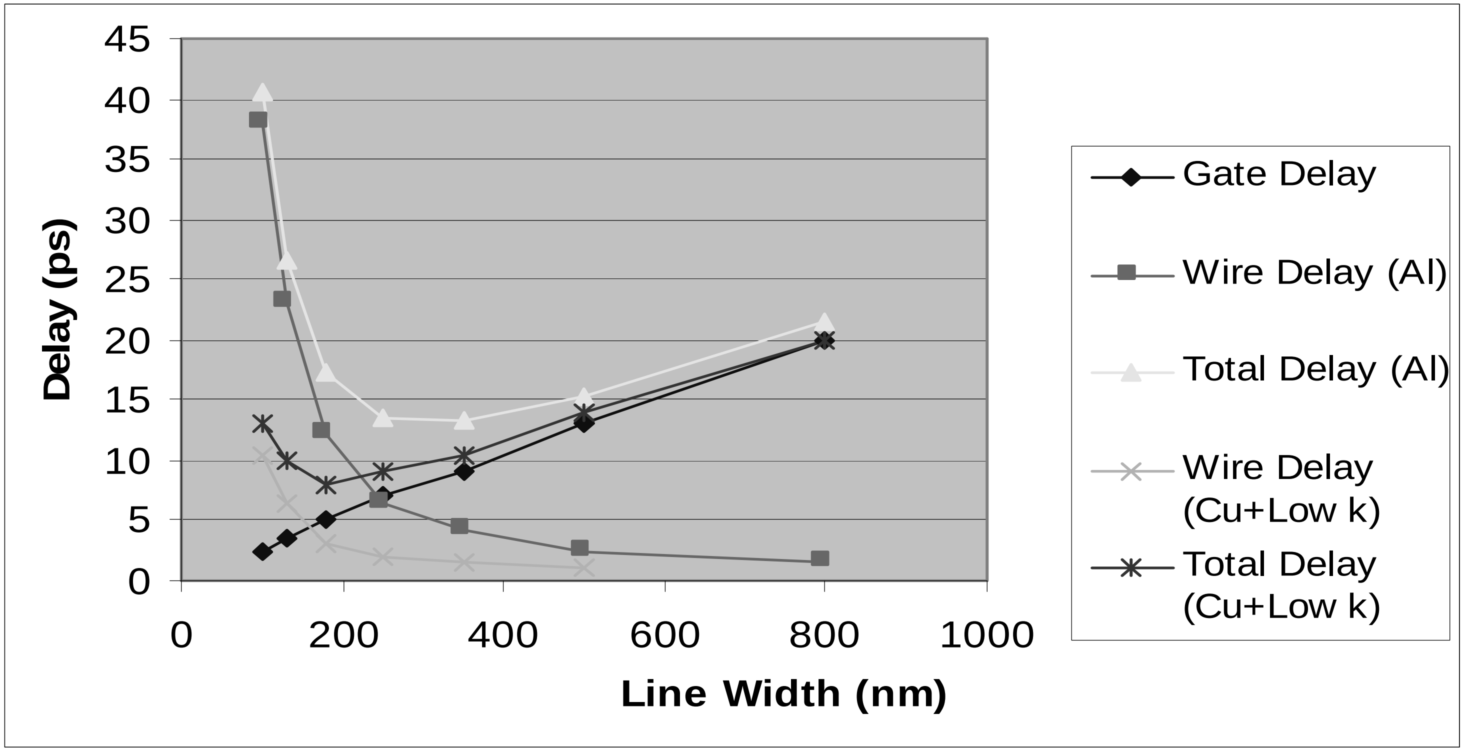
Top Technologies That Will Change Our Lives –
Field programmable “chameleon chips” ranked #1.
Ahead of cloning!

BusinessWeek 50: Masters of Innovation, April 7, 2001

#1 Chameleon chips
#2 Custom Kids
#3 Protein maps
#4 Fractal models
#5 Off-planet production
#6 Nanotechnology
#7 Virtual reality
#8 HIV Antivirals
#9 Optical computing
#10 Ambient Intelligence

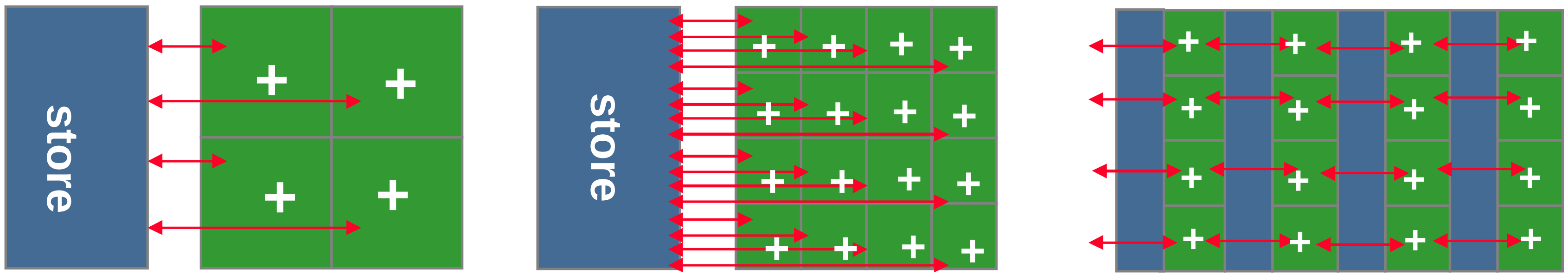


Performance Scaling



Source: ITRS

Architecture Requirements



λ $\lambda/2$ $\lambda/2$

Best design practice to benefit from Moore's Law

- Regular architecture
- Parallel architecture
- Highly testable
- Distributed memory
- Highly pipelined

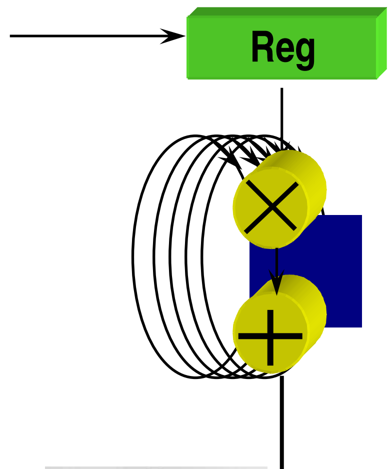
Heat/area V^3/λ^3

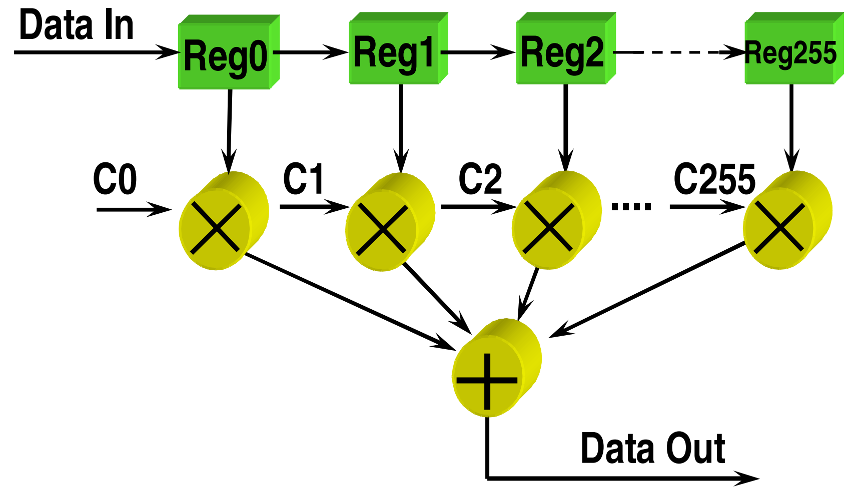
Interconnect Delay $\rho.l^2/\lambda^2$

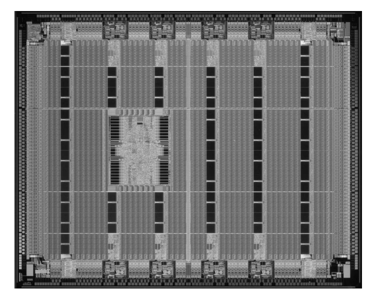
FPGA is future proof

Performance requirements

From **sequential** to **spatial** computing







► **FPGA provides highest MOPS/Watt/$**

Alternative Architectures…

- Cell based design
  - Deep submicron ends ‘composability’ of design
- Processors
  - Not scalable because of data transfer bottleneck
- Application Specific Standard Products (ASSP)
  - Bull’s eye market
- ‘Structured’ ASICs
  - Worst of both worlds

Conclusions

- Today : FPGA's ride the tide of Moore's Law
- Future proof architecture
- Opportunities :
  - Programmable System Platform
  - DSP
- Challenges
  - Low Power
  - Design technology
  - Use model to exploit time dimension