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REVISION HISTORY

Sept. 7, 2001 : T. Obuchowicz, modifications to Dynatext browser information, added information on expansion I/O.

July 25, 2002: T. Obuchowicz, modifications to paths of setup files (found in /CMC/ENVIRON-MENT instead of /home/ted/ENVIRONMENT), removed Dynatext browwer information since it has been replaced by a Web browser interface).

June 2006: T.Obuchowicz, complete revision of Part II and Part III and Part IV. Part II rewritten for Using Precision RTL for synthesis since Synopsys Design Compiler no longer supports FPGA synthesis. Part III rewritten for use with Xilinx ISE, Part IV revised for the new XUP Virtex-II Pro XC2VP30 board which replaces the XC4010E boards made obsolete due to vendor (Mentor) no longer supporting techniology libraries for this device family. Added a Reference section.

July 2007: T. Obuchowicz, added Part V on running tools from the UNIX command line. Added Part VI on performing gate-level simulation.

August 2007: T. Obuchowicz, updated Part IV to include expansion IO module pin mapping information.

March 7, 2011: T. Obuchowicz, updated Part II to reflect the fact that Precision RTL runs only on Linux (and is no longer available on Solaris 10 systems).

July 21, 2011: T. Obuchowicz, updated Part I to account that Synopsys VSS is no longer available under Linux and that Modelsim is the replacement simulator. The Solaris systems in H913 have been replaced with Linux systems. Updated Part III to account for slight differences in the Xilinx ISE 9.2i GUI for the Impact software.