v3.0

MIL-STD-1553B Remote Terminal Core1553BRT

Product Summary

Intended Use

- 1553B Remote Terminal (RT)
- DMA Backend Interface to External Memory
- Direct Backend Interface to Devices

Key Features

- Supports MIL-STD 1553B
- 1 Mb/s Time-Multiplexed Serial Data Bus
- Interfaces to External RAM or Directly to Backend Device
- Synchronous or Asynchronous Backend Interface
- Selectable Clock Rate of 12 or 16 MHz
- Interfaces to Standard 1553B Transceivers
- Programmable Mode Code and Sub-address Legality for Illegal Command Support
- Memory Address Mapping Allowing Emulation of Legacy Remote Terminals
- Fully Synchronous Operation

Targeted Devices

- SX-A Family
- RTSX Family
- RTSX-S Family
- ProASIC^{PLUS} Family
- Axcelerator Family

Core Deliverables

- Netlist Version
  - Compiled RTL Simulation Model, Compliant with the Actel Libero Integrated Design Environment (IDE)
  - Netlist Compatible with the Actel Designer Place-and-Route Tool (with and without I/O pads)
- RTL Version
  - VHDL or Verilog Core Source Code
  - Synthesis Scripts
- Actel Developed Testbench (VHDL)

Development System

- Complete 1553BRT Implementation, Implemented in an A54SX32A
- Includes transceivers and bus termination components

Synthesis and Simulation Support

- Synthesis: Exemplar, Synplicity, Design Compiler, FPGA Compiler, FPGA Express
- Simulation: Vital-compliant VHDL Simulators and OVI-Compliant Verilog Simulators

Verification and Compliance

- Actel-Developed Simulation Testbench Implements a Subset of the RT Test Plan (MIL-HDBK-1553A)
- Test Systems, Inc. (TSI) certified Core1553BRT to MIL-STD-1553B (RT Validation Test Plan MIL-HDBK-1553, Appendix A)

General Description

The Core1553BRT provides a complete, dual-redundant MIL-STD-1553B remote terminal (RT) apart from the transceivers required to interface to the bus. A typical system implementation using the Core1553BRT is shown in Figure 1 and Figure 2 on page 2.

At a high level, the Core1553BRT simply provides a set of memory mapped sub-addresses that 'receive data written to' or 'transmit data read from.' The core can be configured to directly connect to synchronous or asynchronous memory devices. Alternately, the core can directly connect to the backend devices, removing the need for the memory buffers. If memory is used, the core requires 2k words of memory, which can be shared with the local CPU.

The core supports all 1553B mode codes and allows the user to designate as illegal any mode code, or any particular sub-address for both transmit and receive operations. The command legalization can be done within the core or in an external command legality block via the command legalization interface.

The core consists of six main blocks, 1553B encoders, 1553B decoders, backend interface, command decoder, RT controller blocks, and a command legalization block (Figure 2 on page 2).

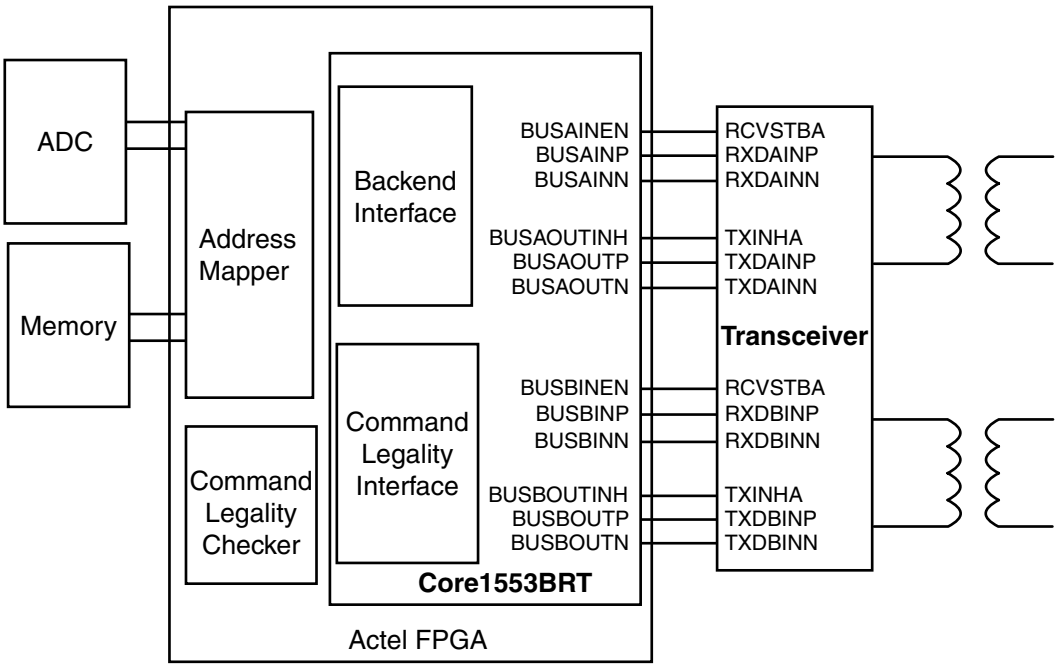


Figure 1 • *Typical Core1553BRT System*

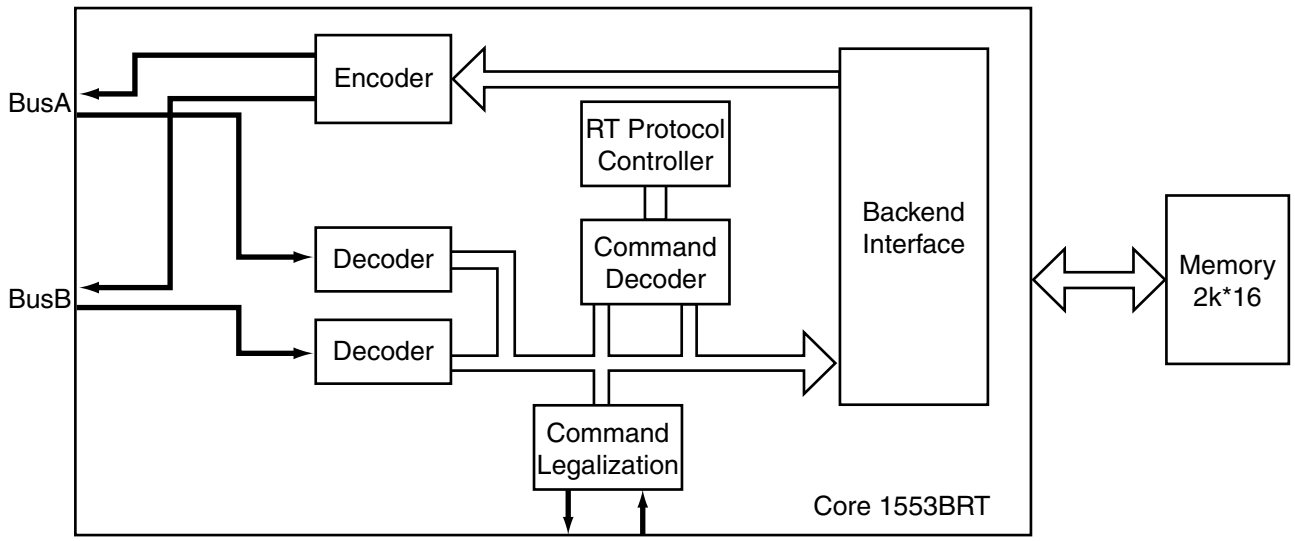


Figure 2 • *Core1553BRT RT Block Diagram*

A single 1553B encoder is used. This takes each word to be transmitted and serializes it, after which the Manchester encodes the signal. The encoder also includes both logic to prevent the RT from transmitting for greater than the allowed period and loopback fail logic. The loopback logic monitors the received data and verifies that the core has correctly received every word that it transmits.

The output of the encoder is gated with the bus enable signals to select which buses the RT should use to transmit.

The core includes two 1553B decoders. The decoder takes the serial Manchester data received from the bus and extracts the received data words. The decoder requires a 12 MHz or 16 MHz clock to extract the data and the clock from the serial stream.

The decoder contains a digital phased lock loop (PLL) that generates a recovery clock used to sample the incoming serial data. The data is then deserialized and the 16-bit word decoded. The decoder detects whether a command or data word is received, and also performs Manchester encoding and parity error checking.

The backend interface for the Core1553BRT allows a simple connection to a memory device or direct connection to other devices, such as analog-to-digital converters, etc. The access rates to this memory are slow with one read or write every 20µs. At 12 MHz operation, this is one read or write every 240 clock cycles.

The backend interface can be configured to connect to either synchronous or asynchronous memory devices. This allows the core to be connected to synchronous logic, memory within the FPGA, or to external asynchronous memory blocks.

The core implements a simple sub-address to the memory address mapping function, allowing the core to be directly connected to a memory block. The core also supports an address mapping function that allows the backend memory map to be modified to emulate legacy 1553B Remote Terminals, therefore, minimizing system and software changes when adopting the Core1553BRT. Associated with this function is the ability to create a user-specific interrupt vector.

The backend interface supports a standard bus request and grant protocol and provides a WAIT input to allow the core to interface to slow memory devices.

The command decoder and RT controller blocks decode the incoming command words, verifying the legality. Then, protocol state machine responds to the command, transmitting or receiving data or processing a mode code.

The Core1553BRT has an internal command legality block that verifies every 1553B command word. A separate interface is provided that, when enabled, allows the command legality decoder to be implemented outside the Core1553BRT. This external interface is intended for use with netlist versions of the core. For the RTL version of the core, this interface can be used or the source code can be easily modified to implement this function.

Core1553BRT Device Requirements

The Core1553BRT can be implemented in several Actel FPGA devices. Table 1 gives the utilization and performance figures for the core implemented in these devices.

The core uses a 16 MHz (or 12 MHz) clock that is required for decoding the Manchester encoded signal. This clock rate is easily met in all Actel silicon families noted in Table 1.

Core1553BRT Verification and Compliance

The Core1553BRT functionality has been verified in simulation and hardware. Full functional verification against the RT test plan as defined in the MIL-HDBK-1553A has been carried out using a VHDL simulation environment.

To fully verify compliance, the core has been implemented on an A54SX32A-STD part connected to external transceivers and memory. Test Systems Inc. has verified the Core1553BRT against the remote terminal test plan in accordance with the RT validation test plan MIL-HDBK-1553A Appendix A.

MIL-STD-1553B Bus Overview

The MIL-STD-1553B bus is a differential serial bus used in military and space equipment. It is comprised of multiple redundant bus connections and communicates at 1MB per second.

The bus has a single active bus controller (BC) and up to 31 remote terminals (RTs). The BC manages all data transfers on the bus using the command and status protocol. The bus controller initiates every transfer by sending a command word and data if required. The selected RT will respond with a status word and data if required.

The 1553B command word contains a five-bit RT address, transmit or receive bit, five-bit sub-address and five-bit word count. This allows for 32 RTs on the bus, but only 31 RTs may be connected, since the RT address (31) is used to indicate a broadcast transfer, i.e. all RTs should accept the following data. Each RT has 30 sub-addresses reserved for data transfers. The other two sub-addresses (0 and 31) are reserved for mode codes used for bus control functions. Data transfers contain up to (32) 16-bit data words. Mode code command words are used for bus control functions such as synchronization.

Table 1 • *Device Utilization*

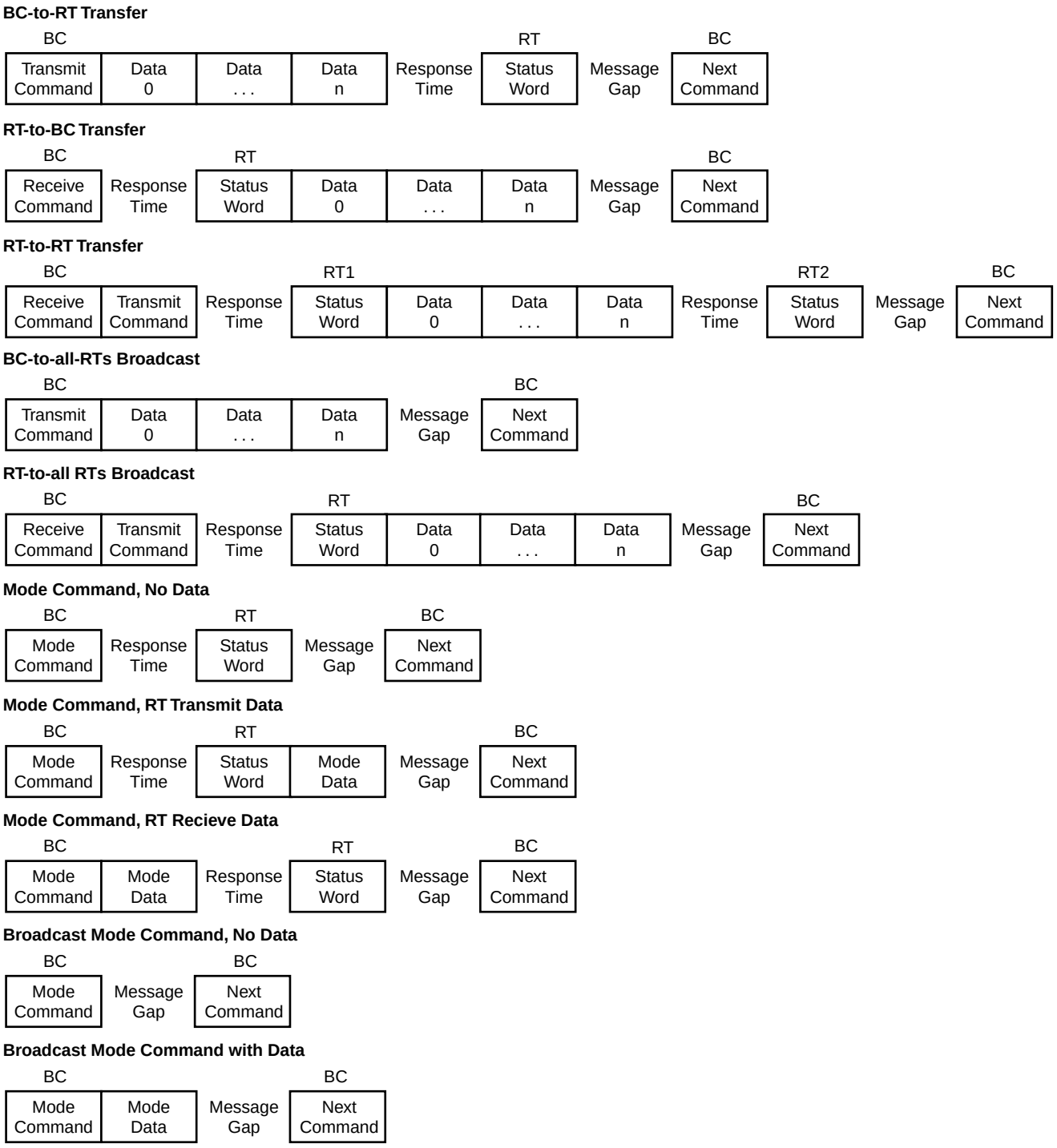
Family	Device	Utilization		
		Comb	Seq	Total
Axcelerator	AX500-STD	14%	12%	13%
ProASIC^{PLUS}	APA150-STD	N/A	N/A	28%
RTSX	RT54SX32-STD	41%	35%	37%
RTSX-S	RT54SX32S-STD	41%	35%	37%
SX-A	A54SX32A-STD	41%	35%	37%

Note: *All devices in this table operate at clock speeds greater than 40 MHz.*

Message Types

The 1553B bus supports ten message transfer types, allowing basic point-to-point and broadcast BC-to-RT data transfers, mode code messages and direct RT-to-RT messages. Figure 3 shows the message formats:

Figure 3 • *1553B Message Formats*



Word Formats

There are only three types of words in a 1553B message: a command word (CW), a data word (DW), and a status word (SW). Each word consists of a three-bit sync pattern, 16 bits of data and a parity bit, providing the 20-bit word (Figure 4).

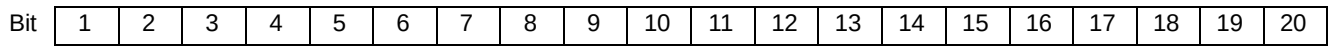
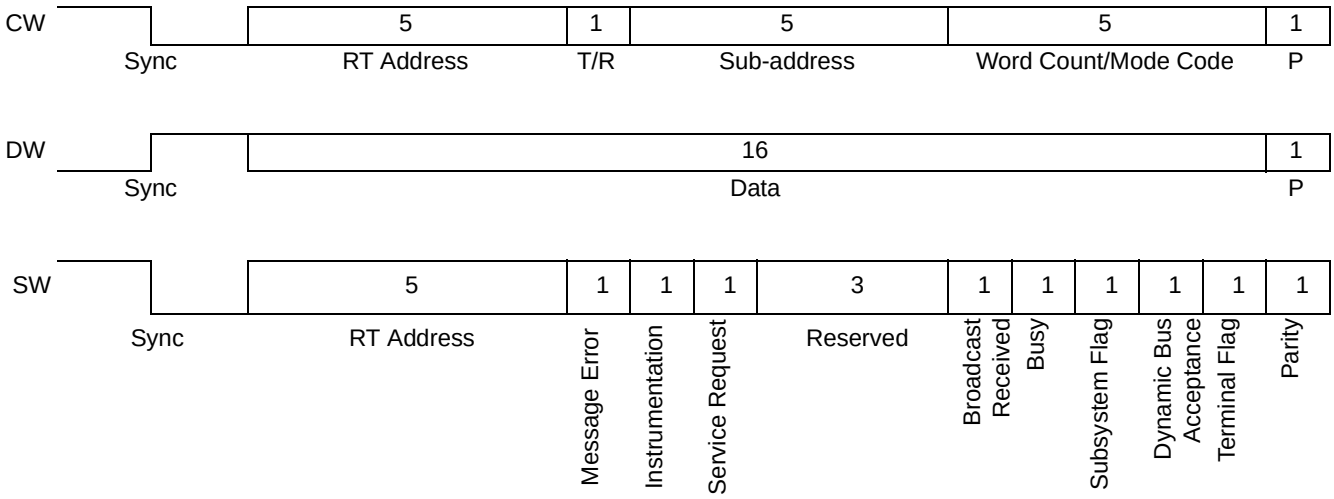


Figure 4 • 1553B Word Formats



I/O Signal Descriptions

1553B Bus Interface

Port Name	Type	Description
RTADDR[4:0]	In	Sets the RT address, must not be set at '11111'
RTADDRP	In	RT Address parity input. This input should be set high or low to achieve odd parity on the RTADDR and RTADDRP inputs. If RTADDR is 00000, the RTADDRP input should be 1
RTADERR	Out	Indicates that the RTADDR and RTADDRP inputs have incorrect parity, or broadcast is enabled, and the RT address is set to 31, and when active (high), the RT is disabled and will ignore all 1553B traffic
BUSAINEN	Out	Active high output that enables for the A receiver
BUSAINP	In	Positive data input from the A receiver
BUSAINN	In	Negative data input from the A receiver
BUSBINEN	Out	Active high output that enables for the B receiver
BUSBINP	In	Positive data input from the bus to the B receiver
BUSBINN	In	Negative data input from the bus to the B receiver
BUSAOUTIN	Out	Active high transmitter inhibit for the A transmitter
BUSAOUTP	Out	Positive data output to the bus A transmitter (is held high when no transmission)
BUSAOUTN	Out	Negative data output to the bus A transmitter (is held high when no transmission)
BUSBOUTIN	Out	Active high transmitter inhibits the B transmitter
BUSBOUTP	Out	Positive data output to the bus B transmitter (is held high when no transmission)
BUSBOUTN	Out	Negative data output to the bus B transmitter (is held high when no transmission)

Control and Status Signals

Port Name	Type	Description
CLK	In	Master clock input (either 12 MHz or 16 MHz)
RSTn	In	Reset input asynchronous (active low)
SREQUEST	In	Directly controls the service request bit in the 1553B status word
RTBUSY	In	Directly controls the busy bit in the 1553B status word
SSFLAG	In	Directly controls the subsystem flag bit in the 1553B status word
TFLAG	In	Controls the subsystem flag bit in the 1553B status word. This can be masked by the "inhibit terminal flag bit" mode code
VWORD[15:0]	In	Provides the 16-bit vector value for the "transmit vector word" mode command
BUSY	Out	Indicates that the 1553BRT is either receiving or transmitting data or handling a mode command
CMDSYNC	Out	This pulses high for a single clock cycle when the RT detects the start of a 1553B command word (or status word) on the bus. Provides an early signal that the RT may be about to receive or transmit data or mode code
MSGSTART	Out	This pulses high for a single cycle when the RT is about to start processing a 1553B message whose command has been validated for this RT
SYNCNOW	Out	This pulses high for a single clock cycle when the RT receives a ‘synchronize’ with or without data mode command. The pulse occurs just after the 1553B command word (sync with no data) or data word (sync with data mode code) has been received
BUSRESET	Out	This pulses high for a single clock cycle whenever the RT receives a reset mode command. The core logic will also automatically reset itself on receipt of this command
INTOUT	Out	This goes high when data has been received or transmitted or a mode command processed. The reason for the interrupt is provided on INTVECT. This output will stay high until INTACK goes high. If INTACK is held high, this output will pulse high for a single clock cycle
INTVECT[6:0]	Out	This seven-bit value contains the reason for the interrupt. It indicates which sub-address data has been received or transmitted. Bit 6: 0: Bad block received 1: Good block received Bit 5: 0: RX data 1: TX data Bits 4:0: Sub-address Further information can be found by checking the appropriate transfer status word for the appropriate sub-address
INTACK	In	Interrupt acknowledge input. When high, this resets INTOUT back to low. If this input is held high, the INTOUT signal will pulse high for one clock cycle every time an interrupt is generated
MEMFAIL	Out	This goes high if the core fails to read or write data to the backend interface within the required time. This can be caused by the backend not asserting MEMGNTn fast enough or asserting MEMWAITn for too long
CLRERR	In	Used to clear the MEMFAIL and other internal error conditions. Must be held high for greater than 2 clock cycles

Note: *All control inputs except RSTn are synchronous and sampled on the rising edge of the clock. All status outputs are synchronous to the rising edge of the clock.*

Command Legalization Interface

The core checks the validity of all 1553B command words. In RTL and netlist versions of the core, the logic may be implemented externally to the core. The command word is provided, and the logic must generate the command valid input. The command legalization interface also provides two strobes that are used to latch the command value to enable it to be used for address mapping and interrupt vector extension functions (Table 2).

Backend Interface

The backend interface supports both synchronous operation (to the 12/16 MHz clock) and asynchronous operation to backend devices (Table 3 on page 8).

***Table 2** • Command Legalization Interface*

Port Name	Type	Description
USEEXTOK	In	When '0,' the core uses its own internal command valid logic, enabling all legal supported mode codes and all sub-addresses When '1,' the core disables its internal logic and uses the external CMDOKAY input for command legality
CMDVAL[11:0]	Out	Active Command 11:0: Non-broadcast; 1: Broadcast 10:0: Receive; 1: Transmit 9:5: Sub-address 4:0: Word count / mode code These outputs are valid throughout the complete 1553B message. They can be also be used to steer data to particular backend devices. In particular, bit 11 allows non-broadcast and broadcast messaged to be differentiated as required by Mil-STD-1553B Notice 2
CMDOKAY	In	Command word is okay (active high). The external logic must set this within 2µs from the CMDVAL output changing
ADDRLAT	Out	CMDVAL address latch enable output (active high) is used to latch the CMDVAL when it is being used for an address mapping function. ADDRLAT should be connected to the enable of a rising edge clock flip flop
INTLAT	Out	CMDVAL interrupt vector latch enable output (active high) is used to latch the CMDVAL when it is being used for an extended interrupt vector function. INTLAT should be connected to the enable of a rising edge clock flip flop

Table 3 • *Backend Signals*

Port Name	Type	Description
MEMREQn	Out	Memory Request (active low) output. The backend interface requires memory access completion within 10µs of MEMREQ going low to avoid data loss or overrun on the 1553B interface*
MEMGNTn	In	Memory Grant (active low) input. This input should be synchronous to CLK and needs to meet the internal register setup time. This input may be held low if the core has continuous access to the RAM
MEMWRn	Out	Memory Write (active low) Synchronous mode: This output indicates that data is to be written on the rising clock edge Asynchronous mode: This output will be low for a minimum of one clock period and can be extended by the MEMWAITn input. The address and data are valid one clock cycle before MEMWRn is active and held for one clock cycle after MEMWRn goes inactive
MEMRDn	Out	Memory Read (active low) Synchronous mode: This output indicates that data will be read on the next rising clock edge. This signal is intended as the read signal for synchronous RAMS Asynchronous mode: This output will be low for a minimum of one clock period and can be extended by the MEMWAITn input. The address is valid one clock cycle before MEMRDn is active and held for one clock cycle after MEMRDn goes inactive. The data is sampled as MEMRDn goes high
MEMCSn	Out	Memory Chip Select (active low). This output has the same timing as MEMADDR
MEMWAITn	In	Memory Wait (active low) Synchronous mode: This input is not used, it should be tied high Asynchronous mode: Indicates that the backend is not ready, and the core should extend the read or write strobe period. This input should be synchronous to CLK and needs to meet the internal register set up time. It can be permanently held high
MEMOPER[1:0}	Out	Indicates the type of memory access being performed 00: Data transfer for both data and mode code transfers 01: TSW 10: Command Word 11: Not used
MEMADDR[10:0]	Out	Address (active low). Memory address output (The sub-address mapping is covered in the memory allocation section)
MEMDOUT[15:0]	Out	Memory Data output (active low)
MEMDIN[15:0]	In	Memory Data input (active low)
MEMCEN	Out	Control Signal Enable (active high). This signal is high when the core is requesting the memory bus and has been granted control. It is intended to enable any tristate drivers that may be implemented on the memory control and address lines
MEMDEN	Out	Data Bus Enable (active high). This signal is high when the core is requesting the memory bus, has been granted control and is waiting to write data. It is intended to enable any bidirectional drivers that may be implemented on the memory data bus

Note: **The 10µs refers to the time from MEMREQn being asserted to the core, de-asserting its MEMREQn signal. The core has an internal overhead of five clock cycles and any inserted wait cycles will also reduce this time. This time increases to 19.5µs, if the WRTTSW and WRTCMD inputs are low.*

Miscellaneous I/O

Several inputs are used to modify the core functionality to simplify integration in the application. These inputs should be tied to logic '0' or logic '1,' as appropriate (Table 4).

Generics (RTL Version Only)

Core1553BRT has some top-level generics (parameters) that are used to select the actual operational modes of the core. These parameters are not supported on netlist versions of the core. Instead, Actel supplies different netlists for each possibility (Table 5).

Standard Memory Address Map

Core1553BRT requires an external 2048*16 memory. This memory is split into (64) 32-word data buffers. Each of the thirty sub-addresses has a receive and a transmit buffer, as shown in Table 6 on page 10.

The memory allocated to the unused receive sub-addresses 0 and 31 is used to provide status information back to the rest of the system. At the end of every transfer, a transfer status word, TSW, is written to these locations.

Table 4 • Miscellaneous I/O

Port Name	Type	Description
WRTCMD	In	When '1,' the core will write the 1553B command word to the locations used for the TSW values. If WRTTSW is also enabled, then the command word is written to memory at the start of a message and the TSW value will overwrite the command word at the end of the message, unless an external address mapping function is used
WRTTSW	In	When '1,' core will write the transfer status word to the memory When '0,' the core disables the writing of the transfer status word to memory. This is useful for simple RT applications that do not use memory but has a direct connection to the backend device
EXTMDATA	In	When '1,' the core reads and writes mode code data words to and from the external memory (except for the transmit last command and transmit Bit word). The VWORD input is not used when this input is active
INTENBBR	In	When active '1,' the core generates interrupts when both good and bad 1553B messages are received. When in-active '0,' the core only generates interrupts when good messages are received
ASYNCIF	In	When '1,' the backend interface is in asynchronous mode When '0,' the backend interface is in synchronous mode
TESTTXTOUT	In	This input is for test use only. It should be tied low When high, the RT will transmit greater than 32 data words if a transmit data command word is received. This will cause the RT to shut down the transmitter and set the TIMEOUT bits in the BIT word
BCASTEN	In	This input enables broadcast operation When '1,' broadcast operations are enabled When '0,' broadcast messages (i.e. RT Address 31) are treated as normal messages. If the RTADDR input is set to 31, then the RT will respond to the message
SA30LOOP	In	This input alters the backend memory mapping so that sub-address 30 provides automatic loopback (Table 6) When '0,' the RT does not loopback sub-address 30. Separate memory buffers are used for transmit and receive data buffers When '1,' the RT maps the transmit memory buffer for sub-address 30 to the receive memory buffer for sub-address 30, i.e. the upper address line is forced to '0'

Table 5 • Generics

Port Name	Type	Description
CLKSPD	Integer	Sets the clock frequency of the core. When '0,' the clock must be 16 MHz. When '1,' the clock must be 12 MHz

Table 6 • Standard Memory Address Map

Address	RAM contents	
000-01F	RX transfer status words	The core only writes to these addresses (except when SA30LOOP is high)
020-03F	Receive sub-address 1	
	…	
3C0-3DF	Receive sub-address 30	
3E0-3FF	TX transfer status words	
400-41F	Not used	The core only reads from these addresses
420-43F	TX transfer sub-address 1	
	…	
7C0-7DF	TX transfer sub-address 30	
7E0-7FF	Not used	

If the SA30LOOP input is set high, the RT maps transmit sub-address 30 to the receive sub-address 30, i.e. the upper address bit is forced to '0.' This provides a loopback sub-address as per MIL-STD-1553B Notice 2. The TSW is still written to address 03EE. It should be noted that this is not strictly compliant with the specification since the transmit buffer will contain invalid data if the received command fails, e.g. parity error. The transmit buffer should only be updated if the receive command had no errors. To implement this function in a full compliance, the SA30LOOP input should be tied low and the RT backend should copy the receive memory buffer to the transmit memory buffer only after the RT signals that the message was received with no errors.

When the memory buffer is implemented within the FPGA device using dual port RAMs (in ProASIC^{PLUS}), separate receive and transmit RAM blocks can be used (each as 1k words), as shown in Figure 5. In these cases, the RX memory is selected when A10=0 and the TX memory when A10=1. In this case, the SA30LOOP input must be tied low.

Memory Address Mapping

The core supports an external memory address mapper that allows the RT memory allocation to be easily customized. To use this function the CMDVAL output must be latched by the ADDRLAT signal as shown in Figure 6 on page 11.

Then, the address mapper function can map the 1553B command words, data words including mode code data and the transfer status words to any memory address.

Interrupt Vector Extension

The core generates a seven bit interrupt vector that contains the sub-address and whether it was a transmit or receive message. Some systems may need to include whether the message was broadcast, a mode code, or the actual word count in the interrupt vector. The core supports an interrupt vector extension function, similar to the address mapper function using the INTLAT signal, as shown in Figure 7 on page 11.

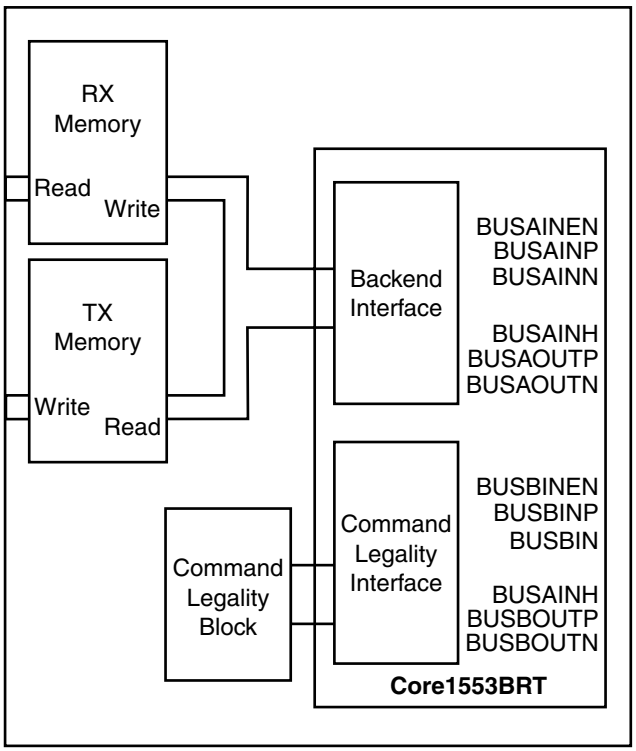


Figure 5 • Using Internal FPGA Memory Blocks

Status Word Settings

The Core1553BRT sets bits in the 1553B status word in compliance with MIL-STD1553B. This is summarized in Table 7 on page 11.

Command Word Storage

At the start of every 1553B bus transfer, the 1553B command word is written to the RAM locations 000-01F for receive operations and 3E0 to 3FF for transmit operations, the address used is

CMD location RX Commands "000000" and SA

CMD location TX Commands "100000" and SA

If the RT is implemented without a memory-based backend, the writing of the command word can be disabled (WRTCMD

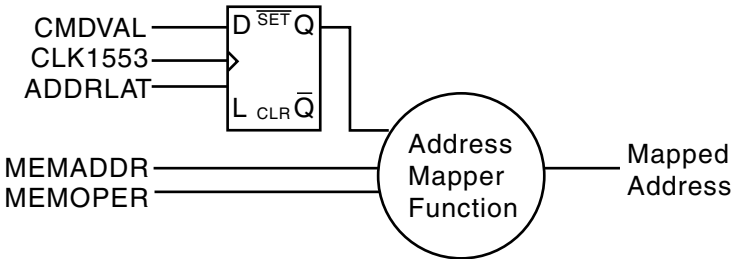


***Figure 6** • Memory Address Mapping*

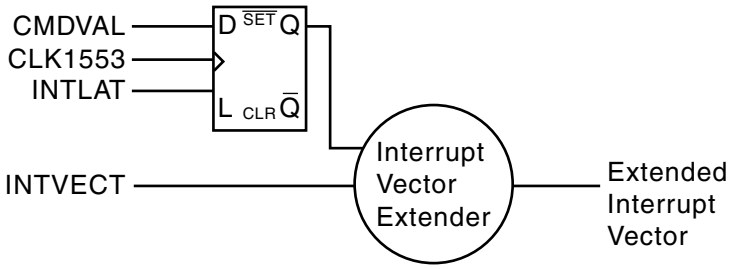


***Figure 7** • Interrupt Vector Extension*

***Table 7** • Status Word Bit Settings*

Bit	Function	Setting
15:11	RT Address	Equals the RTADDR input
10	Message Error	Is set whenever the RT detects a message error
9	Instrumentation	Always ‘0’
8	Service Request	Controlled by the SSFLAG input
7:5	Reserved	Always ‘000’
4	Broadcast Received	Is set whenever a broadcast message received
3	Busy	Controlled by the RTBUSY input
2	Subsystem Flag	Controlled by the SSFLAG input
1	Dynamic Bus Acceptance	Always ‘0.’ The Core1553BRT does not operate as a bus controller
0	Terminal Flag	Controlled by the TFLAG input. If a “inhibit terminal flag” mode code is in effect will be ‘0’

input). This simplifies the design of the backend logic that directly controls the backend function.

Transfer Status Words (TSW)

At the end of every 1553B bus transfer, a transfer status word is written to the RAM in locations 000-01F for receive operations and 3E0-3FF for transmit operations. The address used is:

TSW location RX Commands: ‘000000’ and SA

TSW location TX commands: ‘011111’ and SA

As an example, the TSW address for a transmit command with sub-address 24 would be ‘01111110100’ (3F4h). The TSW contains the information in Table 8 on page 12.

If the RT is implemented without a memory based backend, the writing of the TSW can be disabled. This simplifies the design of the backend logic that directly controls backend functions.

Backend Access Times

During normal operation, the backend must allow a memory access to complete within 19.5µs. When either the command word or the TSW are written to memory, the backend must be capable of completing memory accesses in 10µs.

While the status word is being transmitted, the core must write the command word to memory and fetch the first data word. Two memory accesses are performed in the 20µs that the status word takes to transmit.

At the end of a broadcast-receive command, Core1553BRT writes the last data word and the TSW value before the RT decodes the next command. Two memory accesses occur in the 20µs that the command word is being decoded.

The core includes a timer that is set to terminate backend memory access at 19.5µs or 10.0µs when either WRTCMD or WRTTSW are active.

1553BRT Operation

Data Transfers – Receive

When a receive data transfer command is detected, the core will decode each incoming word. At the end of each word, the core will assert MEMREQn. When MEMGNTn goes low, it will write the data word to the memory and release the MEMREQn. This process is repeated until the correct number of words has been transferred. The core will then transmit its 1553B status word. Finally, the TSW is also written to the memory.

Data Transfers – Transmit

When a transmit data transfer command is detected, the core will transmit its status word and assert MEMREQn. When MEMGNTn goes low, it will read a data word from the memory and release the MEMREQn. Once the word is available, the core will transmit the data word. The core will continue to request data from the memory interface until the required number of words have been transferred. Finally, the TSW is written to the memory.

RT-to-RT Transfer Support

The core supports RT-to-RT transfers. If a transmitting core does not start transferring data within the required time, the core will detect this and set the WCNTERR bit in the transfer status word.

Mode Codes

When the core receives a mode code, it first checks its command validity. If the command is valid, it is processed in accordance with the specification. Otherwise, the message error bit will be set in the 1553B status word. Table 9 on page 13 lists the supported mode codes.

Two mode codes, (1) transmit a vector word and (2) synchronize with data, require external data. When EXTMDATA is active, these values are read from and written to memory. The vector word, which is read from location 210h or 3F0h and the synchronize with the data word, is written to location 011h or 1F1h, depending on whether sub-address 0 or 31 is used. When EXTMDATA is inactive, the vector word value is set by the VWORD input and the synchronize with the data word that is discarded.

If EXTMDATA and either WRTCMD or WRTTSW are active, then the command word will be written to location 000h during a synchronize with the data mode code (sub-address 0). Then, the data word is written to location 011h, and finally, the TSW value is written to location 000h. Location 011h is also used to store the command word and/or TSW value for sub-address 17. This may cause some system problems and can be avoided by making legal the synchronization with the data mode code or implementing an external address mapper function to map these accesses to different addresses.

Loopback Tests

The Core1553BRT performs loopback testing on all of its transmissions. The transmit data is fed back into the receiver and each transmitted word is compared. If an error is detected, the loopback fail bit is set in the TSW and also in the BIT word.

Table 8 • Transfer Status Word

Bit	Name	Description	
15	USED	This bit is set to ‘1’ at the end of the transmit or receive command	
14	OKAY	Indicates that no errors are detected, i.e. bits 11 to 5 are all ‘0’	
13	BUSN	Indicates on which bus the command was received 0: BUSA 1: BUSB	
12	BROADCAST	Indicates a broadcast command	
11	LPBKERRB	Indicates that the loopback logic detected an error on the transmitted data for bus B	
10	LPBKERRA	Indicates that the loopback logic detected an error on the transmitted data for bus A	
9	ILLEGAL CMD	The command was illegal. Either a request to transmit from an illegal sub-address or an illegal mode code was received	
8	MEMIFERR	Indicates that the DMA memory access failed to complete quickly enough	
7	MANERR	Indicates that a Manchester encoding error was detected in the incoming data	
6	PARERR	Indicates that a parity error was detected in the incoming data	
5	WCNTERR	Indicates that the incorrect number of words was received	
4:0	COUNT	SA1 to SA31	Indicates the number of words received or transmitted for that sub-address. If WCNTERR is ‘0,’ 00000 indicates 32 words. Otherwise, 00000 indicates zero words transferred
		SA0 or SA31	Indicates which mode code was received or transmitted per the 1553B specification

Table 9 • Supported Mode Codes

T/R Bit	Mode code	Function and Effect	Data Word	Core Supports	Broadcast Allowed
1	00000 0	Dynamic Bus Control Core does not support bus controller functions, so it will set the message error and the dynamic bus control bit in the status word	No	No	No
1	00001 1	Synchronize The core will assert its SYNCNOW output after the command word has been received	No	Yes	Yes
1	00010 2	Transmit Status Word The core re-transmits the last status word	No	Yes	No
1	00011 3	Initiate Self Test Core does not support self test. Since the core supports the transmit BIT word mode code, this command is treated as legal and will not set message error	No	Yes	Yes
1	00100 4	Transmitter Shutdown The core will disable the encoder on the other bus	No	Yes	Yes
1	00101 5	Override Shutdown The core will re-enable the encoder on the other bus	No	Yes	Yes
1	00110 6	Inhibit Terminal Flag The core will mask the TFLAG input and the terminal flag bit in the status word will be forced to zero	No	Yes	Yes
1	00111 7	Override Inhibit Terminal Flag The core will re-enable the TFLAG input	No	Yes	Yes
1	01000 8	Reset Remote Terminal The core will assert its BUSRESET output after the command word has been received. It will also reset itself	No	Yes	Yes
1	10000 16	Transmit Vector Word The core will transmit a single data word that contains the value on the VWORD input	Yes	Yes	No
1	10010 18	Transmit Last Command Word The core will transmit a single data word that contains the last command word received	Yes	Yes	No
1	10011 19	Transmit Bit Word The core will transmit a single data word that contains the extended core status information. The value of this word is defined in Table 11 on page 16	Yes	Yes	No
0	10001 17	Synchronize with Data The core will assert its SYNCNOW output after the data word has been received	Yes	Yes	Yes
0	10100 20	Selected Transmitter Shutdown The core only supports two buses. Hence, this command is illegal, the message error bit in the status word will be set	Yes	No	Yes
0	10101 21	Override Selected Transmitter Shutdown The core only supports two buses. Hence, this command is illegal. The message error bit in the status word will be set	Yes	No	Yes

Error Detection

Error Condition	Action
Command Word 1. Parity or Manchester Encoding Errors 2. Incorrect SYNC waveform	Command is ignored No interrupt generated
Mode Codes 1. Illegal Mode Code or invalid sub-address (from internal or external legality block)	MSGERR in SW is set, and the SW is transmitted Message Failure interrupt generated
Broadcast Data Commands 1. TX bit set in Command word	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
Data Word 1. Parity or Manchester Encoding Errors 2. Incorrect number of words received 3. Data words are continuous 4. Incorrect SYNC waveform	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
RT-to-RT 1. First command word must be RX 2. Second command word must be TX and non-broadcast 3. RX RT checks the TX SW and verifies the SYNC pattern, RT address, MSGERR, and BUSY fields 4. The first data word sync must be received within 57µs of the command word parity bit	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
Transmit Data Error 1. The RT monitors its transmissions on the bus through its decoder and verifies that the correct data is transmitted with no Manchester or parity errors	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
Backend Failure 1. The RT makes sure that the backend responds to read and write cycles within the required time	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
BUSY 1. Backend RTBUSY input is active at any point during the message	Data transfer is aborted MSGERR in SW is set, and the SW is not transmitted Message Failure interrupt generated
Transmitter Overrun 1. Transmits for greater than 668µs. The internal state machines prevent this from happening, but the core includes the required timer and functionality. This is implemented separately to the encoder to provide complete protection	Core shuts down transmissions on the bus

Built-in Test Support

The Core1553BRT provides a BIT word. This is used to communicate fail information back to the bus controller. The BIT word contains information from Table 10.

Command Legalization Interface

1553B commands can be legalized in two ways with the Core1553BRT. For RTL versions, one of the modules in the source code can be edited to legalize or make illegal command words based on the sub-address, mode code/word count or broadcast fields of the command word. For netlist and RTL versions, external logic may be used to decode the legal/illegal command words (Figure 8).

The user customization logic block takes in the CMDVAL and simply sets CMDOKAY for all legal command words, the CMDVAL encoding is given in Table 11 on page 16. The external logic must implement this function within 3µs.

Table 10 • *External Command Legalization*

Bit	Function	Description
15	BUSINUSE	Indicates on which bus the transmit BIT word command was received 0 : Bus A 1: Bus B
14	LPBKERRB	Indicates that the loopback logic detected an error on the transmitted data for Bus B. Is cleared by the CLRERR input
13	LPBKERRA	Indicates that the loopback logic detected an error on the transmitted data for Bus A . Is cleared by the CLRERR input
12	SHUTDOWNB	Indicates that Bus B is shutdown. This occurs after a transmitter shutdown mode code is received or the hardware timer detected that the core transmitted for greater than 668µs on Bus B
11	SHUTDOWNA	Indicates that Bus A is shutdown. This occurs after a transmitter shutdown mode code is received or the hardware timer detected that the core transmitted for greater than 668µs on Bus A
10	TFLAGINH	Terminal flag inhibit setting
9	WCNTERR	A word count error has occurred. This bit is cleared by the CLRERR input
8	MANERR	A Manchester encoding error has occurred. This bit is cleared by the CLRERR input
7	PARERR	A parity error has occurred. This bit is cleared by the CLRERR input
6	RTRTTO	The transmitting RT did not provide data on RT-to-RT transfer. This bit is cleared by the CLRERR input
5:0	VERSION	Indicates the core version

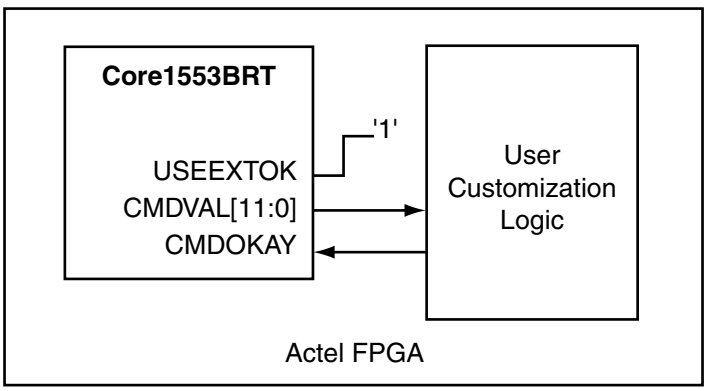


Figure 8 • *Command Legalization Logic*

Bus Transceivers

The Core1553BRT does not include the transceiver that is required to drive the 1553B bus. The Core1553BRT is designed to directly interface to MIL-STD-1553 transceivers. There are several suppliers of MIL-STD-1553 transceivers, such as DDC (BU-63147), and Aeroflex (ACT4402).

In addition to the transceiver, a pulse transformer is required for interfacing to the 1553B bus. Figure 9 and Figure 10 on page 17 show the connections required from the Core1553BRT to the transceivers and then to the bus via the pulse transformers.

Typical RT Systems

The Core1553BRT can be used in systems with and without backend memory. Figure 9 shows a typical implementation for a system with backend memory and a CPU to process the messages. Figure 10 on page 17 shows a system with direct connection between the Core1553BRT and external analog-to-digital converters, etc. In this case, any glue logic required between the core and the device being interfaced to can simply be implemented within the FPGA containing the core.

Table 11 • *CMDVAL Encoding*

Bits	Function	Description
11	Broadcast	'1' indicates broadcast, i.e. the RT address was set to 31 in the 1553B command word
10	Transmit or Receive	TX/RX field from the 1553B command word. '0' indicates receive and '1' transmit
9:5	Sub-address	Sub-address field from the 1553B command word
4:0	Word Count Mode Code	Word count field from the 1553B command word, when the sub-address is 0 or 31 this contains the 1553B mode code

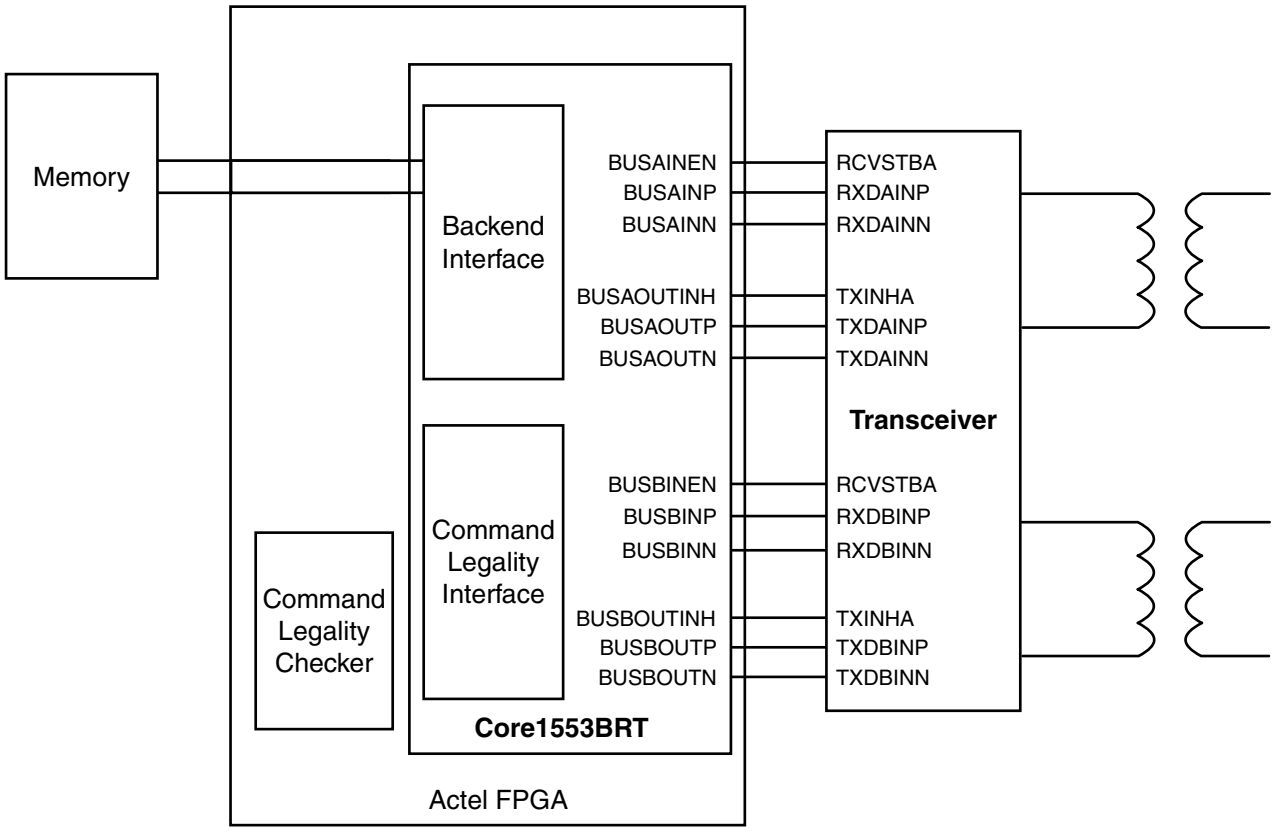


Figure 9 • *Typical CPU and Memory-based RT System*

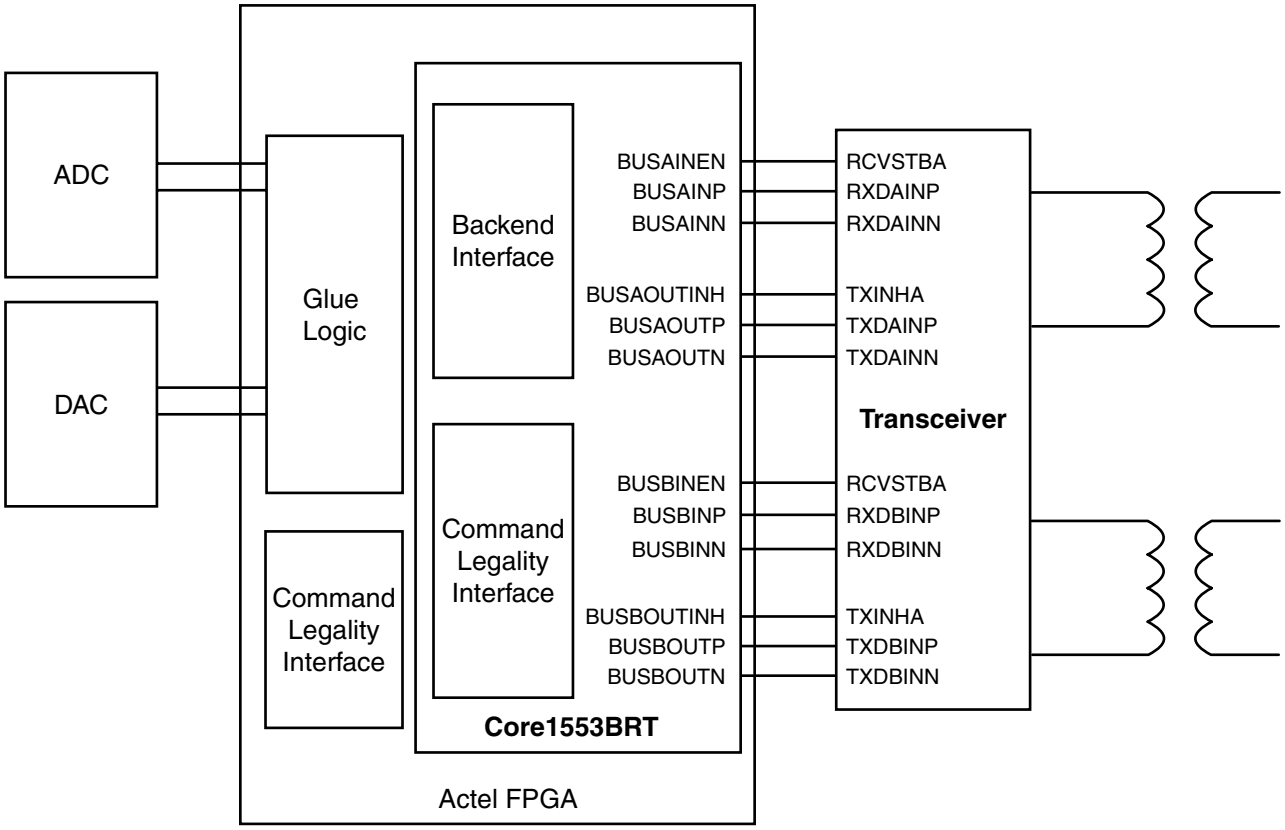
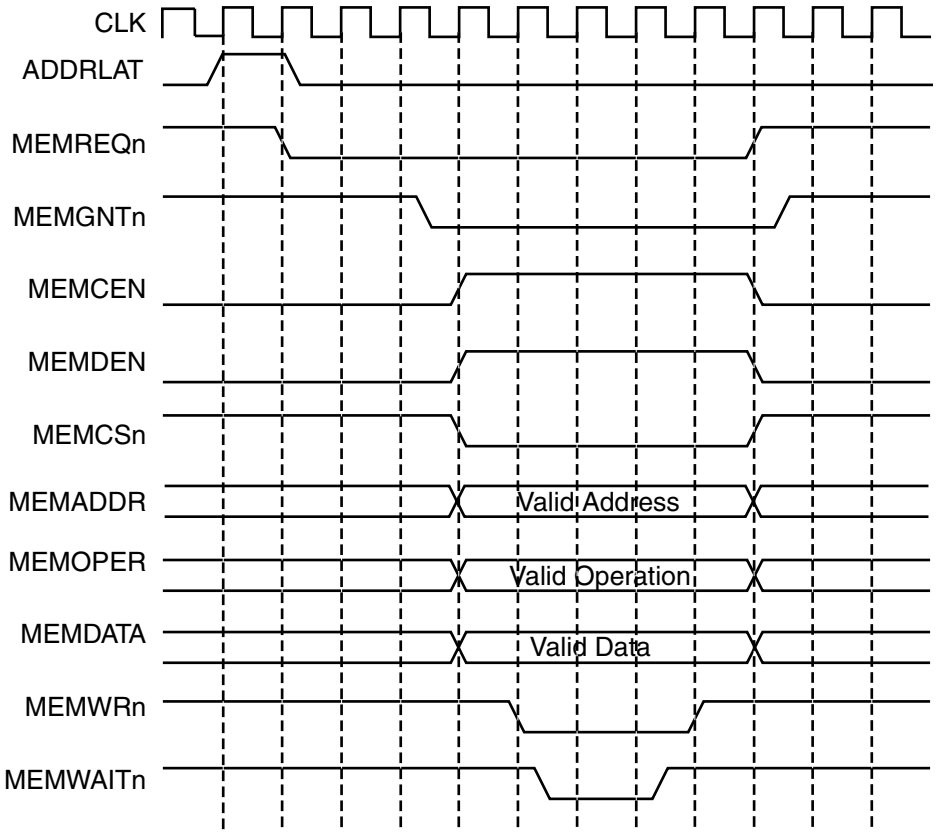


Figure 10 • *Typical Non-Memory-based RT System*

Specifications

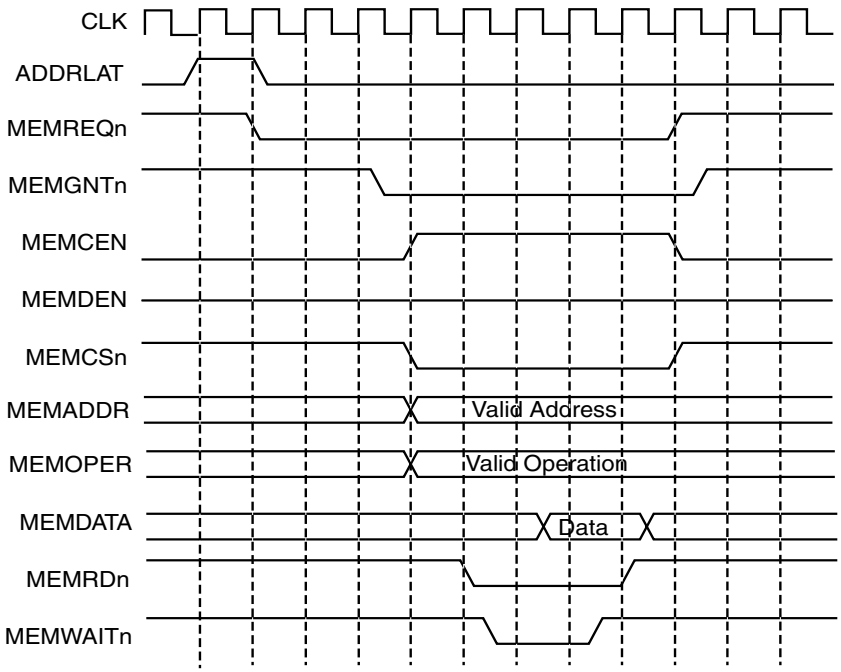
Memory Write Timing – Asynchronous Mode



Memory Write Timing

Sync Mode	Description	at 12 MHz	at 16 MHz
T_{pwWR}	Write pulse width (No wait states)	83.3ns	62.5ns
T_{pdGNT}	Maximum delay from MEMREQn to MEMGNTn active	12.0µs	12.0µs
T_{suDATA}	Data setup time to MEMWRn low	83.3ns	62.5ns
T_{suADDR}	Address setup time to MEMWRn low	83.3ns	62.5ns
T_{hdDATA}	Data hold time from MEMWRn high	83.3ns	62.5ns
T_{hdADDR}	Address hold time from MEMWRn high	83.3ns	62.5ns
T_{suWAIT}	Wait setup to rising clock edge	15.0ns	15.0ns

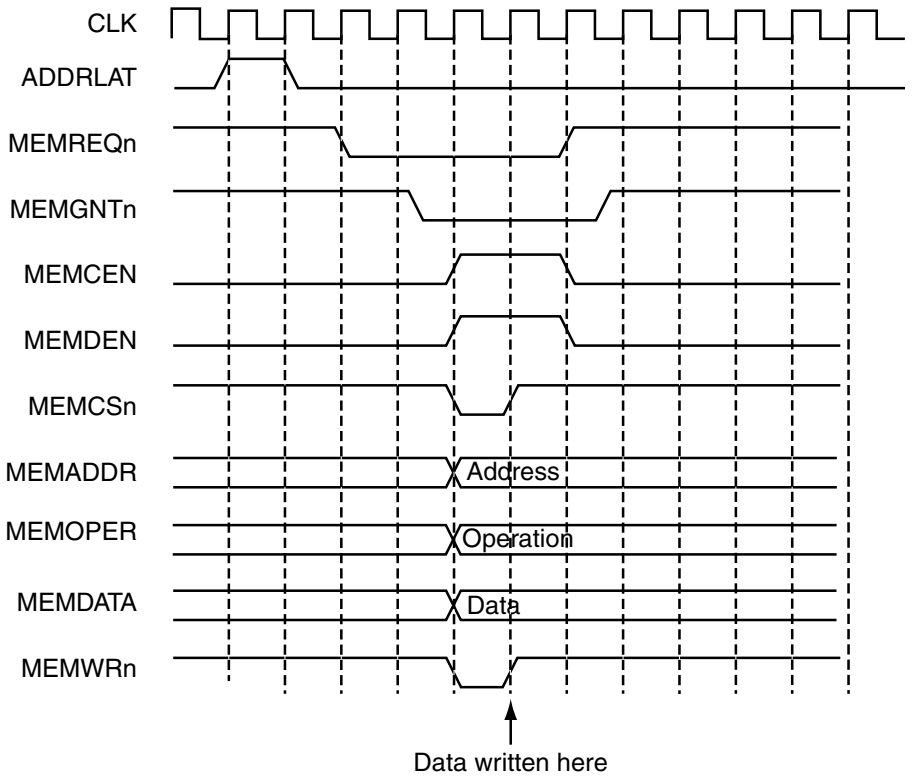
Memory Read Timing – Asynchronous Mode



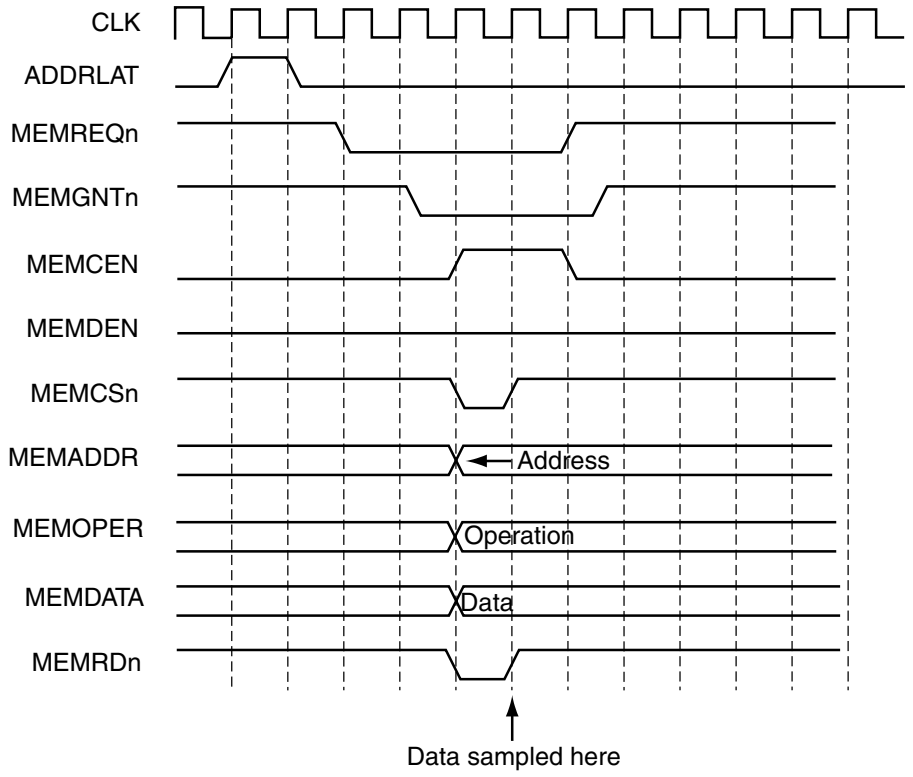
Memory Read Timing

Async Mode	Description	Typical at 12 MHz	Typical at 16 MHz
T_{pwRD}	Read pulse width (No wait states)	83.3ns	62.5ns
T_{pdGNT}	Maximum delay from MEMREQn to MEMGNTn active	12.0µs	12.0µs
T_{suADDR}	Address setup time to MEMRDn low	83.3ns	62.5ns
T_{hdADDR}	Address hold time from MEMRDn high	83.3ns	62.5ns
T_{suWAIT}	Wait setup to rising clock edge	15.0ns	15.0ns
T_{suDATA}	Data setup time to MEMRDn high	15.0ns	15.0ns

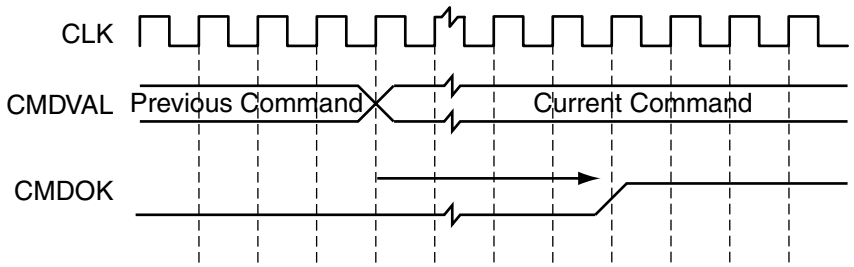
Memory Write Timing – Synchronous Mode



Memory Read Timing – Synchronous Mode



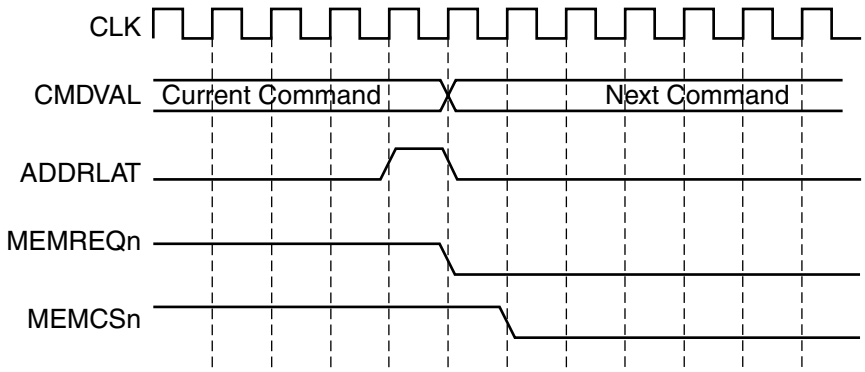
Command Word Legality Interface Timing



Command Word Legality Interface Timing

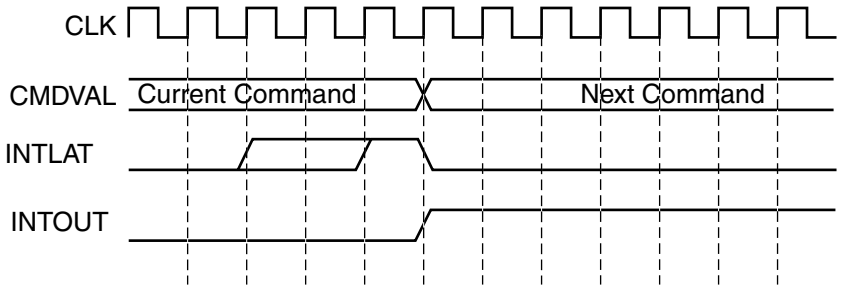
Name	Description	Typical at 12 MHz	Typical at16MHz
TpdCMDOK	Maximum external command word legality decode delay	3µs	3µs

Address Mapper Timing



Note: *This figure shows the worst-case timing when a second 1553B command arrives as the core starts a backend transfer and MEMGNTn is held low.*

Interrupt Vector Extender Timing



Note: *This figure shows the worst-case timing when a second 1553B command arrives as the core asserts an interrupt request. Also, INTLAT may be active for several clock cycles prior to INTOUT.*

RT Response Times

RT response time is from the midpoint of parity bit in the command word to the midpoint of the status word sync (Table 12).

RT-to-RT time out is from the first command word parity bit to the expected sync of the first data word.

Table 12 • RT Response Times

Spec	Description	@ 12 MHz	@ 16 MHz
T_{rtresp}	RT response Time	4.75 to 7.0µs	4.75 to 7.0µs
T_{rtrtto}	RT-to-RT time-out	57µs	57µs
T_{xxto}	Transmitter time-out	704µs	668µs

Ordering Information

Core1553BRT can be ordered through your local Actel sales representative. It should be ordered using the following number scheme: Core1553BRT-XX, where XX is (Table 13):

Table 13 • Ordering Codes

XX	Description
SN	Single-use netlist restricted to Actel devices Core meets MIL-STD-1553B for remote terminal applications and includes testbench
AN	Same as Core1553BRT-SN but with unlimited use on Actel devices
AR	Unlimited use RTL license restricted to Actel devices. Identical functionality as Core1553BRT-SN with VHDL and Verilog source code and synthesis scripts for user customization
UR	Same as Core1553BRT-AR but with unrestricted and unlimited use

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v3.0)	Page
v2.0	Figure 2 on page 2 and Figure 9 on page 16 have been changed.	page 2 page 16
Advanced v0.2	The "Product Summary" section on page 1 was updated.	page 1
	The "General Description" section on page 1 was updated.	page 1
	Figure 1 on page 2 was updated.	page 2
	Table 1 on page 3 was updated.	page 3
	The "1553B Bus Interface" table on page 5 was updated.	page 5
	The "Command Legalization Interface" section on page 7 was updated.	page 7
	Table 2 on page 7 was updated.	page 7
	Table 3 on page 8 was updated.	page 8
	Table 4 on page 9 was updated.	page 9
	The "Status Word Settings" section on page 10 was updated.	page 10
	The "Command Word Storage" section on page 10 is new.	page 10
	The "Mode Codes" section on page 12 was updated.	page 12
	Figure 5 on page 10 was updated.	page 10
	Figure 6 on page 11 was updated.	page 11
	The "Memory Write Timing – Asynchronous Mode" figure on page 18 was updated.	page 18
	The "Memory Read Timing – Asynchronous Mode" figure on page 19 was updated.	page 19
	The "Memory Write Timing – Synchronous Mode" figure and the "Memory Read Timing – Synchronous Mode" figure on page 20 were updated.	page 20
	The Command Word Legality Interface Timing section, Command Word Legality Interface Timing section, and "Interrupt Vector Extender Timing" section on page 21 are new.	page 21
	The "Ordering Information" section on page 22 is new.	page 22
Advanced v0.1	Datasheet is released for certified core.	
	The "General Description" section on page 1 has been updated.	page 1

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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