3200DX Wide Decode Modules

When simple programmable logic devices (PLDs) first became available, designers quickly embraced the new technology. Programmable logic allowed designers to develop and test logic designs quickly and immediately correct design errors. Soon they began to demand larger, more flexible devices so that they could incorporate much of their system into programmable logic. Field Programmable Gate Arrays (FPGAs) extended the programmable logic concept to become more adaptable and encompass many thousands of gates. The increased size, however, did not solve all the system designers' problems. The richness of the FPGA as a design element came at the cost of speed for simpler functions such as address decoding.

Today's digital system designers have a tough job. Their circuits must perform complex and diverse tasks at ever-increasing clock speeds. Further, system designs often need small amounts of fast random-access memory (RAM), which conventional FPGAs don't offer. To date, whatever is available on programmable logic is a simple by-product of the architecture and has limited applicability to system needs. The result has been that system designers have had to add fast PLDs or small SRAMs to their FPGA-based designs in order to meet speed-critical decoding and memory needs. Actel's 3200DX family addresses FPGA limitations that designers have had to work around. In addition to providing high capacities (up to 40,000 gates), this family eliminates the need for additional ICs, because it includes system logic elements such as fast decode and dual-port SRAM blocks.

Address Decoding

Introduction of faster processor-based systems dictates high-speed interface requirements between the modules within these systems. One of the most generic interface issues in microprocessor-based systems is the address decoding task. Figure 1 shows a typical system consisting of a microprocessor and peripheral components. Typically, the N-bit-wide processor address line, along with some control signals, must be decoded. The address is decoded by an address decoder, which generates a chip-select signal for each device in the system. The performance of the address decoder is critical, since the present address on the address line is valid for only a short duration (depending on the system requirements and timing specifications). With the 3200DX devices, a designer no longer needs to implement the address decoder block outside of the FPGA. (The gray box in Figure 1 shows only a few possible blocks suitable to be implemented within a 3200DX device.)

3200DX Family

Actel's 3200DX family of devices provides an array of features such as internal dual-port SRAM, Wide Decode (WD) modules, quadrant clocks, and JTAG compliance. Table 1 summarizes the 3200DX product family.

The WD modules are located at the top and bottom rows of the chip and are indicated by shaded blocks in Figure 2. The modules are accessed through one of three library hard macros. These library elements are shown in Figure 3. One main feature of the WD module is the direct connection to an I/O pin. The module can drive an I/O pin without the usual interconnect delay associated with regular logic modules. To implement the direct I/O connection, the user needs to connect an output buffer of any type (OUTBUF, TRIBUFF, etc.) to the output of the Wide Decode library element (Figure 4). In addition, the output of the WD modules can be routed within the chip for internal connections. Each WD module has a specific I/O module associated with it. Only that I/O module will accommodate its associated WD module with a direct I/O connection. Actel's software will automatically place and route the cell mapped into a WD module to its associated I/O pin.

When to Use the WD Modules

The WD modules offer two main advantages not provided by other Actel library elements:

- A direct I/O connection (not routed) with 0.5 ns delay
- Seven-input AND/NAND function implemented in one logic module

The wide AND/NAND functionality, among other advantages, makes the WD modules suitable for decoding of wide address lines up to 35 bits.

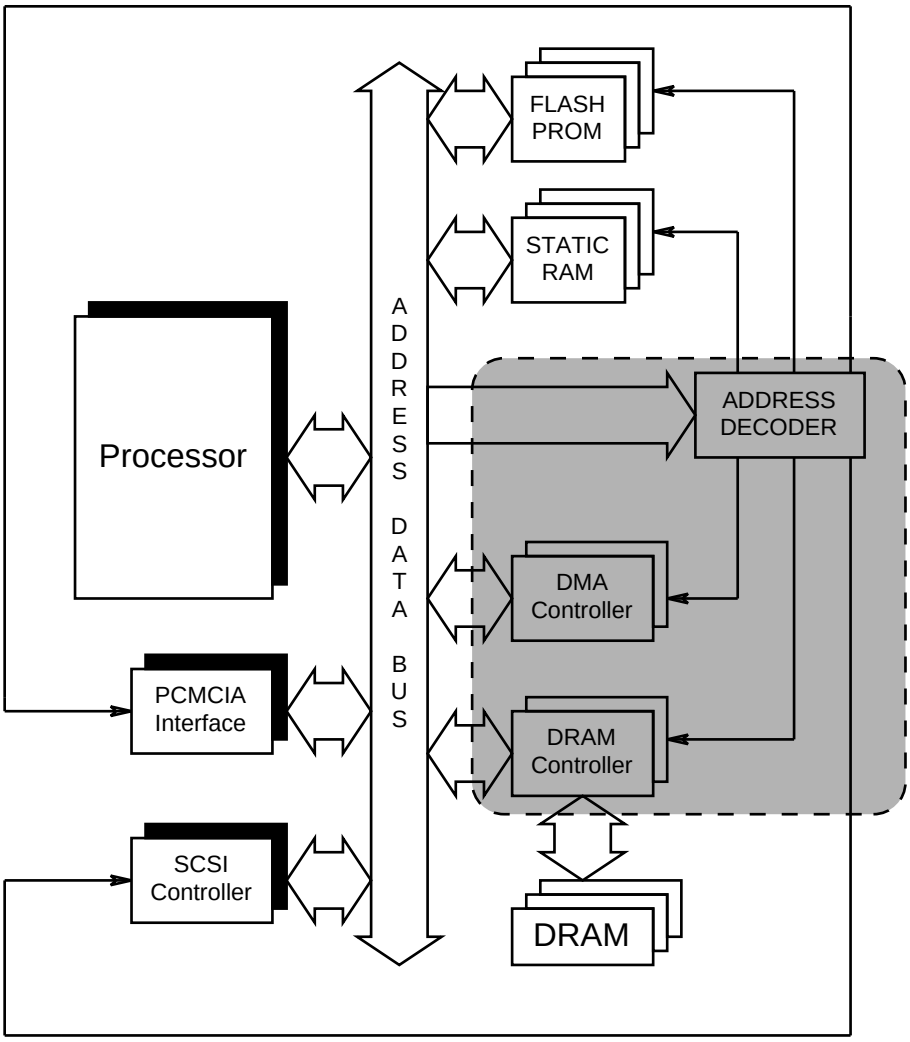

Figure 1 • *Microprocessor-Based System Block Diagram*

Table 1 • *3200DX Family*

	3265DX	32100DX	32140DX	32200DX	32300DX	32400DX
Gates	6,503	9,420	14,210	20,140	30,735	40,000
C-mod	475	662	912	1,184	1,833	2,466
S-mod	510	700	954	1,230	1,888	2,526
I/O max	126	152	176	202	250	288
Wide Decode cells	20	20	24	24	28	28
JTAG	No	Yes	Yes	Yes	Yes	Yes
SRAM bits	0	2,048	0	2,560	3,072	4,096

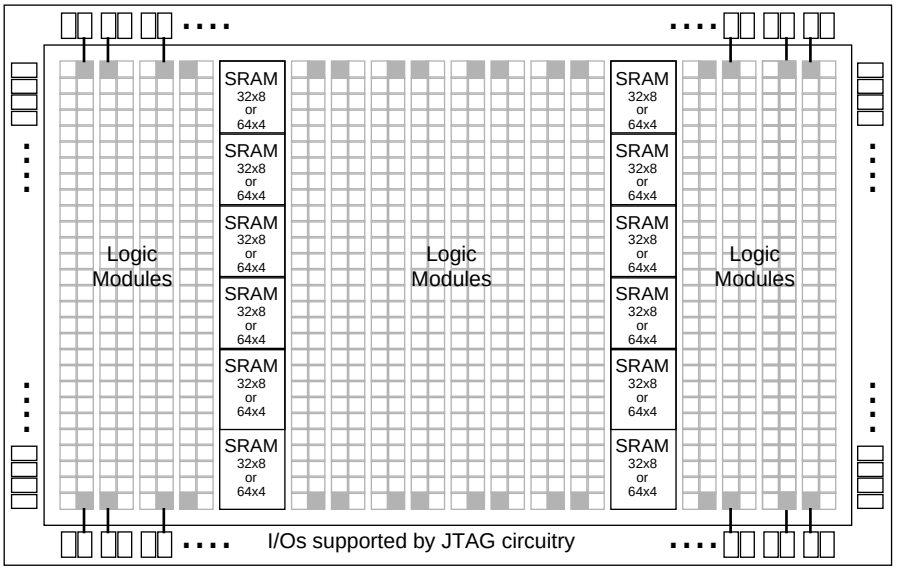

Figure 2 • *3200DX Floor Plan*

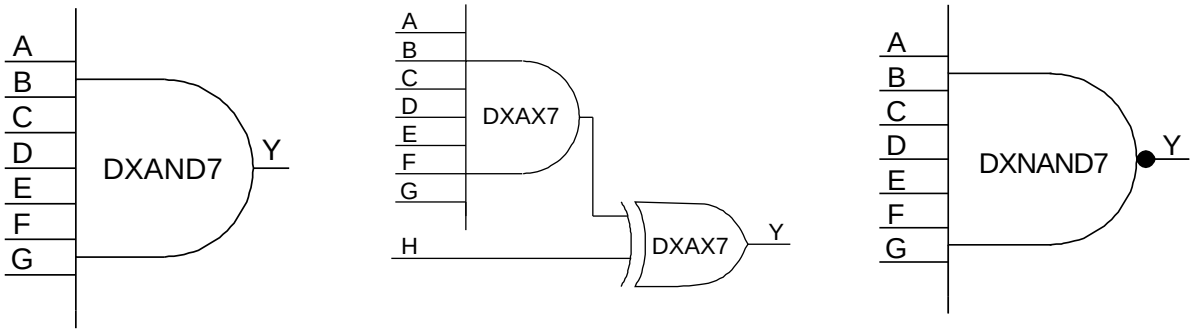

Figure 3 • *Wide Decode Library Elements*

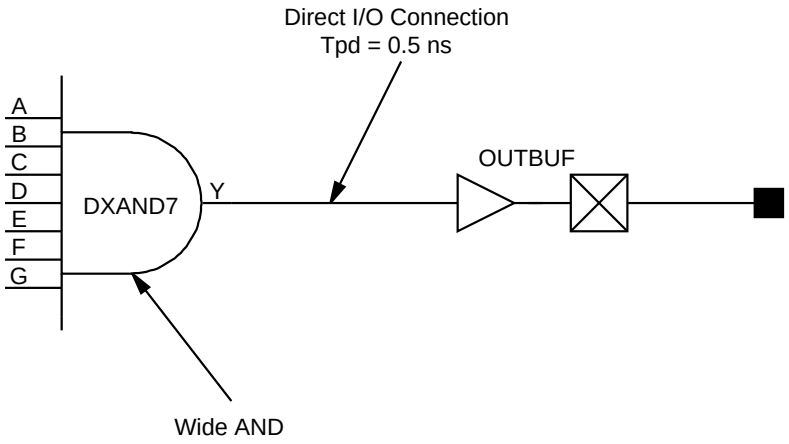

Figure 4 • *WD Module Direct I/O Connection*

The WD module applications reach beyond just address decoders. In general, any critical path of a design in which a wider gate would save a level of logic is an appropriate place to use these modules. Also, if a critical path in your design requires a fast connection to an output pin, the WD modules can be used to accommodate the situation. Another feature that may be useful in an application is the WD module's internal Exclusive-OR. This feature can be exploited by using the DXAX7 library macro (Figure 3).

Implementing Address Decoders

The best way to take advantage of the WD modules when implementing address decoders is to use Actel's macro builder, ACTgen. Figure 5 shows the ACTgen 3.1 graphical user interface. Clicking the Constant Decoder button causes ACTgen's Constant Decoder window to appear, as shown in Figure 6.

From the Constant Decoder menu, you can assign any bit width from 2 to 64. You can enter the constant to be decoded in hexadecimal, decimal, or binary. The address decoder's output sense, along with tristate options, can also be selected by simply clicking the appropriate ACTgen Constant Decoder button.

Constant decoders (or any other block) generated by ACTgen can be used in schematics or high-level language designs. Furthermore, any logic block generated by ACTgen does not need to be simulated functionally at the block level. Only the interface with other blocks needs to be simulated.

For more information on other 3200DX features, such as SRAM blocks and Wide Decode modules, refer to the *FPGA Application Guides.*

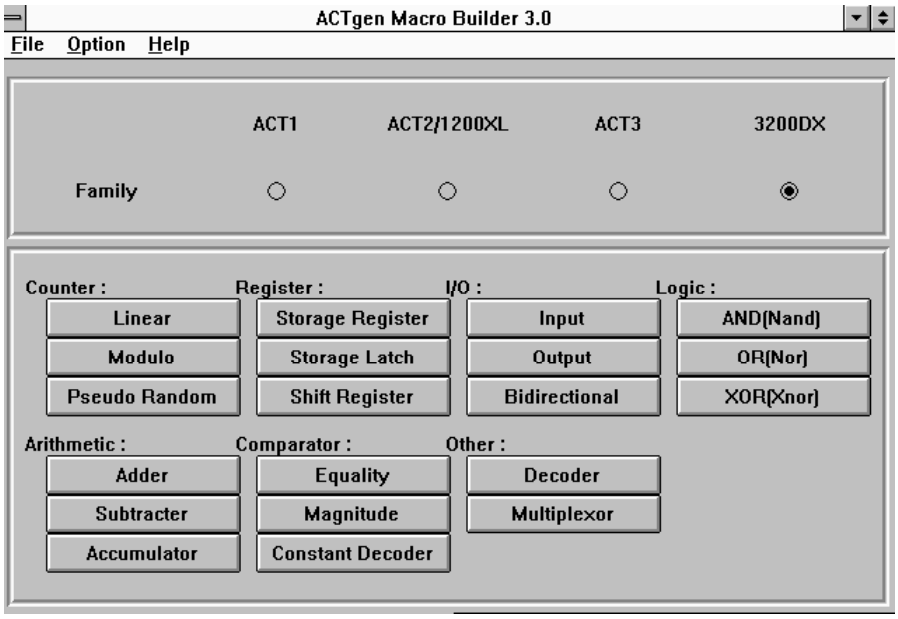

Figure 5 • *Actel Marco Builder, ACTgen 3.0*

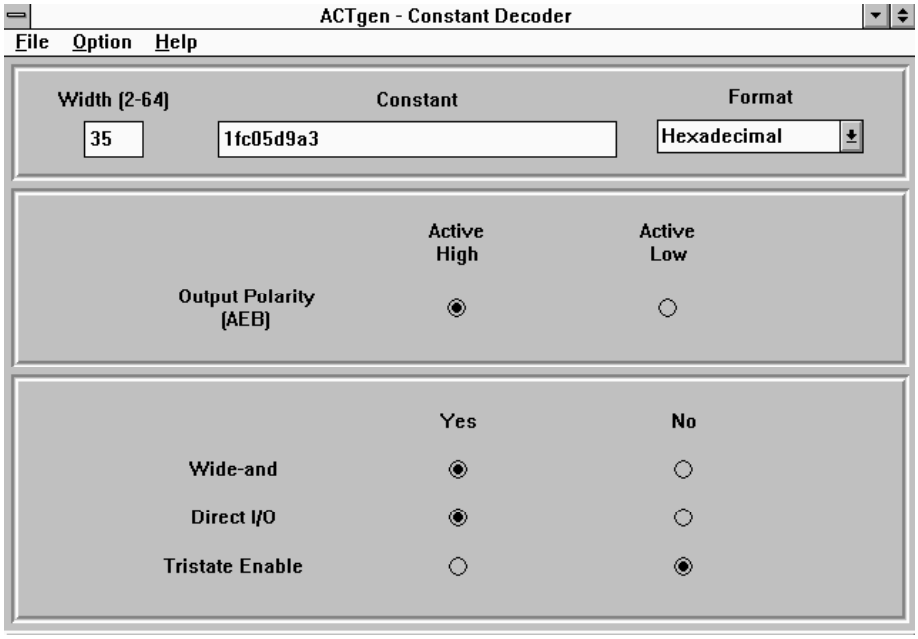

Figure 6 • *ACTgen Constant Decoder*