Using ACT 3 Family I/O Macros

The ACT 3 family from Actel has a complex I/O macro which allows users to implement high speed complex functions entirely in the I/O. Common functions like shift registers operating at 160 MHz, state machines and counters with 7.5 ns clock-to-output (pin-to-pin) and 160 MHz pipeline registers are all implementable in ACT 3 I/Os. This significantly increases capacity and I/O performance of ACT 3 devices over previous generations of FPGAs. This application note covers several examples of how designers can use these powerful I/O macros in real world applications.

ACT 3 I/O Architecture

The ACT 3 family architecture is shown in Figure 1. The logic array consists of rows of Sequential and Combinatorial logic cells with routing channels in between, much like a channeled gate array. I/O modules are located at the periphery of the array. Each I/O module is used to interconnect device signal pins to array inputs and outputs. The I/O module contains specialized circuitry to assist the designer in getting signal on and off chip. Figure 2 shows the detailed block diagram of the ACT 3 I/O module.

I/O Module

The main function of the ACT 3 I/O module is to provide a high-speed high-functionality interface between the pins of the device and the logic array. Data to/from the logic array arrives on the left side of Figure 2. U01 and U02 are the data from the array and 'Y' is the data to the array. The pad is shown on the far right side of Figure 2 and is the input/output pin of the device. Data from the array may be registered in the output register or bypassed using the OTB control signal. If registered, the data may be selectively loaded or held via the synchronous enable signal ODE and asynchronously initialized to a logic Low or High via the IOPCL input. The output drivers have both an individual slew control and individual output enable. The Preset/Clear, OTB, and Slew features are usually automatically determined when the user selects the desired I/O macro. For example, the I/O macro ORECTH shown in Figure 3A uses a Clearable output register with High Slew. Correct selections of OTB, Preset/Clear, and Slew are made automatically. Another feature of the I/O macro is the ability to feedback the contents of the output register back to the logic array. This allows embedded functions like state machines and shift registers to be easily implemented in the IO macro. Figure 3B shows the FECTML macro and the feedback multiplexor used to select between the output register and the device pad.

When data is sourced from the device pad, the input register can be used to capture incoming data. The input register has a synchronous data enable and a Preset/Clear feature similar to the output register. The IDE and IEN signals are used to control the Y multiplexer and the data enable multiplexer and provide the most commonly needed input functions. Again, these signals are usually determined automatically when the user selected the desired macro. For example, the IREC input register macro is shown in Figure 3C and has IDE, IEN, and Preset/Clear predetermined to implement the desired functions.

Actel provides an automatic software tool (ACTgen Macro Builder) to help in implementing a wide range of I/O functions in ACT 3 devices. The designer can select the width of the macro and a variety of operating modes with a few mouse clicks. A sample menu from ACTgen is shown in Figure 4.

Table 1 • *ACT 3 I/O Macro Performance*

Input Features	
Input Timing Register	167 MHz
Input Pipeline Register	167 MHz
Pulse Stretching Input Register	120 MHz
Input Synchronization	167 MHz
Input Address Holding Register	164 MHz
Input Control Register	167 MHz
Output Functions	
State Machine Output Register	135 MHz
Output Shift Register	167 MHz
Output Pseudo Random Counter	131 MHz
Output Datapath	131 MHz
Bi-Directional Functions	
Bi-Directional Registers	167 MHz

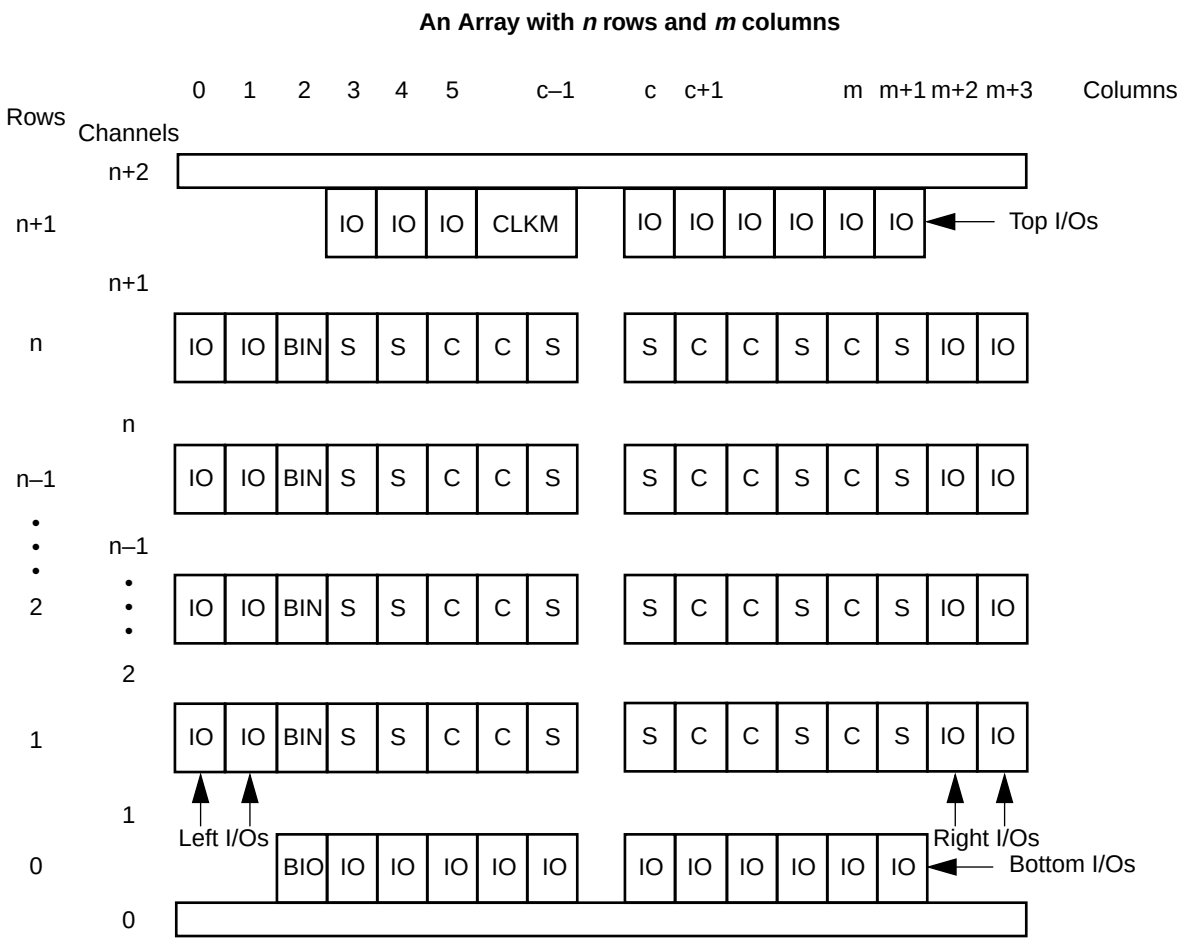


Figure 1 • *Generalized Floor Plan of ACT 3 Device*

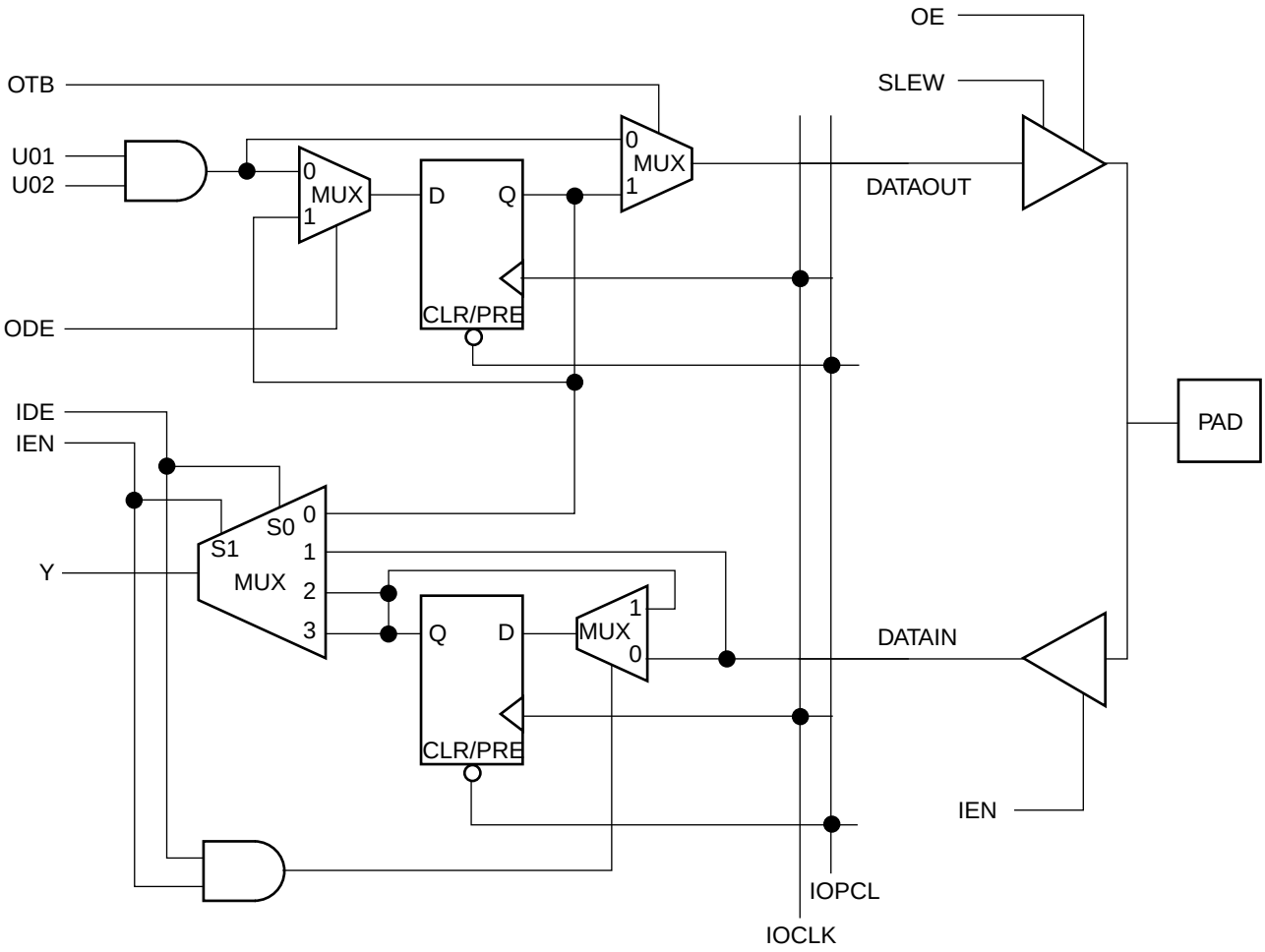
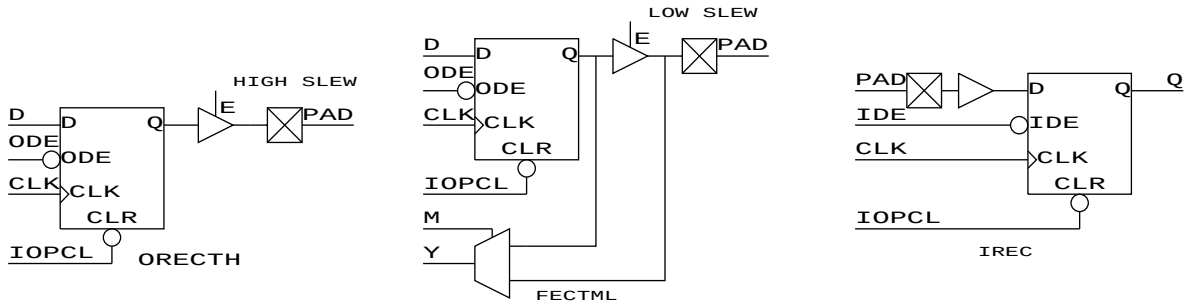


Figure 2 • I/O Macro Block Diagram



3A **3B** **3C**

Figure 3 • I/O Macro Implementations

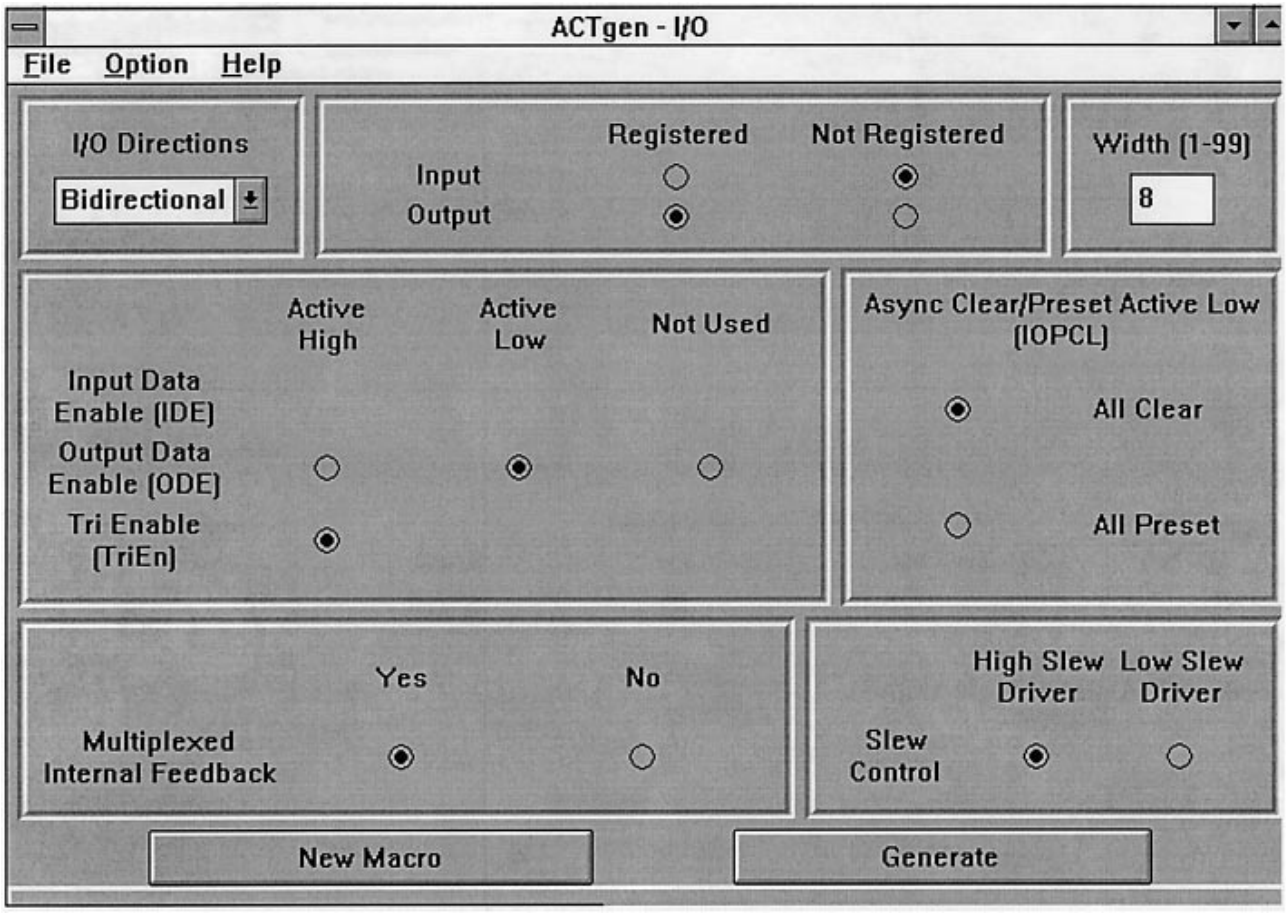


Figure 4 • *ACTgen Selection of ACT 3 I/O Functions*

Every registered ACT 3 I/O macro (for example, DECETH, IREC, and OREPTL) includes an asynchronous preset or clear input IOPCL. This input asynchronously sets the output of I/O flip-flops to 0 or 1. The IOPCL pin of a registered I/O macro must be driven by the dedicated I/O macro, IOPCLBUF. The IOPCLBUF is externally driven in turn by the dedicated IOPCL package pin as shown in Figure 5.

Similarly, the clock (CLK) inputs of registered I/O macros are driven by a dedicated circuit. The dedicated I/O clock buffer, IOCLKBUF, is used to drive the clock pin of each I/O macro. The IOCLKBUF is driven in turn by the dedicated external package pin, IOCLK, as shown in Figure 6. See the package pin assignment diagrams in the ACT 3 data sheet for specific locations of the IOPCL and IOCLK package pins.

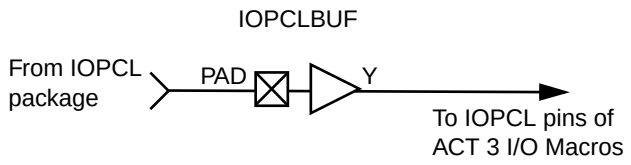


Figure 5 • An IOPCLBUF Driven by a Dedicated IOPCL Package Pin

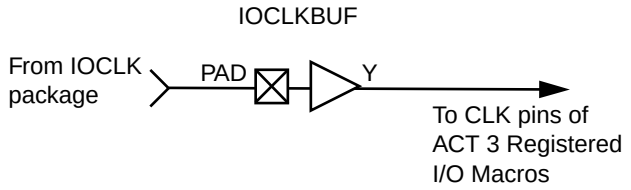


Figure 6 • An IOCLKBUF Driven by a Dedicated IOCLK Package Pin

If no registered I/O macros are used in an ACT 3 design, then the dedicated IOCLK and IOPCL package pins can be used as normal I/O pins. In that case, these pins can be connected to any other type of I/O buffer except IOCLKBUF, IOPCLBUF, and HCLKBUF. For example, undedicated normal I/O buffers such as INBUF and OUTBUF may be connected to these pins. If any registered I/O macros are used in an ACT 3 design, then the IOCLKBUF and IOPCLBUF macros must be included in the design, and the pin assignment must include the IOPCL and IOCLK pins. The IOPCL and IOCLK pins must be explicitly specified because the Designer Series software will not automatically create pin assignments for IOCLKBUF and IOPCLBUF.

In an ACT 3 design, all types of I/O macros can be used in a single design. For example, I/O macros without registers, I/O macros with preset, and I/O macros with clear can be used together in one design. However, IOCLKBUF must drive all the clock inputs of the registered I/O macros and the IOPCL must drive all the clear or preset inputs of the registered I/O macros. CLK and IOPCL pins of registered I/O macros cannot be connected to GND or V_{CC}. All ACT 3 I/O registered buffers share the same dedicated clock and asynchronous clear or preset network. Once the built-in dedicated IOCLK and IOPCL networks are used, all registered I/O macros will be cleared and preset at the same time by the same signal.