Actel's Antifuse FPGAs
Programmable ASIC Solutions

Space Electronics
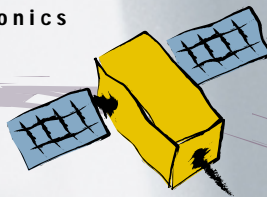
**Communications
Infrastructure**

e-Appliances

Actel

## The Antifuse Advantage

Actel's antifuse devices are low-cost, high-performance solutions for today's logic designer. Ideal for integrating logic typically implemented in multiple CPLDs, PALs, and FPGAs, antifuse devices offer significant cost savings while maintaining high performance. In addition, the Actel antifuse technology ensures design security and gets your design to market faster than an ASIC. Actel antifuse FPGAs combine the benefits of programmable logic and ASICs for a "programmable ASIC solution."
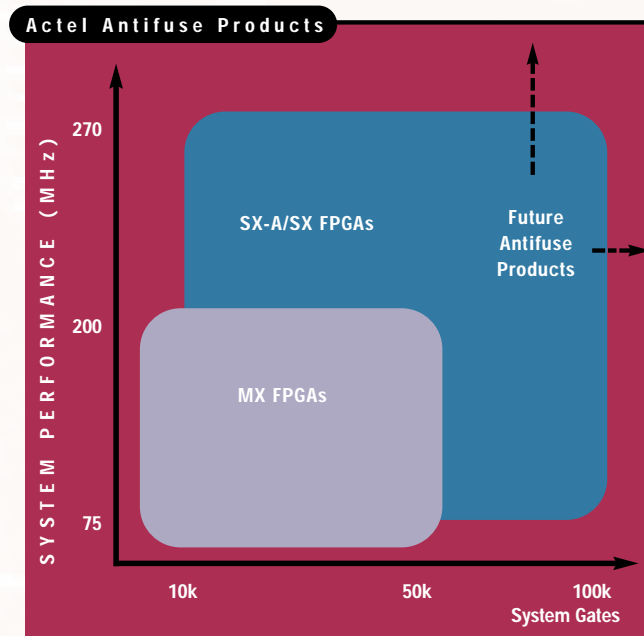
Save Money

With a smaller switching element and a smaller die size, Actel's antifuse FPGAs provide a substantial cost advantage over equivalent SRAM FPGAs. Plus, Actel's antifuse FPGAs are nonvolatile, enabling them to retain their configuration indefinitely and without an external storage device. With no external storage device necessary to hold the configuration data, the need for a PROM or microprocessor and the associated board space are eliminated, providing additional cost savings.
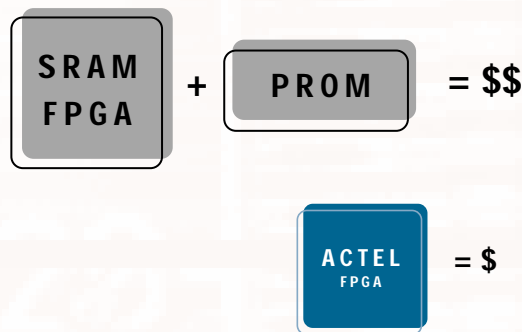
Maintain High Performance

Low cost does not mean low performance. With its low resistance and low capacitance properties, Actel's antifuse technology offers very high speeds. And since Actel devices are permanently programmed, they are instantly operational on power-up. There is no boot-up period while data is being downloaded from an external device.

SRAM FPGA + **PROM** = **$$**

ACTEL FPGA = **$**

Actel Antifuse Products

SYSTEM PERFORMANCE (MHz)

270

200

75

SX-A/SX FPGAs

MX FPGAs

Future Antifuse Products

10k   50k   100k
System Gates

Protect Your Intellectual Property

Design security is a necessity in today's highly competitive technology industry to protect designs from theft. Actel's antifuse FPGAs offer that security. Actel devices do not need a start-up bitstream, eliminating the possibility of configuration data being intercepted. This also prevents in-system errors and accidental data erasures that otherwise may occur during download.

Add to that the inherent security of the antifuse technology itself. The antifuses that form the interconnections within an Actel FPGA are extremely small, are densely distributed throughout the device (over 6.5 million on the largest Actel device), and do not leave an observable signature that can be electrically probed or visually inspected. With these safeguards, Actel devices are virtually immune to copying and reverse engineering.

Speed Time-to-Market

Actel devices offer a host of other benefits that simplify the design cycle and speed the design to market. Using Actel's automatic place-and-route tools, 100% logic utilization is possible, speeding
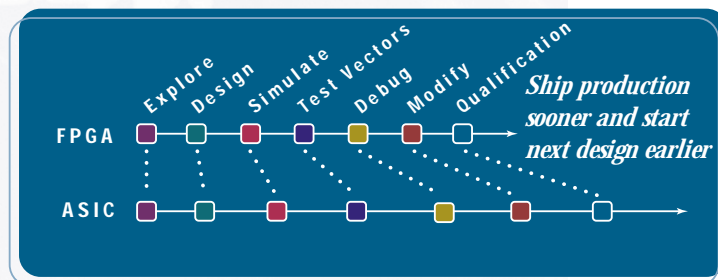
SX-A Power Consumption

Power Consumption (Watts) vs Frequency (MHz)
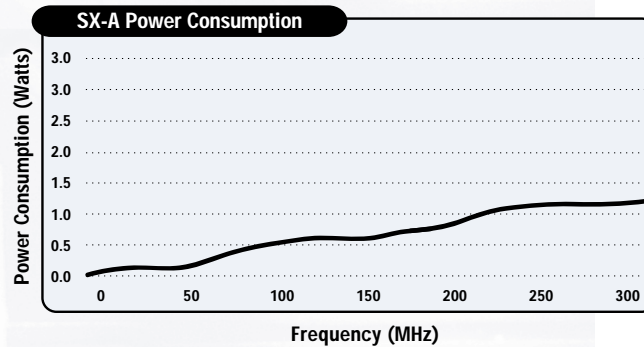
Based on an A54SX08A device with all registers toggling at clock speed.

design time. And Actel's unique general and local routing structure allows 100% pin-locking, even at full logic utilization, so the PCB can be developed concurrently with the FPGA. Even during verification, Actel devices can be observed on the board and in real time using the Silicon Explorer diagnostic tool, decreasing verification times.
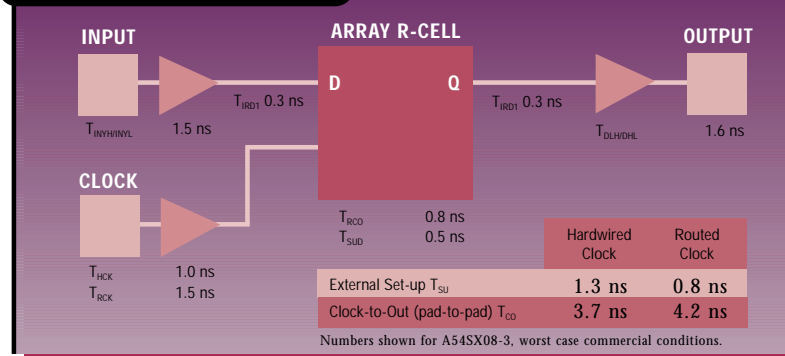
Consume Less Power

An additional benefit of Actel's antifuse technology is its inherently low power consumption. Antifuses have low resistance properties, and the architecture does not require active circuitry to hold a charge, reducing thermal and power supply design problems.

FPGA: Explore, Design, Simulate, Test Vectors, Debug, Modify, Qualification

ASIC

Ship production sooner and start next design earlier

SX-A/SX I/O Performance

INPUT	**ARRAY R-CELL**	**OUTPUT**

T_{IRD1} 0.3 ns (D — Q) T_{IRD1} 0.3 ns

$T_{INYH/INYL}$ 1.5 ns

$T_{DLH/DHL}$ 1.6 ns

CLOCK

T_{RCO} 0.8 ns
T_{SUD} 0.5 ns

T_{HCK} 1.0 ns
T_{RCK} 1.5 ns

	Hardwired Clock	Routed Clock
External Set-up T_{SU}	1.3 ns	0.8 ns
Clock-to-Out (pad-to-pad) T_{CO}	3.7 ns	4.2 ns

Numbers shown for A54SX08-3, worst case commercial conditions.

With capacities ranging from 12,000 to 108,000 system gates, 270 MHz system performance, and prices competitive with those of ASICs, Actel's SX-A/SX FPGAs are the high-performance, low-price leader. Featuring a sea-of-modules architecture, these devices are able to deliver integration at performance levels previously limited to ASICs.

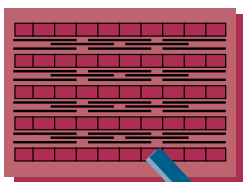### Sea of Modules—An Evolution in Architecture

The sea-of-modules architecture is enabled by Actel's patented metal-to-metal antifuse interconnect elements. The unique architecture consists of a grid of fine-grained logic modules covering the entire floor of the device, reducing the distance signals have to travel between logic modules, and saving almost 1/2 the die size of an equivalent FPGA with a traditional channel array architecture. The result is that SX-A/SX devices cost less overall than other FPGAs of comparable density.

Speed Things Up

To minimize signal propagation delays, SX-A/SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation, optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. This unique local and general routing structure provides fast and predictable performance, allowing designers to meet their goals with minimum effort.

Further complementing the flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation delays with a maximum clock skew of only .25 ns. With internal clock speeds of 330 MHz and clock-to-out performance of 3.7 ns, designs previously limited to ASICs can now be implemented in Actel's SX-A/SX FPGAs.

Channel Array Architecture

Sea-of-Modules Architecture

Metal 3

Metal-to-Metal Antifuse

Metal 2   Metal 2

Via

Metal 1

Contact

Silicon
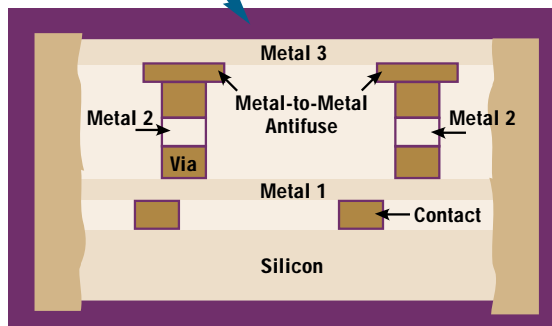
Metal-to-Metal Antifuse

Performance

SX-A/SX devices allow designers to achieve a higher level of performance without using complicated and time consuming performance-enhancing design techniques, such as redundant logic, data pipelining, or instantiation of custom macros in VHDL or Verilog-HDL code.
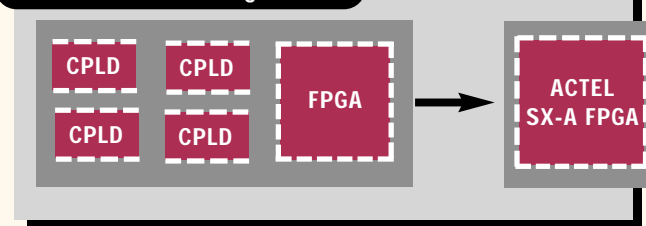
66 MHz PCI Compliance

With the SX-A/SX FPGAs, designers can implement high speed 66 MHz PCI applications. In conjunction with SX-A/SX devices, Actel offers a suite of intellectual property (IP) cores intended to enhance time to market for programmable logic users.
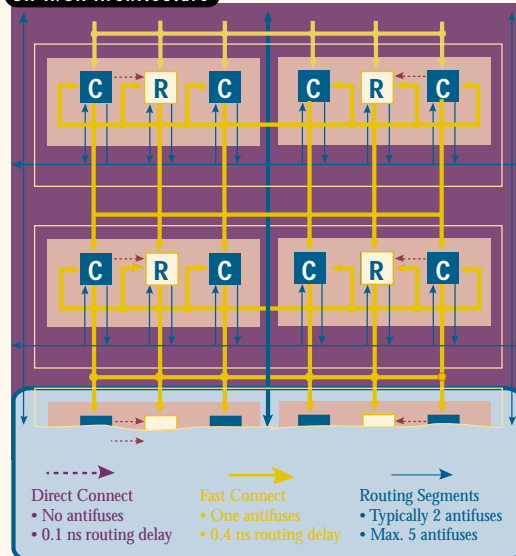
Low Cost of Integration

Ideal for integrating designs that were previously segmented between CPLDs for speed and FPGAs for capacity, SX-A/SX devices offer a low-cost, single-chip solution.

Designs can now be easily integrated into a single SX-A/SX FPGA, improving system reliability and simplifying system integration. Integration also typically results in 1/3 the power consumption of comparable CPLDs and FPGAs. And, of course, fewer components means reduced production costs associated with component counts and board space.

CPLD/FPGA Integration

SX-A/SX Architecture

Direct Connect
• No antifuses
• 0.1 ns routing delay

Fast Connect
• One antifuses
• 0.4 ns routing delay

Routing Segments
• Typically 2 antifuses
• Max. 5 antifuses

SX-A/SX Applications

- *8b/10b encoder for 1 Gigabit Ethernet Router with 125 Mbyte/sec sustained data throughput.*

- *66 MHz compliant PCI Bus Arbiter with a 6 ns clock-to-out and 3 ns input setup time.*

- *Interfacing and control logic in OC-192 10Gb/s line cards.*

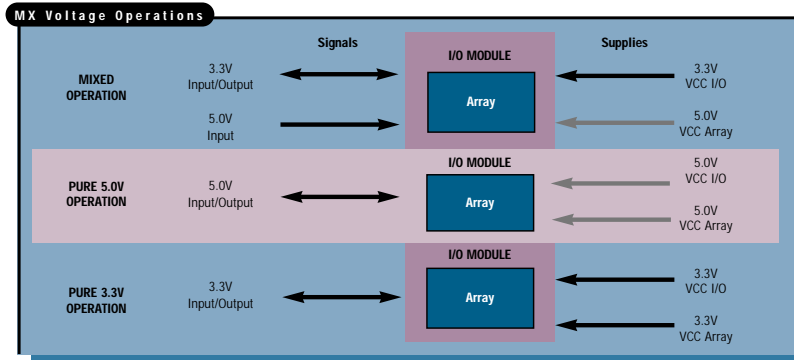- *Synchronizes DRAM control for ATM/SAR processor in ATM switch.*

MX FPGAs

5.0V Leader

With capacities ranging from 3,000 to 54,000 system gates, 250 MHz system performance, and clock-to-out delays as low as 5.6 ns, Actel's MX family of FPGAs offers high-performance 5.0V solutions.

A Mixed-Voltage Solution

Actel's 42MX family of FPGAs includes MultiPlex I/O, an architectural feature that supports mixed-voltage systems and delivers high-performance operation at 5.0V.

Embedded Dual-Port SRAM

The A42MX36 device contains embedded dual-port SRAM modules. With a 5 ns access time, this device allows designers to build on-board FIFOs and buffers with up to 100 MHz performance. These SRAM modules have been optimized for synchronous and asynchronous applications. The modules are arranged in 256-bit blocks that can be configured 32x8 or 64x4. They can also be cascaded together to form memory spaces of user-definable width and depth.

MX Voltage Operations

	Signals	I/O MODULE	Supplies
MIXED OPERATION	3.3V Input/Output / 5.0V Input	Array	3.3V VCC I/O / 5.0V VCC Array
PURE 5.0V OPERATION	5.0V Input/Output	Array	5.0V VCC I/O / 5.0V VCC Array
PURE 3.3V OPERATION	3.3V Input/Output	Array	3.3V VCC I/O / 3.3V VCC Array

42MX FPGAs can operate in 5.0V-only systems, 3.3V-only systems, and mixed 5.0V/3.3V systems, which allow for 5.0V input tolerance in a 3.3V system while providing maximum internal performance. This feature provides flexibility when working with mixed-voltage systems by ensuring compatibility between devices of different voltages.

PCI Compliant

The MultiPlex I/O feature allows for chipwide selection of PCI output drives, enabling 100% PCI compliance for both 5.0V and 3.3V I/O systems. In systems that do not require PCI, the PCI output drivers can be disabled to minimize switching currents.

MX Applications

- *MP3 Player keypad control, error correction decode, and memory interfacing.*

- *Digital Camera lens motor control, color and brightness control, memory and microprocessor interfacing.*

- *A flight controller system used Actel's software and an A42MX16 to meet density and performance requirements and production commitments in ten weeks.*

Design Services — The One Stop Design Solution

With a ten-year history of providing hardware and software services, Actel's *Protocol* Design Services group offers its customers design support at all stages of project development. With extensive knowledge of FPGA design and prototyping, services are delivered on time, within budget, and to the customers' specifications.

Development Software

The DeskTOP series brings together the best in silicon, synthesis, and simulation to create a complete and integrated design environment for designing Actel FPGAs. The basic **DeskTOP** is an integrated development environment, including simulation, synthesis, and place-and-route tools, for designs less than 50k gates.

DeskTOP Pro increases the design simulation limit to 400k gates with unlimited synthesis, allowing designers to move up as their skills and density requirements to increase.

DeskTOP Open, which includes simulation up to 400k gates, and place-and-route tools, is ideal for ASIC designers who are starting to use FPGAs in their designs, but have already invested in synthesis tools.

Designer Series is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place-and-route and analysis tools, and the Silicon Sculptor and APS device programming software.

Real-Time Device Verification

Actel's antifuse FPGAs contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use 18-channel logic analysis system. Silicon Explorer enables designers to complete real time in-system verification at system rates up to 100 MHz, without leaving their desks.
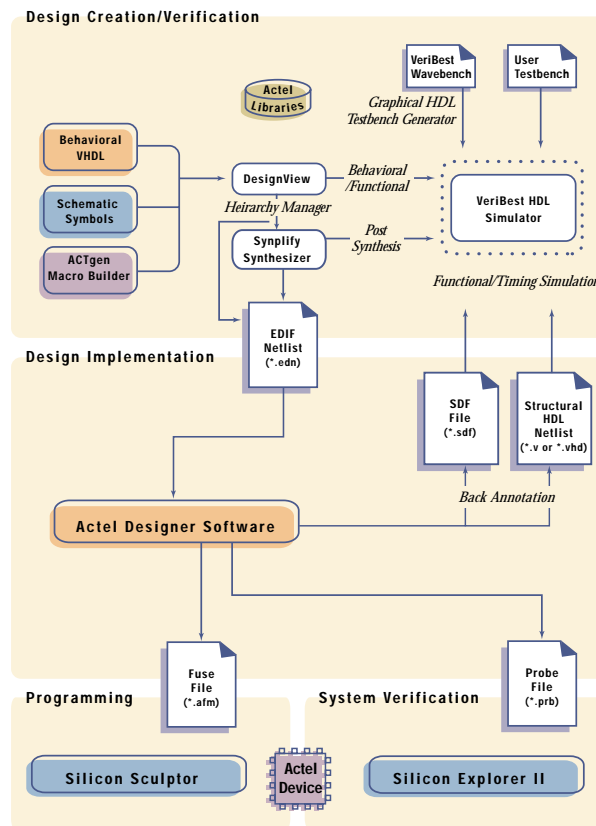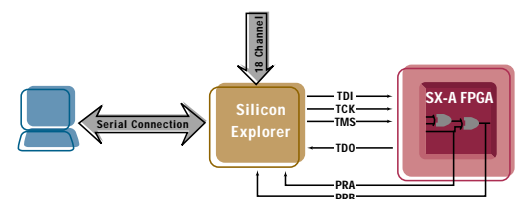
Programming

Actel offers many programming options, including Silicon Sculptor single-site and multisite device programmers that support all Actel device families. For high-volume production programming needs, we offer volume programming services, through our distribution partners.

33/66 MHz, 32/64-Bit PCI Cores

Actel offers the most flexible and cost-effective PCI solution in the FPGA market. Actel's CorePCI is available as a portable, soft RTL macro. Designed to be fully compliant to PCI Specification 2.2, the macro is capable of 33/66 MHz, 32/64-bit implementations with fully compliant zero-wait-state PCI transfer.

Design Creation/Verification

VeriBest Wavebench | User Testbench

Actel Libraries

Behavioral VHDL
Schematic Symbols
ACTgen Macro Builder

DesignView
Heirarchy Manager
Synplify Synthesizer

Graphical HDL Testbench Generator
Behavioral /Functional
Post Synthesis

VeriBest HDL Simulator

Functional/Timing Simulation

EDIF Netlist (*.edn)

Design Implementation

SDF File (*.sdf) | Structural HDL Netlist (*.v or *.vhd)

Back Annotation

Actel Designer Software

Programming
Fuse File (*.afm)

System Verification
Probe File (*.prb)

Silicon Sculptor | Actel Device | Silicon Explorer II

18 Channel
Serial Connection
Silicon Explorer
TDI / TCK / TMS / TDO
SX-A FPGA
PRA / PRB

SX-A/SX FPGA Family Selector Guide

Part Number	A54SX08/SX08A	A54SX16/SX16A	A54SX16P	A54SX32/SX32A	A54SX72A
Capacity (System Gates)	12,000	24,000	24,000	48,000	108,000
Boundary Scan	YES	YES	YES	YES	YES
PCI Compliant	YES*	YES*	YES	YES*	YES
Maximum I/Os	130	180	177	249	360
Dedicated Flip-Flops	256	528	528	1,080	2,012
Logic Modules	768	1,452	1,452	2,880	6,036

SX-A only

MX FPGA Family Selector Guide

Part Number	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity (System Gates)	3,000	6,000	14,000	24,000	36,000	54,000
Mixed Voltage	-	-	YES	YES	YES	YES
PCI Compliant	-	-	-	-	YES	YES
Maximum I/Os	57	69	104	140	176	202
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Logic Modules	295	547	684	1,232	1,890	2,438
Dual-Port SRAM Bits	-	-	-	-	-	2,560

PCI in Actel FPGAs

	32-Bit		64-Bit	
	33MHz	66MHz	33MHz	66MHz
Target	SX16A SX32A SX72A MX24*	SX16P SX16A SX32A	SX32A SX72A	SX32A
Master/Target	SX16A SX32A SX72A MX24*	SX16P SX32A	SX32A SX72A	SX32A
Master	SX16A SX32A SX72A MX24*	SX16P SX32A	SX32A SX72A	SX32A

PCI support in MX with CorePCI Version 5.11 only

For more information about Actel's products, call 1.888.99.ACTEL or visit our Web site at http://www.actel.com

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