Axcelerator Family FPGAs

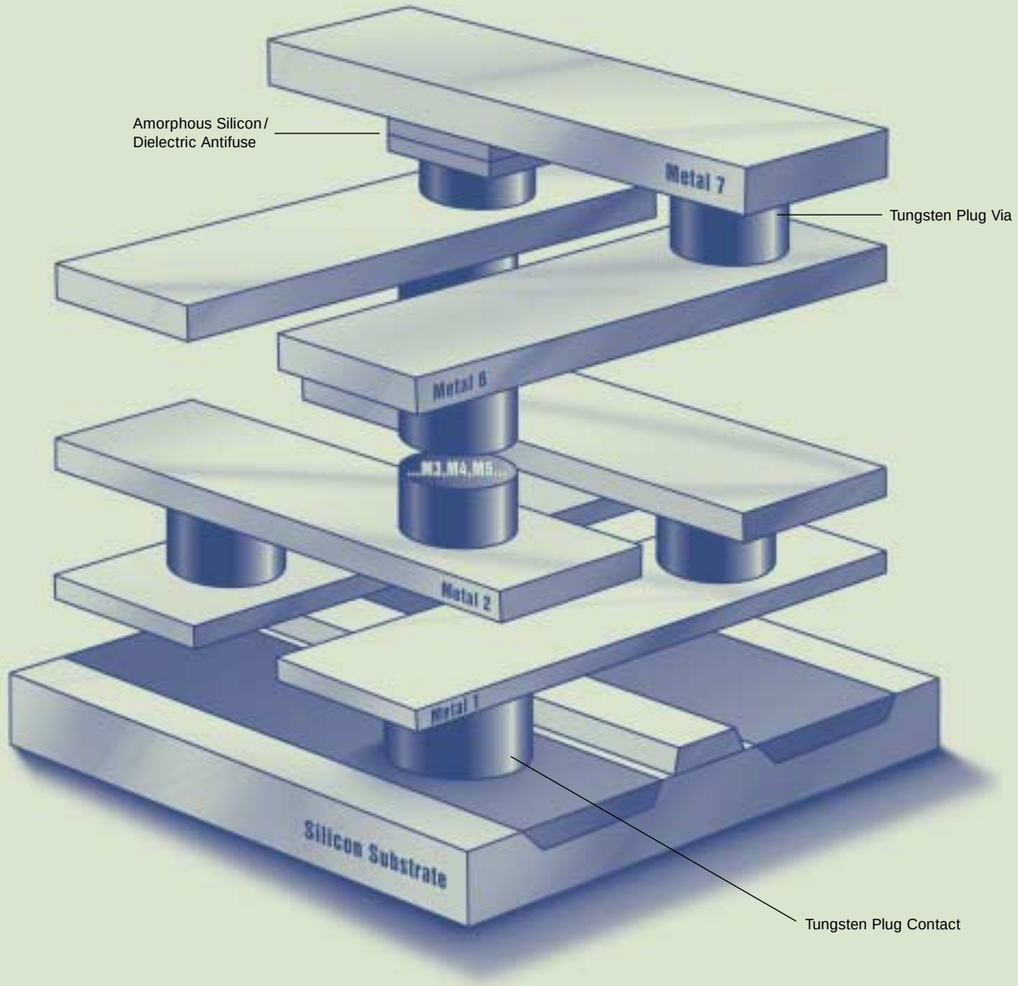
Key Features

- 350 MHz System/500 MHz Internal Performance
- 2 Million Equivalent System Gates
- Up to 339kbits Embedded SRAM with FIFO Logic
- Flexible Multiple Standard I/Os
- Innovative 64-bit PerPin FIFO
- 8 Embedded 1 GHz PLLs
- Secure
- Nonvolatile

FuseLock™

First for Speed and Performance. Accept Nothing Less.

The Axcelerator family of antifuse FPGAs takes performance to new levels. Manufactured on a .15µm antifuse process with 7 layers of metal, the Axcelerator family is a single-chip, nonvolatile solution that offers high densities, flexible I/Os, and unique logic to enable implementation of high performance, high gate count designs. Built on Actel's innovative sea-of-modules architecture, Axcelerator FPGAs are designed to deliver 100% pure performance with low power consumption, high logic utilization, unprecedented design security and the world's fastest FPGA core.



Seven Layers of Metal

Actel | Axcelerator Family

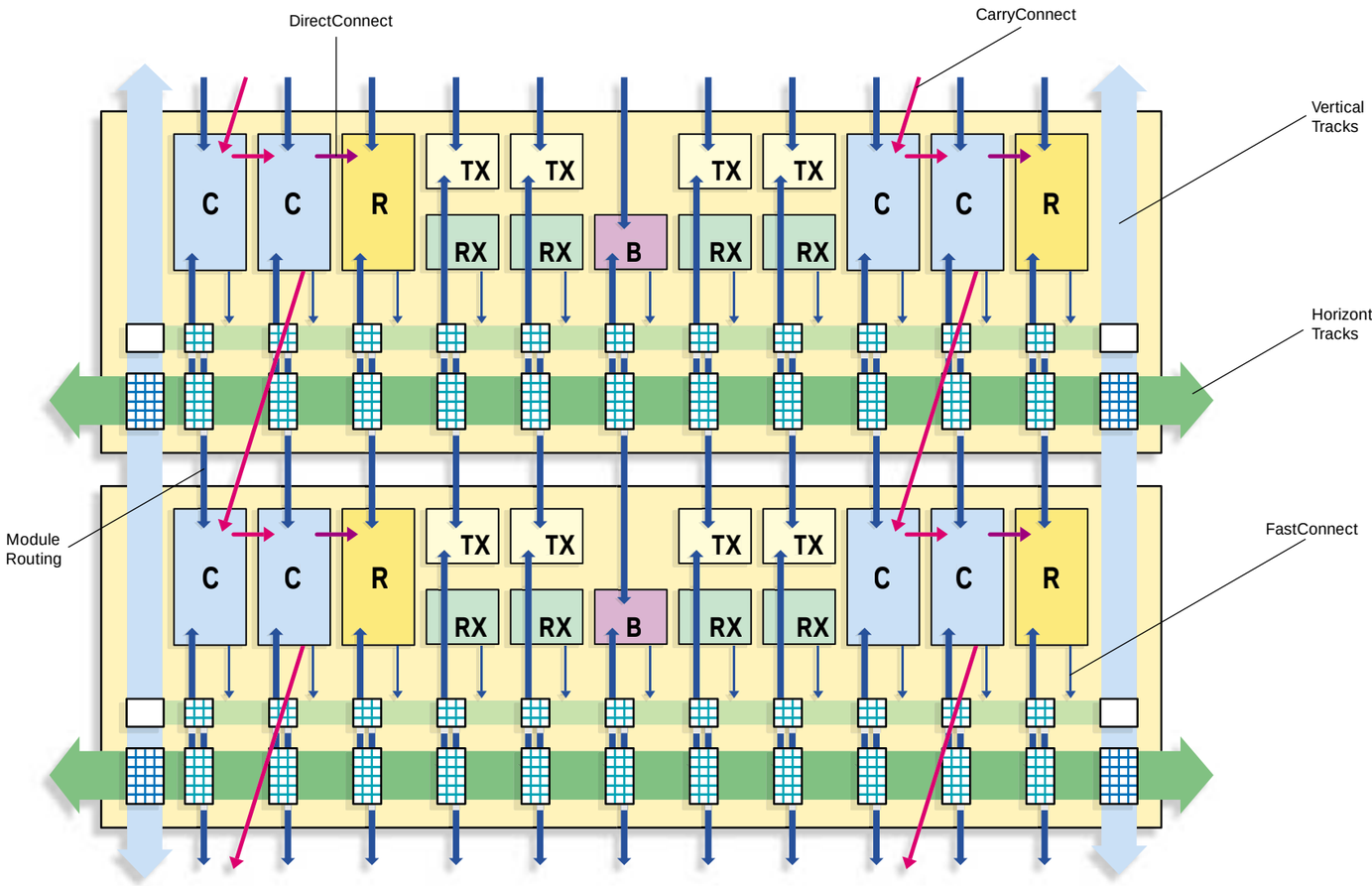
Architecture Comparison

New, Innovative Architecture

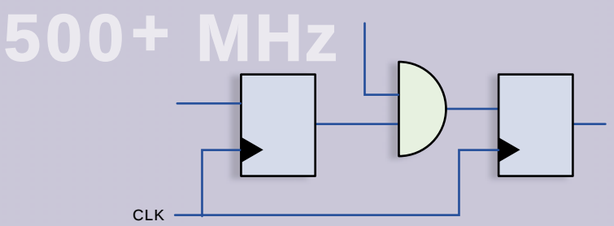
The Axcelerator is based on the AX architecture, which builds on the evolution of Actel's sea-of-modules architecture. Axcelerator FPGAs have two basic modules, the C-cell (Combinatorial cell) and the R-cell (Register cell), which efficiently implement combinatorial and register-based logic. When combined, the R-cell and C-cell create Clusters. Two Clusters are then combined to form SuperClusters, which are organized into Core Tiles to make up a sea-of-modules at the chip level. The entire floor of the Axcelerator device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing, unlike SRAM FPGAs.

Fast, Hierarchical Routing

Connecting the modules is a high-speed hierarchical routing structure. DirectConnects provide very high performance routing inside SuperClusters, while FastConnects provide high speed routing inside the SuperCluster and to the SuperCluster below. Additional CarryConnect routing connects C-cells in SuperClusters when building arithmetic functions. Core Tiles are also connected with vertical and horizontal routing resources. Finally, at the chip level, routing highways are used for efficient long-distance routing.



High-Speed Hierarchical Routing



Internal Performance — Register to Gate to Register

Performance

With 7 layers of metal on a .15µm process, the Axcelerator family was designed for speed and total logic utilization. Redesigned flexible logic modules, highway tracks for carrying signals across the chip, extensive carry chain support, and many other innovative attributes have been implemented in the AX architecture to guarantee a high performance solution. Axcelerator FPGAs achieve better than 500 MHz internal and 350 MHz system performance.

Density

With densities ranging from 125,000 to 2 million equivalent system gates, Axcelerator FPGAs are well-suited for large, complex designs. With its abundance of interconnection resources, Axcelerator's innovative routing architecture exploits antifuse technology to achieve nearly 100% utilization. With high densities, high utilization, and low power consumption, Axcelerator FPGAs are a strong alternative to ASICs.

Flexibility

In addition to high performance and high density, Axcelerator FPGAs have numerous other features. Axcelerator FPGAs feature innovative SRAM/FIFO and PerPin FIFOs, enabling data to easily cross clock and phase domains. In addition, Axcelerator FPGAs have an integrated low-power mode to accommodate power-conscious designs, disabling one or more I/O banks while allowing operation of the device's internal logic. With flexible I/Os compliant with multiple standards, embedded SRAM with programmable FIFO logic, segmentable clock resources, and embedded PLLs, Axcelerator FPGAs have all the resources necessary for the complex designs of today and tomorrow.

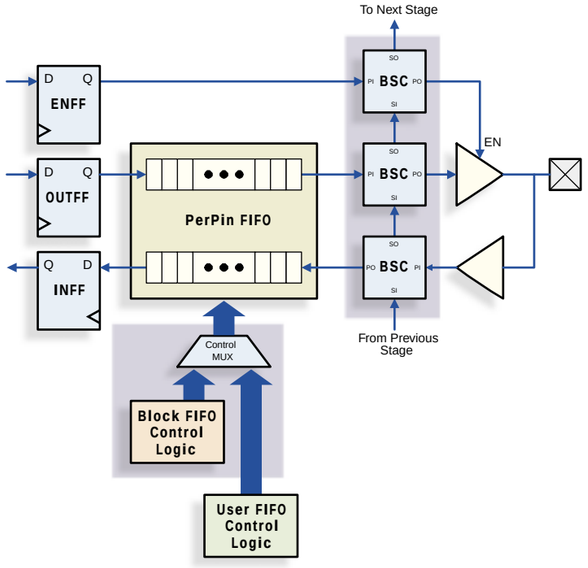
The Axcelerator Advantage

Using high performance FPGAs often means sacrificing other design goals. Not so with Axcelerator FPGAs! Because Axcelerator devices are antifuse-based, all of the inherent benefits of antifuse technology apply. Since Axcelerator FPGAs are nonvolatile, they are live at power up so there's no latency issue while loading configuration data. Axcelerator also does not require a boot PROM, eliminating the possibility of intercepting configuration data. With the advanced AX antifuse architecture, Axcelerator FPGAs have the best performance-to-power consumption ratio of any FPGA and provide a secure, "instant on" solution.

The High-Security Solution

FPGAs are quickly becoming the new alternative to ASICs. Many systems today have a significant portion of the total system-level IP inside the FPGA. Since a conventional SRAM-based FPGA is volatile, it must be re-initialized every time power is applied. This re-initialization requires an external bitstream be loaded into the FPGA. This external bitstream also allows easy, non-invasive, copying of the design.

Unlike SRAM-based FPGAs, Axcelerator does not require an external bitstream and provides significantly higher design security. The FuseLock™ secure programming technology used in the Axcelerator family is highly resistant to both invasive and non-invasive security attacks.



Flexible Multi-Standard I/Os

The Axcelerator family I/Os were designed with performance and flexibility in mind. The I/Os are bank-selectable with 3 registers per I/O. The I/Os are hot-swap compliant and support a range of mixed voltages and I/O standards (LVTTL, LVCMOS, 3.3V PCI, 3.3V PCI-X, LVPECL, LVDS, GTL+, HSTL Class 1, SSTL2 Class 1&2, and SSTL3 Class 1&2). In addition, each I/O features a 64-bit PerPin FIFO with a separate read and write clock.

PerPin FIFOs

The Axcelerator family provides the most flexible I/O structure of any FPGA. Each I/O features a 64-bit deep FIFO that can be independently controlled or combined for bus applications. The PerPin FIFO is unique to the AX architecture and can be used in conjunction with the 14 I/O standards offered by Axcelerator family devices. To further maximize flexibility, selectable, independent read and write clock polarities allow the transfer of data between different clock domains. Embedded I/O FIFO Controllers are provided so that 100% of the core logic resources are available to the user.

High Performance Embedded Memory

Axcelerator devices have up to 64 blocks of embedded, variable-aspect-ratio SRAM with separate read and write ports that can be configured with different bit widths on each port. Configurations include 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1. Each SRAM block has an embedded FIFO control unit that allows the block to be configured as a synchronous FIFO with programmable flag generation. Each block also contains counters to generate address pointers and control circuitry to prevent metastability and error conditions.

Flexible Clock Resources

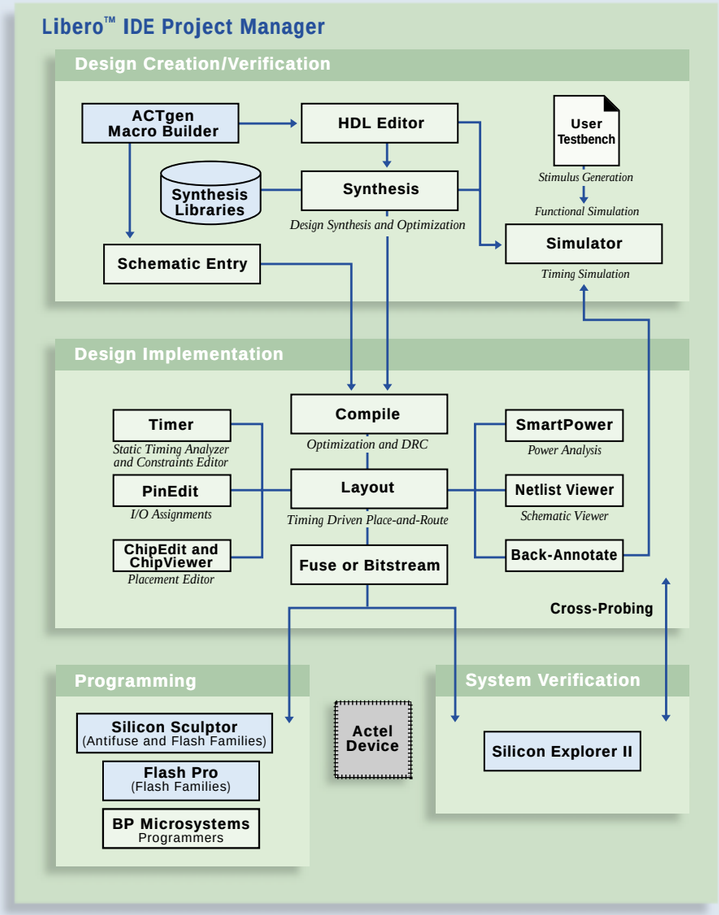
Axcelerator FPGAs have a number of clock resources available to the designer. Every device contains four hardwired and four routed clocks. In addition, every device has a global preset/clear signal available. Each hardwired and routed clock has an associated analog PLL. These 8 PLLs can operate with input frequencies from 14-200MHz and can generate output frequencies between 20 MHz and 1 GHz.

Design Tools

Design Environment

The Axcelerator family of FPGAs is fully supported by both the Actel Libero™ Integrated Design Environment and the Actel Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity,® ViewDraw for Actel from Mentor Graphics, Designer software from Actel, Model*Sim*™ HDL Simulator from Model Technology,™ and WaveFormer Lite™ from SynaptiCAD.™

Actel's Designer software provides a comprehensive suite of back-end development tools for FPGA development. The Designer software includes timing-driven place-and-route, a world-class integrated static timing analyzer and constraints editor, a design netlist schematic viewer, and SmartPower, a tool that allows the user to quickly estimate the power consumption in a design. With the Designer software, a user can lock their design pins before layout while minimally impacting the results of place-and-route. Additionally, our back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with our Silicon Explorer II in-system probes. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

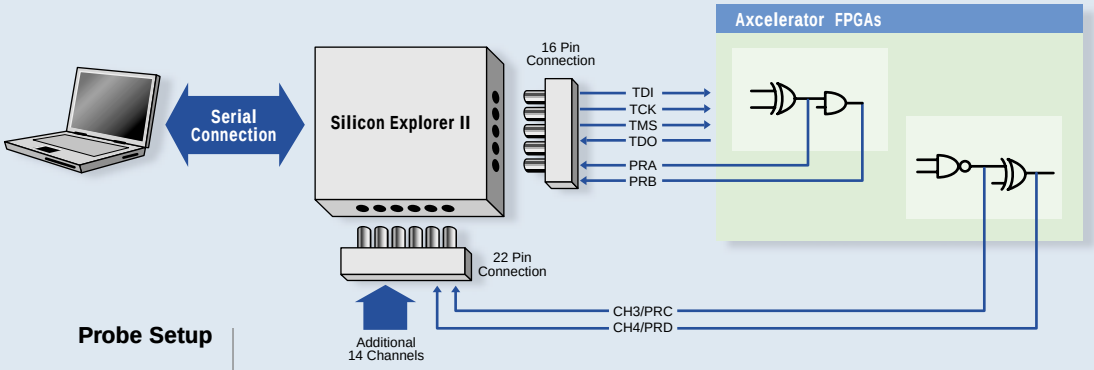


Programming

Programming support is provided through Actel's Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. Programming with Silicon Sculptor II is as easy as pushing a button. There is minimal interaction between the device programmer and the user, which reduces the chances of error. Factory programming is also available for high-volume production needs.

Verification

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allow designers to examine any of the internal nodes of a device operating in a prototype or a production system. Silicon Explorer's non-invasive method does not alter any timing or loading thus helping to shorten the debugging cycle.



Probe Setup

Axcelerator Product Offerings

	AX125	AX250	AX500	AX1000	AX2000
System Gates	125,000	250,000	500,000	1,000,000	2,000,000
Dedicated Registers	672	1,408	2,688	6,048	10,752
Max Registers	1,344	2,816	5,376	12,096	21,504
Embedded RAM bits	29,184	71,168	95,232	198,912	338,688
Embedded RAM Blocks (4,608 bits)	4	12	16	36	64
Max User I/Os	168	248	336	516	684
Max Number of LVDS Pairs	84	124	168	258	342
PLLs	8	8	8	8	8
Global Clocks	8	8	8	8	8
Packages	CS 180 FG 256 FG 324	FG 256 FG 484	FG 484 FG 676	BG 729 FG 484 FG 676 FG 896	FG 896 FG 1152

For more information regarding the Axcelerator family of FPGAs, call 1.888.99.ACTEL or visit our website at http://www.actel.com

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Actel Corporation
955 East Arques Avenue
Sunnyvale, CA USA 94086
Telephone 408.739.1010
Facsimile 408.739.1540

Actel Europe Ltd.
Maxfli Court, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Telephone +44 0 1276.401450
Facsimile +44 0 1276.401490

Actel Japan
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150, Japan
Telephone +81 0 3.3445.7671
Facsimile +81 0 3.3445.7668