Using the Axcelerator PerPin FIFOs

Introduction

In addition to more conventional I/O buffers and single registers, Actel's Axcelerator FPGA family offers an innovative PerPin FIFO structure. The user can use this 64-bit "FIFO-per-pin" to buffer input or output data. The FIFO can be bypassed entirely if desired. The PerPin FIFOs are organized into groups. A hardwired I/O FIFO Embedded Controller provides the following functions to control all I/Os in a group for bus-oriented applications. Maximum operating frequency for the controller is 350 MHz. The controller can also be implemented in FPGA gates – see the "Controller Utilization Statistics" section on page 8.

Architecture

The block diagram of the PerPin FIFO structure and associated control logic is shown in Figure 1. Note that the Boundary Scan Cells (BSCs) are located between the I/O buffers and any core logic – including the PerPin FIFOs. This is required by the 1149.1 JTAG specification. The PerPin FIFO is between the single input and output registers and the boundary-scan logic. The hard-wired I/O FIFO control logic can be used to control the PerPin FIFO. The User FIFO control logic – implemented as a "soft" controller – can either be generated by Actel's ACTgen tool or designed by the user.

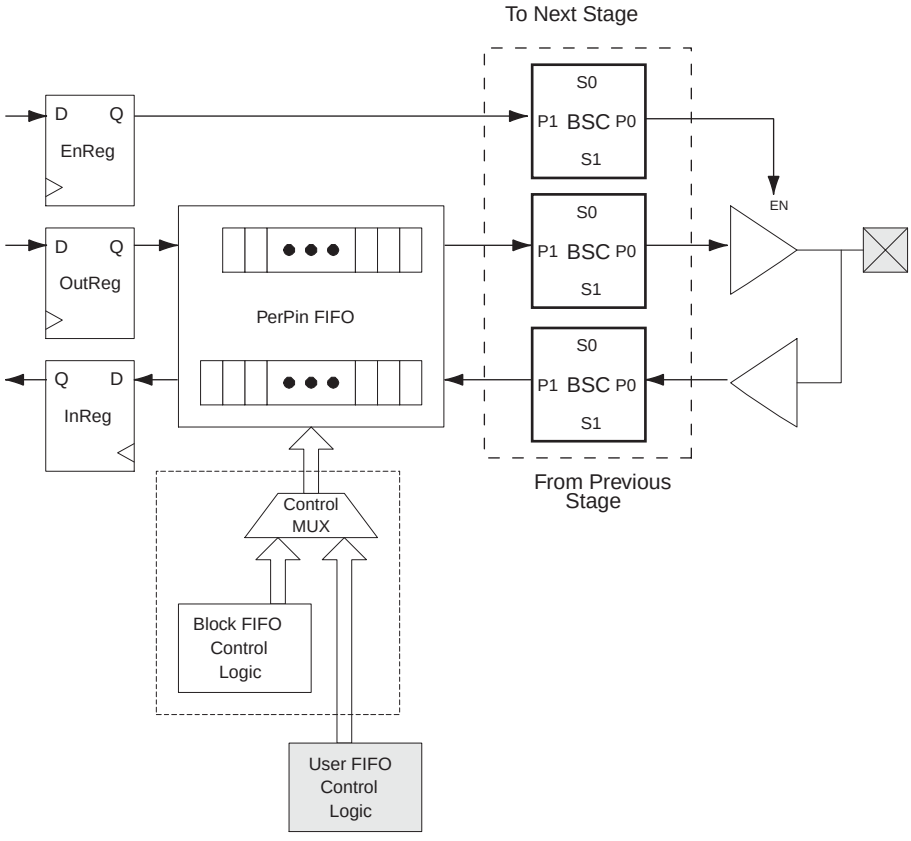

Figure 1 • PerPin FIFO Structure

Two sets of the logic shown in Figure 1 on page 1 (registers and PerPin FIFO) are grouped into an I/O cluster as shown in Figure 2. In turn, the clusters are grouped into blocks of up to 13 clusters (i.e., 26 I/Os); see Figure 3 (12 clusters shown).

The user has three PerPin FIFO choices for each I/O as follows:

- Bypass the PerPin FIFO
- Use the PerPin FIFO as part of a block
- Use the PerPin FIFO as a single-bit FIFO

If the second option is chosen, there are two hard-wired FIFO block controllers per tile edge. Each controller generates Full and Empty flags as well as programmable ALMOST FULL (AFULL) and ALMOST EMPTY (AEMPTY) flags. Writing when full and reading when empty are inhibited by block control signals. Wider FIFO blocks are possible by combining multiple blocks. Maximum operating frequency for the controller is 350 MHz.

Figure 4 illustrates a block diagram showing the PerPin FIFO control signals as well as those of a hard-wired controller.

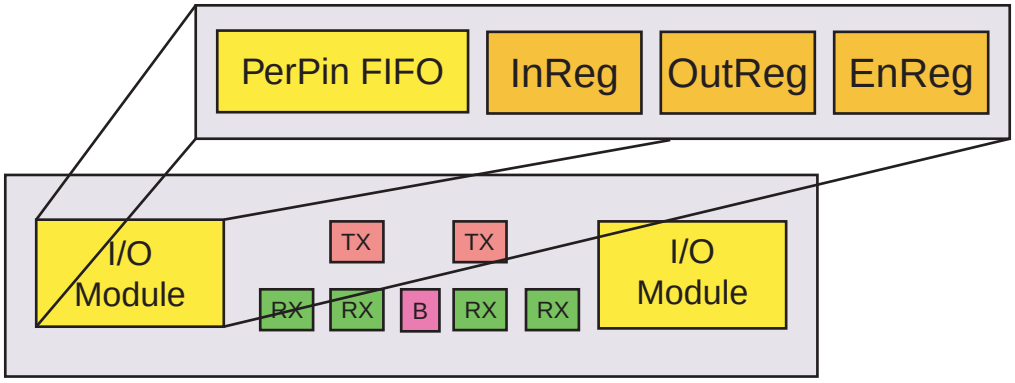

Figure 2 • I/O Cluster Structure

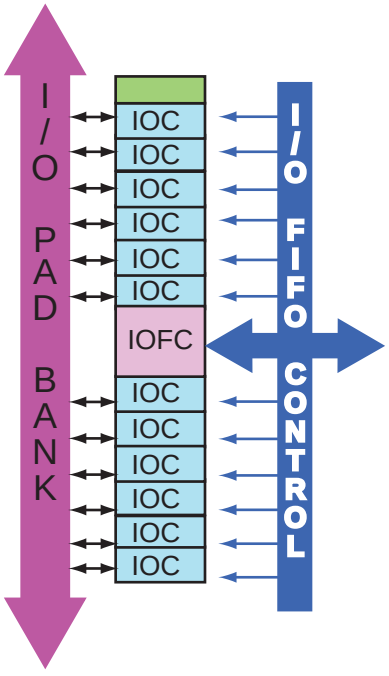

Figure 3 • I/O Cluster Block with Block FIFO Controller

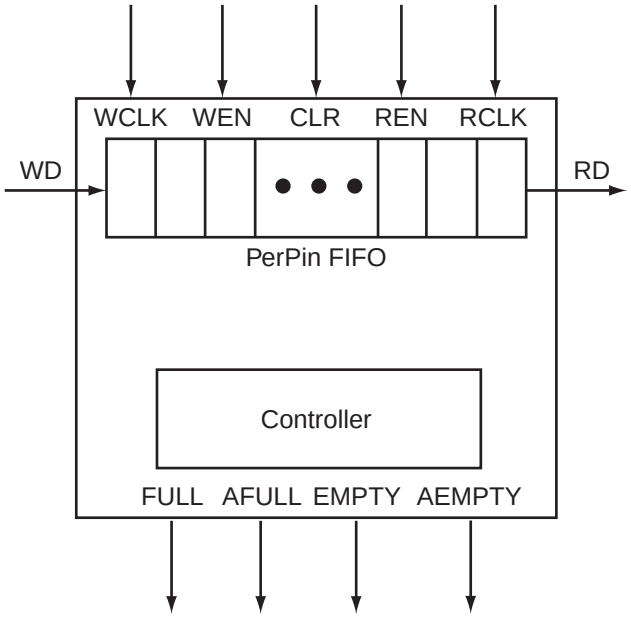

Figure 4 • PerPin FIFO Control Signals

A brief description of the pin usage is as follows:

- RCLK – Read clock input (rising-edge triggered).
- WCLK – Write clock input (rising-edge triggered).
- REN – read enable input (active low). Asserting REN at the rising edge of RCLK outputs data at the current read address and then increments the read address.
- WEN – write enable input (active low). Asserting WEN at the rising edge of WCLK writes data at the current write address and then increments the write address.
- CLR – Clear input (active low). Asserting this signal clears the output data and resets the read and write addresses to FIFO memory location 0.
- RD – Read data
- WD – Write data

In addition, the built-in hardwired controller generates four flags as described below. The "soft" controller generated with ACTgen (see the"Using the PerPin FIFO" section on page 4) generates identical flags. The user is also free to use FPGA gates to implement his own controller logic.

- EMPTY – This flag is asserted when the FIFO is empty. When asserted, reading is inhibited. EMPTY is synchronous with the read clock.
- FULL – This flag is asserted when the FIFO is full. When asserted, writing is inhibited. FULL is synchronous with the write clock.
- AEMPTY – Programmable (range 1 to 63 inclusive) Almost Empty flag. This flag is asserted when the level of the FIFO is at or below the programmed value.
- AFULL – Programmable (range 1 to 63 inclusive) Almost Full flag. This flag is asserted when the level of the FIFO is at or above the programmed value.

Timing Diagrams

Basic PerPin FIFO write and read timing diagrams are shown in Figure 5 and Figure 6 on page 4, respectively. Also shown in the diagrams are the timings of the flags if the hardwired I/O FIFO Embedded Controller is used.

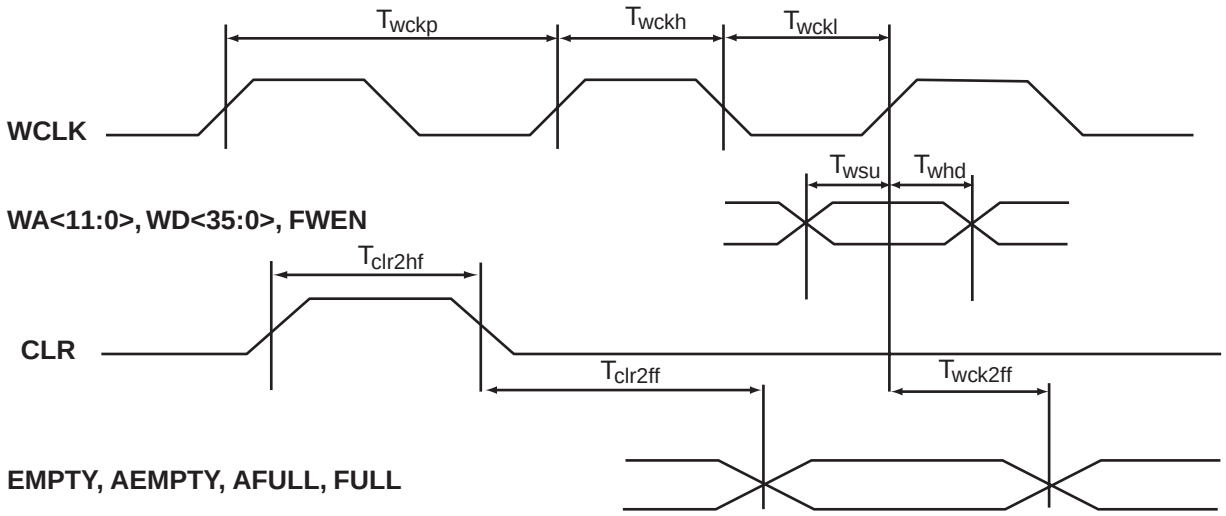

Figure 5 • *PerPin FIFO Write Timing*

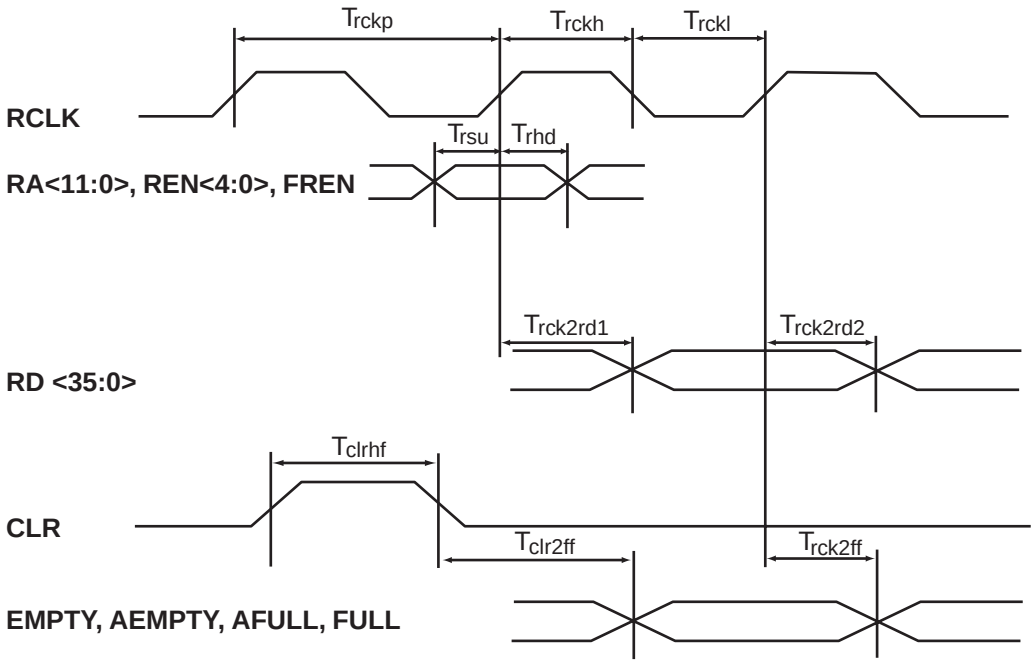

Figure 6 • *PerPin FIFO Read Timing*

Using the PerPin FIFO

The PerPin FIFO capability is accessed through ACTgen in Designer as outlined below.

- Invoke ACTgen.
- Select File -> New to select the AX Family as shown in Figure 7. Click OK.
- Click on the I/O Icon under the Macro window (Figure 8 on page 5).
- At this point the user can select either the Input PerPin FIFO or the Output PerPin FIFO. See the separate sections below for details.

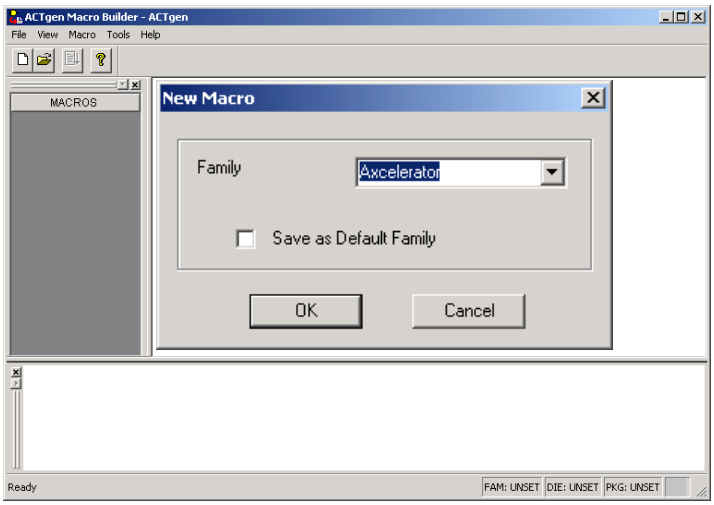

Figure 7 • *Invoking ACTgen and Choosing the Axcelerator Family*

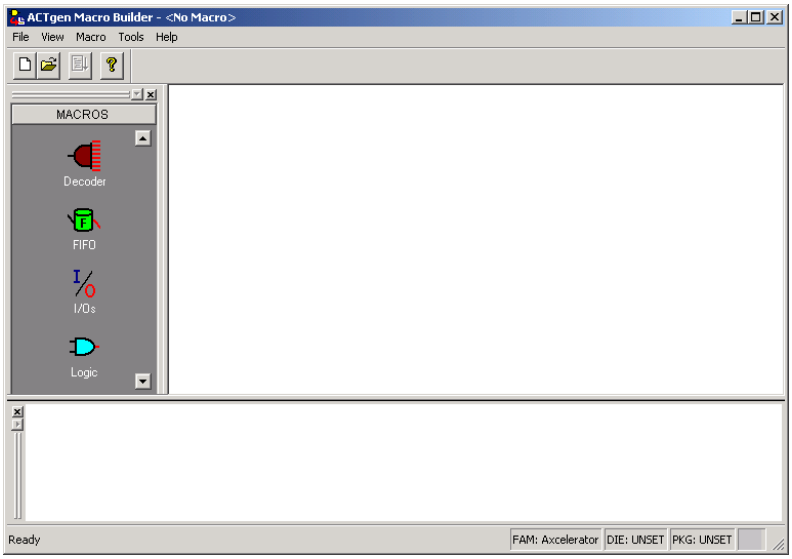

Figure 8 • Selecting the I/O Macro

Input PerPin FIFO

The Input PerPin FIFO is configured using the following options:

- Select the Input IOFIFO tab (see Figure 9).
- Choose one of the Variations (see below).
- Choose Width – 1 (default) to 499.
- Edit the Port Mapping list if other than default names are desired (Figure 10 on page 6).
- If the Controller box is checked (Figure 11 on page 6).
  - Select the Embedded or Soft version.
  - Choose AEMPTY (AEVAL) and AFULL (AFVAL) thresholds between 1 (default) and 63.
- Select Generate. You will be prompted for a file name, and the file format can be selected as EDIF, VHDL, VERILOG, or WV..

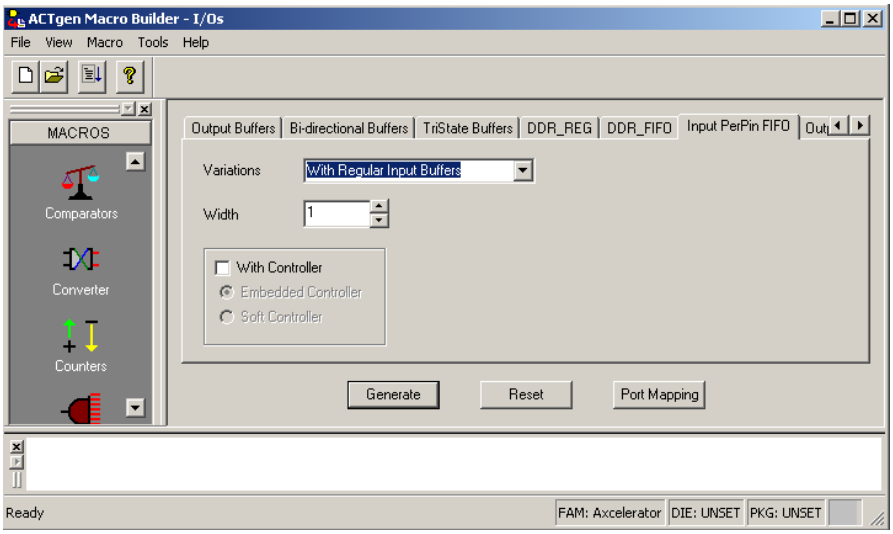

Figure 9 • Choosing Input PerPin FIFO (With Regular Input Buffer and Without Controller)

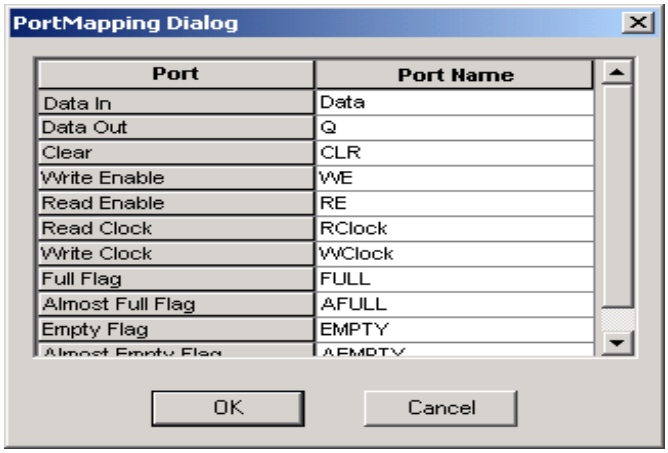

Figure 10 • *Input PerPin FIFO Poert Mapping*

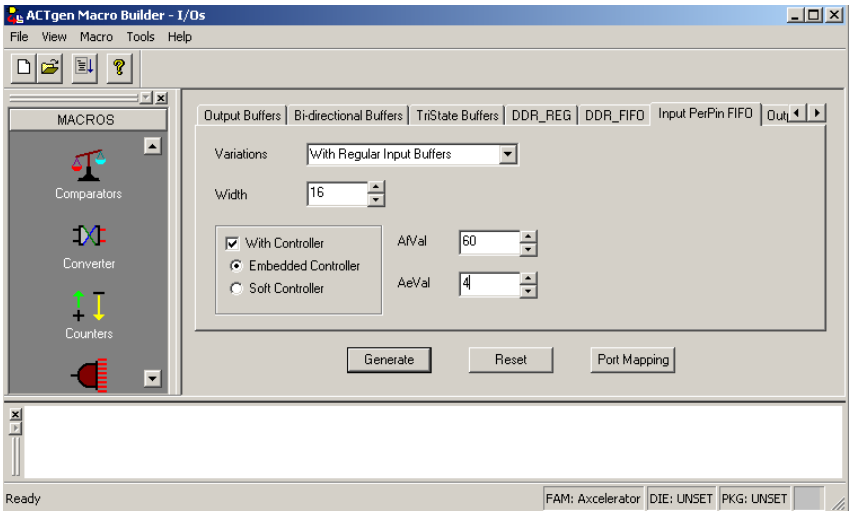

Figure 11 • *Selecting Input PerPin FIFO Controller Option*

Note that the Variation illustrated is With Regular Input Buffers. Other options include:

- With Special Input Buffers – Type choices are LVCMOS25 (2.5v LVCMOS) (default), LVCMOS18 (1.8v LVCMOS), LVCMOS15 (1.5v LVCMOS), PCI, PCIX, GTLP25 (GTL+ 2.5v), GTLP33 (GTL+ 3.3v), HSTL_I, HSTL_II, SSTL3_I, SSTL3_II, SSTL2_I, SSTL2_II.
- With Pull-Up Input Buffers – Type choices are LVCMOS25 (default), LVCMOS18, LVCMOS15.
- With Pull-Down Input Buffers – Type choices are LVCMOS25 (default), LVCMOS18, LVCMOS15.
- With LVDS/LVPECL Input Buffers – Type choices are LVDS (default) and LVPECL.

Output PerPin FIFO

Configuring the Output PerPin FIFO is very similar to the Input PerPin FIFO:

- Select the Output IOFIFO tab (Figure 11).
- Choose one of the Variations – Regular or Special.
- Choose Width – 1 (default) to 499.
- Edit the Port Mapping list if other than default names are desired.
- If the Controller box is checked.
  - Select the Embedded or Soft version.
  - Choose AEMPTY (AEVAL) and AFULL (AFVAL) thresholds between 1 (default) and 63.

- If the With Special Output Buffer Variation is selected (Figure 12):
  - Select Output Drive – 1x, 2x, 3x, 4x (default).
  - Select Slew Rate – Low or High (default).
  - Select Generate. You will be prompted for a file name, and the file format can be selected as EDIF, VHDL, VERILOG, ADL, or WV.

Note that the Variation illustrated is With Special Output Buffers. Other options include:

- With Regular Output Buffers .
- With LVDS/LVPECL Output Buffers – Type choices are LVDS and LVPECL .

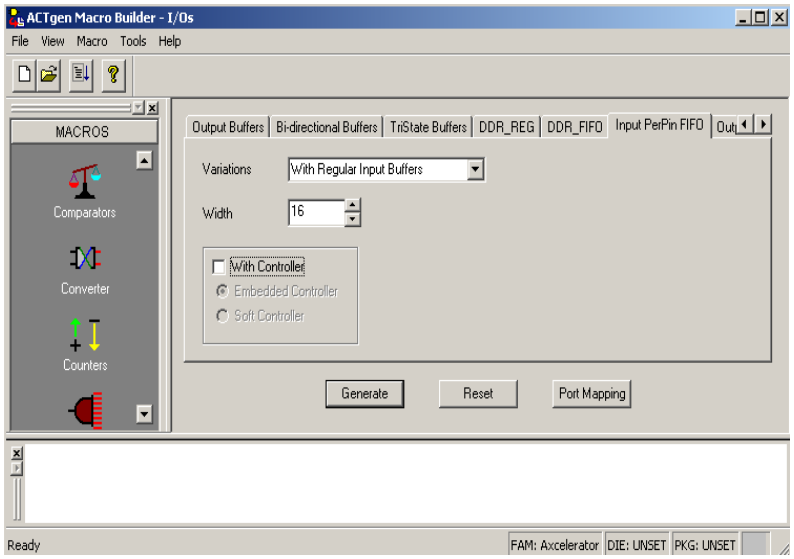

Figure 12 • *Choosing Output PerPin FIFO (With Special Input Buffer and Without Controller)*

Typical PerPin FIFO Application

Figure 13 illustrates the typical usage of the PerPin FIFO. The figure shows the built-in I/O FIFO hard controller associated with one group of PerPin FIFOs as well as a soft controller associated with another group. As mentioned in the text, both controllers use the same control signals.

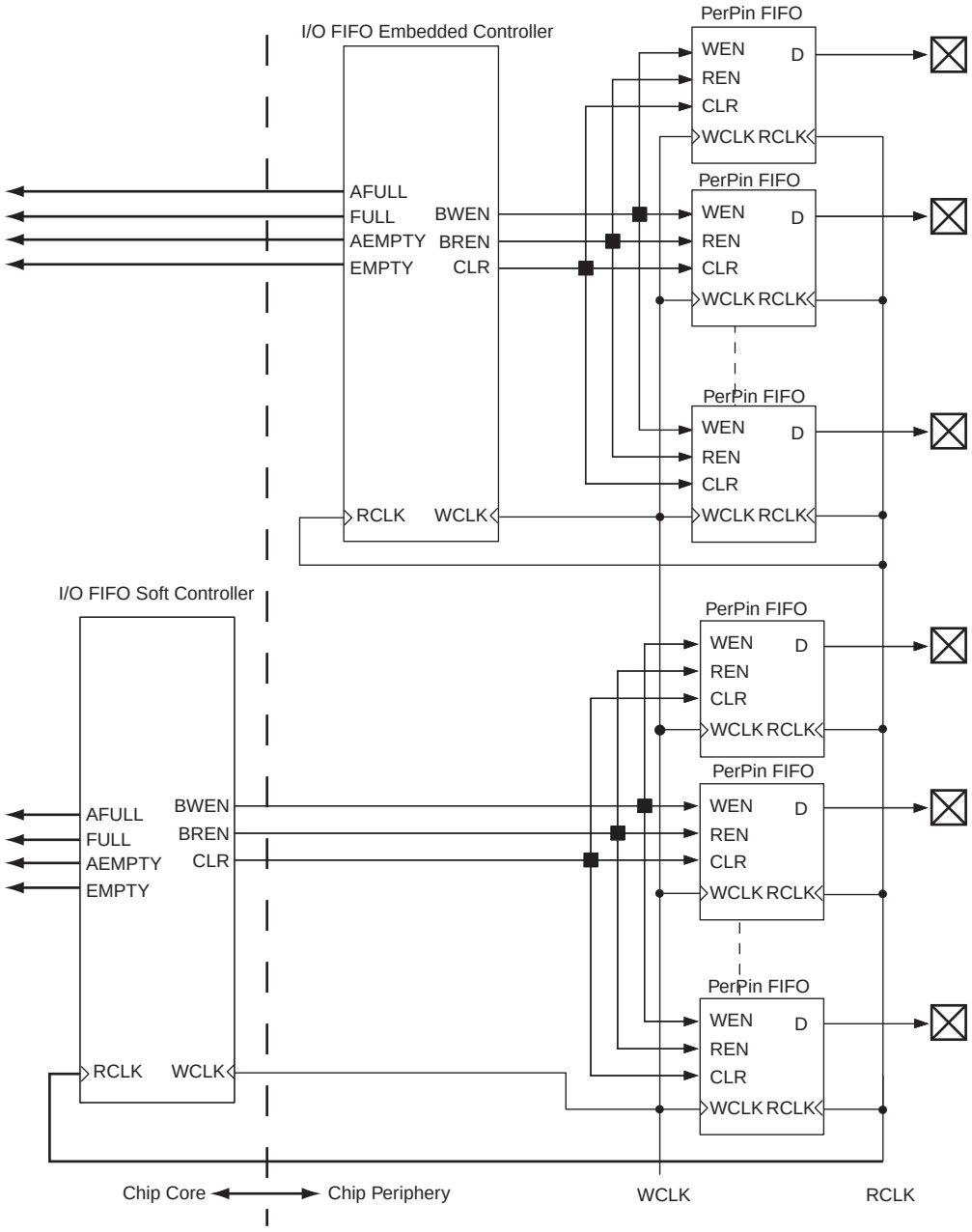

Figure 13 • *PerPin FIFO Usage*

Controller Utilization Statistics

The following is a summary of utilization when ACTgen is used to generate a soft controller:

- 112 Combinatorial cells (8% of an AX 125)
- 46 Sequential cells (7%)
- 158 Total cells (8%)

Conclusion

The innovative Axcelerator PerPin FIFO structure allows extremely flexible data buffering without wasting core logic. In addition, the option of using a hardwired FIFO controller for groups of I/Os results in further logic savings. Operation up to 350 MHz adds very high performance to the mix!

Appendix A

PerPin FIFO and Timing Parameters

Parameter	Description	Mode	Typical (ns)	WC (ns)	Timer (ns)
t_{WSU}	Write Setup	1-bit FIFO	0.57	0.67	0.77
t_{WHD}	Write Hold	1-bit FIFO	0.01	0.01	0.05
t_{WCKH}	WCLK High	1-bit FIFO	0.74	0.97	1.12
t_{WCKL}	WCLK Low	1-bit FIFO	0.78	1.01	1.16
t_{RSU}	Read Setup	1-bit FIFO	0.64	0.78	0.85
t_{RHD}	Read Hold	1-bit FIFO	-0.31	-0.41	-0.50
t_{RCKH}	RCLK High	1-bit FIFO	0.86	1.15	1.27
t_{RCKL}	RCLK Low	1-bit FIFO	1.10	1.40	1.61
t_{RD}	Read Time	1-bit FIFO	1.38	1.83	2.13
t_{RST}	Reset Low	1-bit FIFO	0.43	0.53	0.59
t_{WSUB}	Write Setup	IO Block FIFO	0.81	1.00	1.10
t_{WHDB}	Write Hold	IO Block FIFO	-0.56	-0.74	-0.84
t_{RSUB}	Read Setup	IO Block FIFO	0.81	1.00	1.10
t_{RHDB}	Read Hold	IO Block FIFO	-0.56	-0.74	-0.84
t_{XCKP}	Clock Period	IO Block FIFO	0.85	1.07	1.29
t_{RST2FB}	Reset-to-flat EMPTY/FULL	IO Block FIFO	1.00	1.24	2.32
t_{RST2FB}	Reset-to-flag AEMPTY/AFULL	IO Block FIFO	3.18	4.08	4.36
t_{XCK2FB}	Clock-to-flag EMPTY/FULL	IO Block FIFO	1.02	1.29	1.54
t_{XCK2FB}	Clock-to-flag AEMPTY/AFULL	IO Block FIFO	3.28	4.36	5.04

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