Using Axcelerator PerPin FIFOs for Bus I/Os

Actel's Axcelerator device family provides PerPin FIFOs in each I/O cluster. PerPin FIFOs can be used for both input and output data, and greatly simplify interfacing with off-chip resources on different clock domains.

If designers utilize PerPin FIFOs in their design, they can elect to use the hard-wired embedded FIFO controller or create their own soft controller using internal logic. The soft controller handles bus widths up to 99. Up to 26 adjacent PerPin FIFOs in a single I/O block can share a hard-wired FIFO controller, which controls the FULL, EMPTY, AFULL (ALMOST-FULL), and AEMPTY (ALMOST-EMPTY) flags for all 26 FIFOs. However, if the input or output array is wider than 26 bits or the bus is spread over multiple I/O blocks, then more than one hard-wired I/O FIFO Embedded Controller is required. In future releases, ACTgen will automatically combine multiple hard-wired controllers. Meanwhile, if more than one controller is used, each controller will generate its own flags. As a result, the user must implement control logic to combine the flags generated by the different hard-wired controllers into a single set.

For example, assume that the user requires data rate conversion for a 32-bit input bus. The 32 separate PerPin FIFOs require at least two hard-wired controllers (the number of controllers could be higher depending on the location of each net of the bus). Active-high global flags to control the array of PerPin FIFOs are obtained by ORing the corresponding flags generated by each individual I/O FIFO Embedded Controller. For example, all the FULL flags of the individual FIFO controllers should be ORed to generate the FULL flag of the total array. The AFULL, EMPTY, and AEMPTY flags for the total array are similarly generated.

Figure 1 shows an example of connecting two I/O FIFO Embedded Controllers using OR gates.

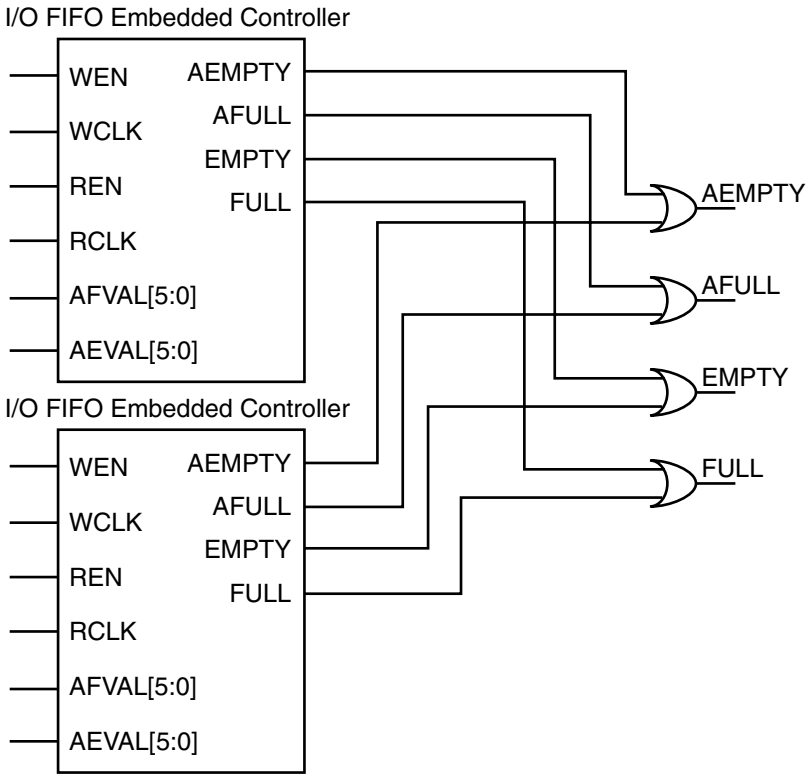

Figure 1 • *Connecting Two I/O FIFO Embedded Controllers*

The user should take the generated flag outputs as the control signals for read and write operations. For example, assume that one of the PerPin FIFOs becomes full, the corresponding hard-wired I/O FIFO Embedded Controller will assert its FULL flag and stop writing into the FIFOs associated with only THAT controller. To retain the synchronization of the data interface, Writes for ALL bits, including those controlled by other controllers, should stop once the global FULL flag is asserted.

In some cases, due to combinatorial logic delays, there is a short period of time between the assertion of the flags in a single hard-wired controller and the assertion of the global flags. This short time delay should be taken into consideration if the read and write operations are performed with very high frequencies.

There may be some synchronization issues in the design if there is large skew between the clocks (WCLK or RCLK) of the I/O FIFO Embedded Controllers. For example, assume that in Figure 1 on page 1 the WCLK signal arrives at the top controller sooner than the bottom one and that the resulting clock skew is larger than the propagation delay from the FULL flag of the top controller to the global FULL flag. In this case, the global FULL flag will be asserted before the bottom controller's last write. As a result, the PerPin FIFOs controlled by the bottom controller may not yet be full. The same scenario may happen during the read process if the clock skew is too large and the clock frequency is high.

The designer should take care when there is noticeable skew between the clock inputs of multiple controllers associated with a single bus. The skew is noticeable when the bus width is too large, or the bus bits are spread across the device. In this case, ONLY if the clock signal is routed through regular nets AND the fanout of the net is high ($\geq$12), the user needs to pay attention to the timing issues.

For example in an AX500, the nominal routing delay for a regular routing net with fanout of 32 across the device is 3.24ns (–3 speed grade). If the WCLK of the PerPin FIFOs is routed through this regular net with a fanout of 32 then for proper write behavior of the I/OFIFO Embedded Controllers, the delay between the assertion of the earliest FULL flag until the assertion of the global flag, must be more than 3.24ns. Otherwise, the global flag will be in logic high while some of the FIFOs are not yet full.

As a rule of thumb, if the write or read clock signals are routed through regular nets with relatively high fanout numbers, the user should look into the timing behavior in greater detail if the clock frequency is higher than 150 MHz.

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