Using the BUFD and INVD Delay Macros

Chip designers often find themselves in a situation where the board layout has been completed before the chip is designed. The FPGA they are targeting must satisfy an external input phase relationship - usually between clock and data inputs. Maintaining this phase relationship for signals going off-chip enables them to meet external setup and hold requirements. BUFD and INVD are special delay macros that give designers more control in the timing behavior of their designs.

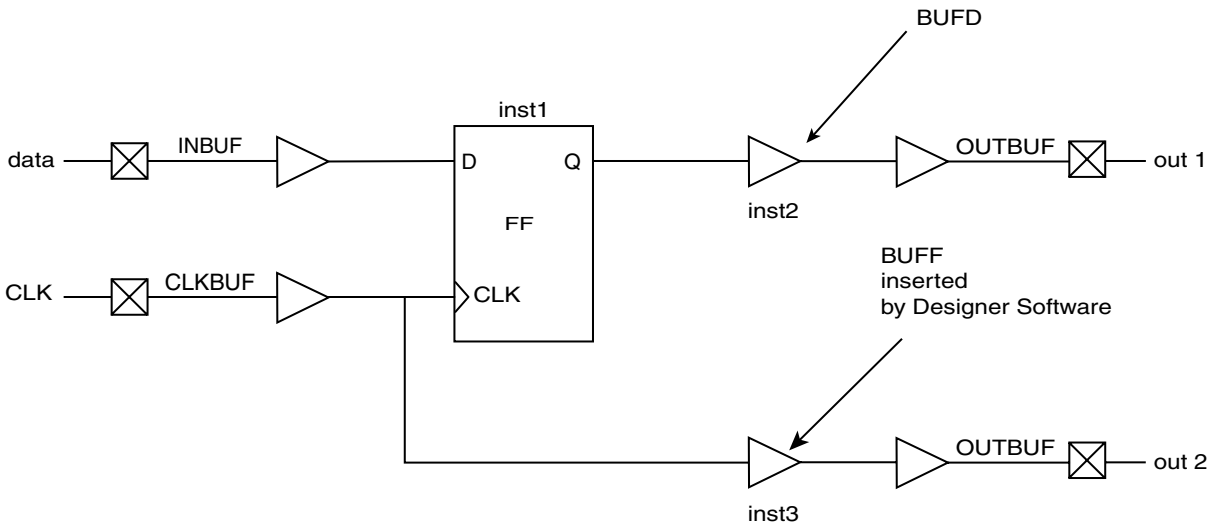
BUFD is a special version of the buffer (BUFF), which will not be removed by Actel's Designer software in its optimization steps. This macro will always be retained and its delay preserved after the compile and layout steps. Similarly, INVD is a special version of the inverter (INV), which is preserved after compilation and layout.

The suggested uses of BUFD and INVD are as follows:

- Maintain the phase relationship between clock and data input signals when sending signals derived from them these signals off-chip. This application enables them to meet external setup and hold requirements.
- Maintain the phase relationship of clock and data input signals in designs with high-fanout clock signals.

Maintaining Phase Relationships

As shown in Figure 1, a certain phase relationship exists between the clock and data signals (generally, the data signal lags the clock signal). Employing BUFD is recommended to maintain this phase relationship. All Actel antifuse device families have a restriction that a CLKBUF cannot be connected directly to an OUTBUF, so Designer software will automatically insert a BUFF module (inst3 in Figure 1). This will introduce a delay that may cause the data signal to arrive ahead of the sys_clk signal going off-chip. To prevent this, the user can insert a BUFD macro in his netlist. The BUFD, unlike a regular BUFF, is assigned the ALSPRESERVE property. This ensures that the BUFD will not be optimized away during the compilation step and hence can offset the delay caused by automatic insertion of the BUFF in the sys_clk path. This technique maintains the phase relationship of the data and clock inputs when going off-chip and the external setup and hold requirements can be met.

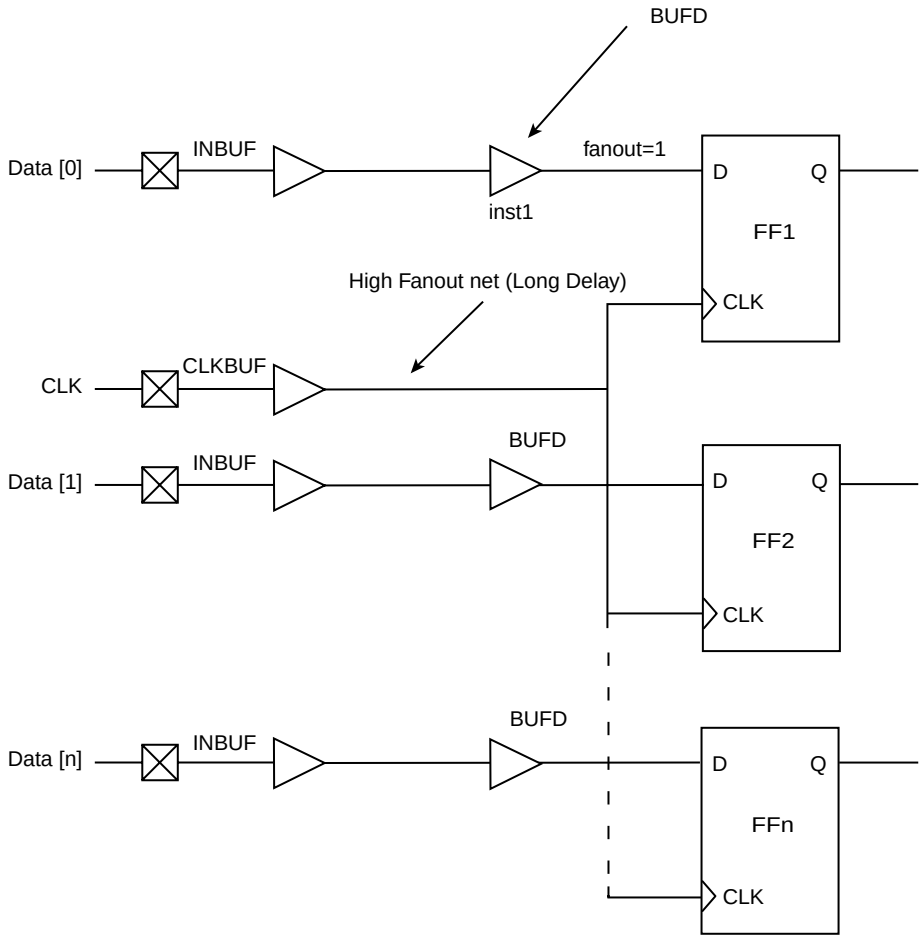


Note: *BUFD is inserted by the user.*

Figure 1 • *Control of Phase Relationship between Data and System Clock using BUFD*

In Figure 2, the clock signal coming from the CLKBUF has a high fanout. This means increased capacitive loading and hence increased delay. In contrast, the data signal has a fanout of only one. The clock network's high fanout may allow the data input to (undesirably) lead the clock signal. Again, introducing one or more BUFD macro (inst1) in the data signal path provides enough delay to offset the delay of the high-fanout clock net.

If inversion of the signal is required in addition to delay, the INVD macro is available. Again, the ALSPRESERVE property is assigned to this macro to avoid elimination during optimization steps.



Note: *BUFD is inserted by the user.*

Figure 2 • *Control of Phase Relationship in Designs with High Clock Fanouts*

Usage Models

HDL Design Flow

None of the synthesis tools that support Actel technologies will infer the INVD or BUFD macros in the synthesized netlist. Simulation library models of INVD and BUFD, similar to their INV and BUFF counterparts, are available from Actel in both VHDL and Verilog. The manual process for buffer insertion is as follows:

1. Import the synthesized netlist into Designer. Run compile and layout.
2. Invoke Timer from Designer to check the timing/phase relationships for the signals of interest.
3. Using a text editor, manually modify the netlist and insert BUFD and/or INVD macros into the desired paths.
4. Import the modified netlist into Designer. Again run compile and layout. Use incremental layout option to preserve previous placement.
5. Invoke Timer again to review the delays for the signals of step 2.

If necessary, repeat steps 3 through 5 until the design timing requirements are met.

Schematic Capture Design Flow

INVDs and BUFDs are available for the following Actel-supported schematic capture tools:

- ConceptHDL PE13.5 and PE13.6
- Mentor Graphics c.4 and D.1
- Workview Office 7.5
- Powerview 6.1
- ePD 1.0
- ePD 1.1 Typical

To avoid inadvertent instantiation of INVD or BUFD where INV or BUFF is intended, the graphical symbols for INVD and BUFD have warning labels "Special Use Only."

The flow for buffer insertion is as follows:

1. Generate an EDIF netlist with the schematic tool.
2. Import the EDIF netlist into Designer. Run compile and layout.
3. Invoke Timer from Designer to check the timing/phase relationships for the signals of interest.
4. Edit the schematics to insert BUFD and/or INVD macros into the desired paths.
5. Check and save your schematics. Generate an EDIF netlist from the modified schematics.
6. Import the modified netlist into Designer. Again run compile and layout. Use incremental layout option to preserve previous placement.
7. Invoke Timer again to review the delays for the signals of step 3.
8. If necessary, repeat steps 4 through 7 until the design timing requirements are met.

Delay Values

Table 1 shows the rising (R) and falling (F) delays for INVD and BUFD in different Actel families. These values are obtained using the fastest speed grade for the device using typical temperature, voltage, and process corners as well as optimized placement. Actual delay numbers may vary with the device, speed grade, and actual placement.

Table 1 • *BUFD/INVD Delay for Various Actel Technology Families*

		ACT1	ACT2	ACT3	3200DX	42MX	SX	eX	Units
BUFD	R	3.9	4.3	2.6	4.2	1.8	0.7	1.1	ns
	F	3.7	3.5	2.5	3.4	1.6	0.7	1.1	ns
INVD	R	3.8	4.3	2.4	3.9	1.8	0.7	1.1	ns
	F	3.6	3.6	2.2	3.2	1.6	0.7	1.1	ns
Speed Grade		-3	-1	-3	-3	-3	-3	STD	ns

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