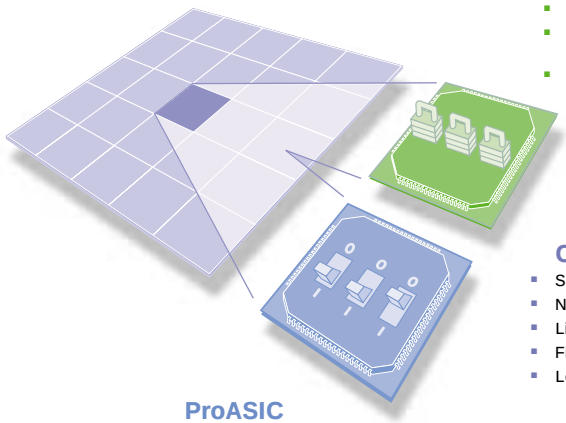
Actel's Flash to ASIC Conversion Program

The Cost Effective Solution for High Volume Applications

Actel offers a risk free conversion path for high volume designs using ProASIC™ or ProASIC PLUS FPGAs by remapping the functionality of the ProASIC Flash FPGA family into a cost-effective standard cell ASIC. These pin-for-pin replacements are designed from the existing FPGA database, which means a reduced risk for the customer.

From Flash to ASIC



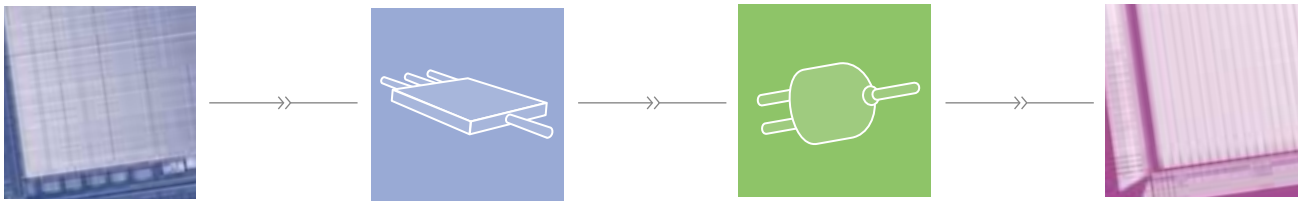
ASIC
- Fixed Design
- High-Volume Production Solution
- Long Development Cycle

Common Features
- Single Chip
- Nonvolatile
- Live at Power Up
- Fine Grained Architecture
- Low Power

ProASIC
- Reprogrammable Design
- Low-Volume Production Solution
- Quick Development Cycle

Key Features

- Support for all ProASIC and ProASIC PLUS family members
- Proven Cost Reduction Migration Path for High Volume Designs
- ProASIC's Fine Grained Architecture Simplifies Conversion and Reduces Risk
- Fully Pin / Feature / Voltage Compatible with ProASIC / ProASIC PLUS
- Support for All ProASIC / ProASIC PLUS Packages
- Fast Turn Around Times



ProASIC Architecture Simplifies Conversion

ProASIC: Fine-Grained Architecture for Easy Conversion

Based on a standard Flash/CMOS process, the ProASIC and ProASIC^{PLUS} families combine high density and low power with nonvolatility and reprogrammability. With a unique fined-grained architecture offering predictable performance, improved utilization, and greater routing efficiency, ProASIC devices allow designers to easily meet performance goals. These same product features allow an easy conversion to a standard cell ASIC. ProASIC's fine-grained (three input, one output) architecture is the closest in the industry to that of an ASIC (two input, one output), making design conversion quick and easy. A designer can quickly develop and debug a prototype system using ProASIC and then, after production ramps to high volume, easily convert to a more cost-effective standard cell ASIC solution.

Like an ASIC, ProASIC requires no PROMs or other external components. There are no power up differences between ProASIC and an ASIC — both are nonvolatile and live at power up. Total development expenses will be minimized while taking advantage of time to production savings because a conversion yields a simple one-to-one FPGA replacement with a fully footprint-compatible ASIC without any changes to the printed circuit board.

Synthesis tools, designed for optimal performance with fine-grained architectures, are well suited for use with Actel's ProASIC devices. The fine-grained nature of ProASIC's architecture yields designs that utilize logic resources efficiently with minimal timing issues, as opposed to the coarse-grained architectures of some FPGAs, which lead to difficulty in prediction of utilization and performance. This architectural similarity between ProASIC and ASICs speeds the conversion process and significantly minimizes risks.

Advantages of Flash to ASIC Conversion

Cost Effective High Volume Applications

If your annual quantity of a programmable device requires very high volumes, it could make sense to consider a conversion. At low to moderate volumes, FPGAs are a better alternative to ASICs because they do not have the NRE charges that make ASICs an expensive solution. But at high volumes, the non-recurring engineering expenses associated with a conversion are easily amortized into the reduced overall unit cost, resulting in desirable annual cost savings.

Time to Market

Today, everyone is competing to get their product to market faster than the competition. For fast time to market, nothing beats an FPGA for flexibility and rapid prototyping. Once the design is finalized and production ramps up, a conversion gives the designer the best of both worlds: short design cycles and low production costs.

Low Power

If total system power consumption is an important issue, a conversion has possible advantages. With the inherent efficiency of the routing structure and the architecture of the logic cell, the ProASIC and ProASIC^{PLUS} families already feature low standby and low operating current but a conversion to ASIC could lower power consumption even further.

System Integration

Since ASICs have much higher gate counts than FPGAs, the functionality of several FPGAs can easily be integrated into a single ASIC. By consolidating multiple FPGAs and other support chips into a single conversion, you will reduce component count, thus saving board space and improving system reliability.

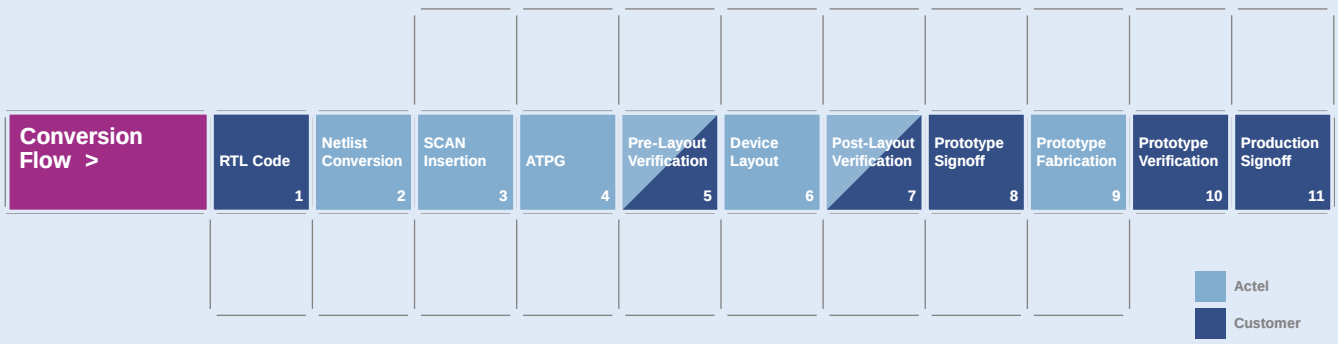
Customer Participation Requirements

To Be Supplied by Customer:

- **Netlist**
- **Pin Assignments**
- **Functional Test Vectors**
- **Timing Constraints**

Design Services Covered by NRE:

- **Netlist Conversion** (optional)
- **Re-synthesis Into Standard Cell Technology**
- **Scan Insertion** (optional)
- **ATPG** (optional)
- **BIST** (optional)
- **JTAG Interface** (optional)
- **Develop Test Fixturing**
- **Develop Test Program**
- **Mask Fabrication**
- **Prototype Fabrication**



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ProASIC Product Offering

ProASIC 500K Family Selector Guide	A500K050	A500K130	A500K180	A500K270
System Gates	100,000	290,000	370,000	475,000
ASIC Gates	25,000	75,000	100,000	125,000
Logic Tiles	5,376	12,800	18,432	26,880
Embedded RAM Bits	14k	45k	54k	63k
User I/Os	204	306	362	440

ProASIC PLUS APA Family Selection Guide	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
ASIC Gates	20,000	40,000	80,000	100,000	150,000	200,000	300,000
Logic Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits	27k	36k	72k	108k	126k	144k	198k
User I/Os	158	242	290	344	454	562	712

For more information regarding Flash to ASIC Conversion Services please contact your local Actel sales representative.

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