Global Clock Networks in Actel Antifuse Devices

System performance is one of the most important characteristics of a design. As a result, designers put a lot of effort to improve clock speed. Clock skew is often a limiting factor in attaining maximum performance, forcing designers to slow down their designs to avoid set-up and hold time violations. High fanout is also a parameter that can limit the timing performance of designs. Regardless of the efficiency of coding style, the clock skew and signal fanout put a physical limitation on the speed of the design. The Actel architecture provides global clock networks that allow high fanout drive for registers with little or no delay penalty and minimal skew. These networks enable the entire device to be spanned with fast, low skew routing resources.

The low skew clock networks can also be driven by internally generated signals or non-clock high fanout signals through regular I/O pins. Combining this flexibility with the efficiency of the low-skew networks allows designers to achieve very high speeds without being forced to compromise their original designs.

Clock Network Resources

Actel's antifuse device families provide different global clock network resources; each provides certain advantages for the user in improving his/her design. Knowing these advantages and considering the design requirements will help the designer to select the most efficient device family in terms of clocking speed.

Dedicated Clock Network

The dedicated clock (HCLK) network is directly wired from the HCLK input pin to the clock inputs of sequential cells. There are no programming elements in the path from the I/O pad driver to the inputs of S-modules. This provides a fast propagation route for input clock signals, enabling very fast clock-to-out performance and negligible clock skew (e.g. less than 0.1ns for the SX-A device family). The HCLK network offers guaranteed low clock skew and clock propagation delay independent of the number of S-modules being driven. This enables excellent design performance and accurate pre-layout timing analysis.

Only one hard-wired dedicated clock network exists on current antifuse parts.

Routed Clock Networks

Routed clock networks, specified by the names CLK, CLKA, CLKB, and Quadrant Clock (QCLK), are global clock networks which can be used both externally and internally (except for the CLK network in ACT1 family devices). The routed clock resources drive both sequential and combinatorial cells. Therefore, they can be used, if desired, as a fast track for non-clock signals, especially those with high fanout. The routed clocks are more flexible but not as fast as the hard-wired clock networks.

QCLKs, similar to CLKA and CLKB, can be sourced from external pins or from internal logic signals within the device. However, each of the QCLK resources can individually drive up to one chip quadrant, or they can be grouped together to drive multiple quadrants.

The number of available routed clock resources varies from device to device. See Table 1 for details.

Special Clock Networks

In addition to hard-wired and routed clock networks, there are other device-specific special resources in the ACT3 family. These resources cannot be driven by an internal logic signal.

IOPCL is a special hard-wired input for I/O modules. It is directly wired to the Preset and Clear inputs of all I/O registers. IOPCL functions as an I/O when no I/O preset or clear macros are used.

IOCLK is a hard-wired clock input for I/O modules (ACT3 device family). This is directly wired to each I/O register and offers clock speeds independent of the number of I/O modules being driven. IOCLK can also be used as an I/O.

Table 1 on page 2 summarizes the information on global clock networks – pad names, macro names, and the device families which support those networks. The table also indicates whether the clock network can be driven by an internal signal.

Clock Networks Architecture

Different clock networks have different architectures. A knowledge of clock network architectures will assist a designer in utilizing these resources in the most efficient manner.

Hard-Wired Clock Network Architecture

HCLK is hardwired from the clock input buffer to the clock select MUX in each R-cell. Figure 1 shows the HCLK network architecture for SX-A family devices.

Table 1 • Summary of Global Clock Network Resources

Input Pad Name	Type	Family	Number	Internal Drive Option	Macro	Note
CLK	Routed	ACT1, 40MX, RT/RH1020	1	No	CLKBIBUF CLKBUF	
HCLK	Dedicated	ACT3, RT1400, RTSX, RTSX-S eX, SX-A, 54SX	1	No	HCLKBUF	Connected only to sequential modulesf.
CLKA CLKB	Routed	ACT2, 1200XL, 3200DX, 42MX, RT/RH, 54SX, SX-A, eX	2	Yes	CLKBIBUF CLKBUF CLKINT	Use CLKINT for internal drive option. Does not include RH/RT 1020 devices.
IOCLK	Dedicated	ACT3, RT1400	1	No	IOCLKBUF	Connected to all I/O modules.
IOPCL	Special	ACT3, RT1400	1	No	IOPCLBUF	Connected to I/O module Set and Reset pins.
QCLK	Routed	3200DX, 42MX, RTSX-S, SX-A	4	Yes	QCLKBUF QCLKINT	Use QCLKINT for internal drive option. Only applies to RTSX72S. Only applies to A54SX72A.

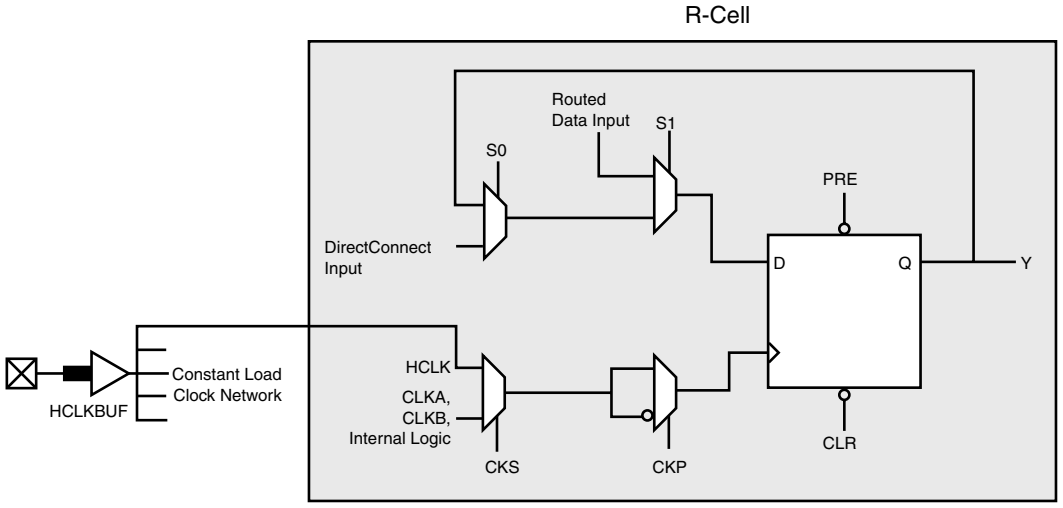

Figure 1 • HCLK Network for an SX-A FPGA Family

Elimination of programming elements (fuses) from the path makes the HCLK network the clocking resource with the lowest skew.

As it can be seen from Figure 1, the inputs of the dedicated clock networks are hard-wired to the pads. In other words, these resources cannot be driven by internal signals. Users should keep in mind that the hard-wired clock network is only connected to the clock input of sequential macros and therefore, it cannot be used to drive combinational cells. As a result, CC macros cannot be driven by the hard-wired clock network.

In device families with I/O registers (such as ACT3), a dedicated clock network is provided to drive the clock input of those registers with a guaranteed speed (IOCLKBUF). Note, these dedicated clock signals also cannot be connected anywhere else.

Routed Clock Network Architecture

Routed clock networks are capable of being driven by either external or internal signals via a MUX architecture. The CLKA and CLKB routed networks are identical. Signals are buffered prior to entering the clock network. Figure 2 on page 3 illustrates the architecture of these routed networks for the SX-A FPGA family (except A54SX72A – see Figure 3 on page 3).

As shown in Figure 2, the registers of the clock network can be clocked by either the positive or negative edge of the clock signal. If CLKA/B are not used externally, these clock pins must be set to logic LOW or HIGH on the board. It should not be left floating.

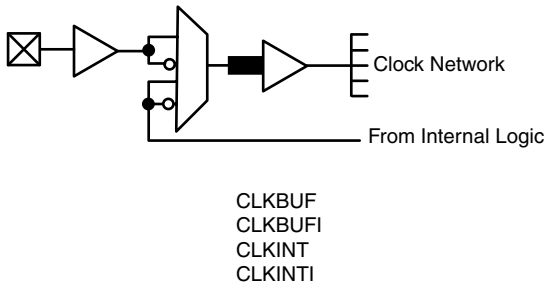

Figure 2 • SX-A Routed Clock Architecture

Routed clock networks can be driven by either external or internal signals and drive both sequential and combinational cells. Therefore, they can be used as the clock network to drive CC macros, especially in radiation-hardened and radiation-tolerant devices.

The quadrant clock architecture is similar to the above routed clocks except that it provides a low-skew network in a single-chip quadrant. This allows designers to use different quadrants of the low-skew network for different signals or clocks. This feature is especially valuable for designs in which there are several signals with strict timing skew requirements or multiple blocks driven by separate clock signals.

If the QCLK pins are not used, they can be configured as user I/Os. Figure 3 shows the architecture of the QCLK network in the A54SX72A device. The A54SX72A and RT54SX72S CLKA/CLKB networks contain an additional feature. Note, the internal logic is buffered so that it can drive both an external pad and the QCLK network.

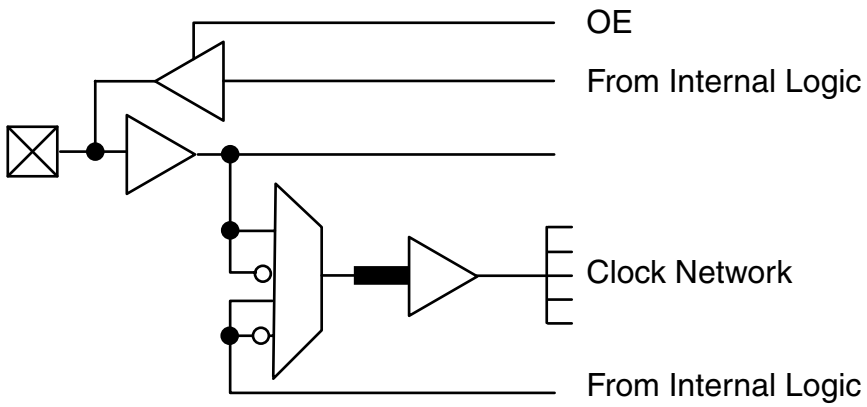

Figure 3 • A54SX72A Routed Clock Structure

Legacy device families (ACT1 prior to 1010B and 1020B) exploit row-buffered routes to establish a high-fanout clocking network. Figure 4 on page 4 illustrates the row-buffered clock network architecture for the 1010A FPGA family. In this architecture, clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Designs in device families with the global clock network architecture, as shown in Figure 4 on page 4, require more attention to place and route. The global clock network in the old FPGA families has considerable path delay and clock skew compared to the newer device families. Therefore, if the routing path lengths from the clock input pin to different registers are very different, there will be a considerable clock skew for those registers. In order to avoid this undesirable clock skew, Actel recommends that the registers driven by the same clock should be placed as close together as possible to prevent unnecessarily long paths for the clock signal. Actel's place-and-route tool will do this automatically, however Designer's Chip Edit provides a manual placement option if replacement of a few registers might improve timing characteristics of the design. One way to have influence on the place and route is to impose timing constraints on the place-and-route tool via SDC format constraints such as set_max_dely to limit delays between the registers (refer to the *Using Synopsys Design Constraints (SDC) with Designer* application note).

In the B die version of ACT1 family and similar devices (i.e. 40MX and RH), the clock network uses an independent TTL driver to increase the speed and drive of the clock network. Moreover, the row drivers are shorted together and this allows a lightly loaded row to offer charging current to a heavily loaded neighboring row. The result is a remarkably reduced clock skew between rows for a given placement.

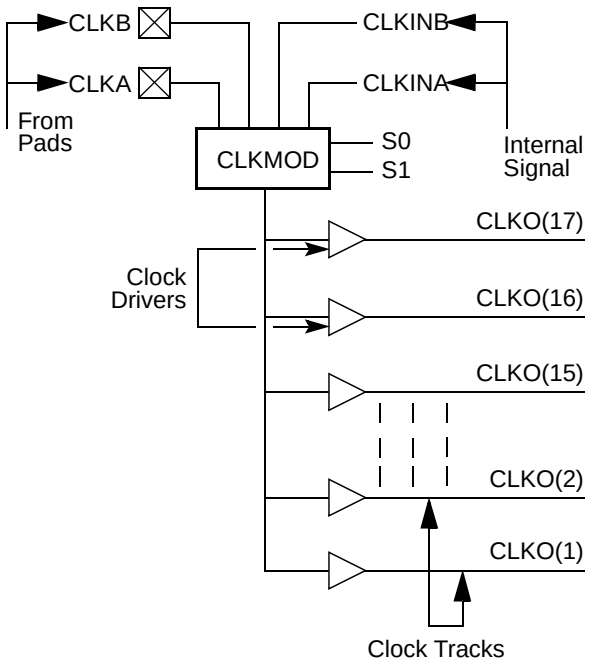

Figure 4 • *Clock Networks*

Clock Network Assignment

Except the hard-wired clock networks (and CLK in the ACT1 FPGA family), which only can be driven by external input signals, the other clock resources can be connected to either external or internal signals. Clock networks are assigned to different signals by instantiating the correct macros. Actel Designer Series software recognizes the macro and, based on its type, assigns the proper clock network to the signal driving that macro.

If designers do not specify global clock network assignments, synthesis tools will assign clock networks based on the priorities that are predetermined for the synthesis tool. These priorities are mostly set by the fanout of each signal. Synthesis tools attempt to assign the low skew resources to the signals in the design which have high fanout (e.g., global reset, enable or clock signals). QCLK networks also will not be instantiated automatically by the synthesis tools and therefore, CLKA and CLKB global resources are the first targets of the synthesis tool for assignment to high fanout non-clock signals. Designers can take control of the clock network assignment to improve their design performance by instantiating proper macros or attributes in the design. The following sections of this document will discuss these.

Dedicated Clock assignment

There are three dedicated clock networks: HCLK, IOCLK, and IOPCL.* Assignment of these clock networks to external signals is accomplished by instantiating HCLKBUF and IOCLKBUF macros. Figure 5 shows these macros.

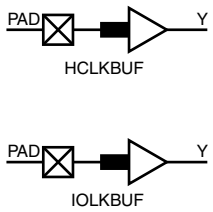

Figure 5 • *Dedicated Hard-Wired and I/O Clock Buffers*

Based on the design flow environment, there are different ways to appropriately instantiate these macros. In a schematic design, the user should simply import the macro from the Actel cell library into his design with its PAD and Y ports connected to the input clock signal and the clock network, respectively. In HDL flow designs, users can instantiate the macro in their code. Table 2 on page 5 describes the basic coding style for instantiation of HCLKBUF. If not instantiated manually, the HCLK network will be assigned at the discretion of the synthesis tool to the clock signals, driving only sequential cells with the highest fanout or most critical timing.

**IOCLK and IOPCL can only be found in ACT3 devices.*

Table 2 • HDL Instantiation of HCLKBUF

HDL instantiation of HCLKBUF	
VHDL	**Verilog**
library IEEE; **use** IEEE.std_logic_1164.**all**; **entity** design **is** **port** (…… : **in** std_logic; …… : out std_logic); end design; **architecture** rtl **of** design **is** -- Component Declaration **component** HCLKBUF **port** (PAD : in std_logic; Y :out std_logic); **end component**; **begin** -- Concurrent Statement U2 : HCLKBUF **port map** (PAD => input_clock, Y => clk_net);	module design (……); input ……; output ……; HCLKBUF U2 (.Y(clk_net), . .PAD(input_clock)); **……** **……** **endmodule**

Designers must avoid conflicts between pin configurations and HCLK network assignment of the input signals. Keep in mind, the HCLK network is hardwired to a specific pin number in each device, and the signal that drives this network must be assigned to that specific pin.

Routed Clock Assignment

Different routed clock macros have been provided for different purposes. They can be categorized as either I/O clock buffers or internal clock buffers. I/O clock buffers are used to route external clocks to the clock networks, while internal clock buffers assign internal signals to the routed clock network. Figure 6 illustrates these buffers for the CLKA or CLKB routed clock. (For the QCLK network, QCLKBUF and QCLKINT are similar to CLKBUF and CLKINT respectively).

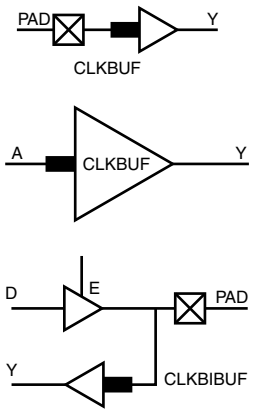

Figure 6 • Routed Clock Buffers

The instantiation of CLKBUF and QCLKBUF is very similar to HCLKBUF, explained in the previous section. The following section discusses the coding styles that achieve the most in network flexibility.

Assigning Internal Logic to the Routed Clock Network

In order to reduce delays and timing skew, internal signals with high fanout can be assigned to routed clock networks. CLKINT or QCLKINT should be instantiated in the design. This is similar to the use of CLKBUF except the input port name "A" replaces "PAD" for (Q)CLKINT. The outputs of these macros will be connected to the routed clock network.

In some cases, the clock signal is generated internally as a part of the FPGA design, while other sections of the FPGA use the generated clock. Actel recommends connecting the clocks to the global networks internally via instantiation of CLKINT or QCLKINT, rather than exporting them from the chip to the board and importing them back into the FPGA through another input pin.

Assigning a Regular I/O Pin to the Global Clock Network

In some cases, the designer needs to drive the clock network with non-clock input pins. This may be due to board limitations where the designated clock input pins cannot be used. In this case, the clock signal must be sourced by a regular input buffer (such as INBUF) and then connected to a global clock resource. This can be accomplished by simply connecting the output of the INBUF to the input of (Q)CLKINT.

Preserving Global Clock Networks

Synthesis tools usually assign clock buffers to clock signals. In some situations, where the clock resources are limited, the designer can control the usage of global clock resources by specifying which clocks do not need a clock buffer. This can be done by instantiating regular I/O buffers in a schematic design for the clock signals or adding attributes to the HDL code. Different synthesis tools use different attributes. Table 3 describes the attribute in both VHDL and Verilog for Synplicity.

Table 3 • Syn_noclockbuf Attribute of Synplicity

Attribute: Syn_noclockbuf
VHDL: (CLK is the name of the clock signal) attribute syn_noclockbuf : Boolean; attribute syn_noclockbuf of CLK : signal is true; Verilog: Module example (CLK); input CLK /* synthesis syn_noclockbuf =1 */; ……. endmodule

In the Synopsys synthesis tool, dont_use and dont_touch attributes are used for the same functionality.

Other Design Considerations

Many designers have concerns about global clock networks regarding the capability of driving I/O macros, reset or preset of registers, or the data inputs of flip flops. As mentioned earlier, I/O macros can be driven only by dedicated networks.

Routed clock networks CAN be connected to the reset or data inputs of the registers. The user should take care when driving data inputs of registers. If the routed clock network is connected to the register data input of a sequential cell, a buffer is needed in the data path. These buffers change the signal name and bring the data out of the clock network. In such cases, Designer software will insert the buffers (BUFF) automatically and issue a warning to notify the user.

In the case that the routed clock also drives combinational cells, the buffer insertion might be needed. The architecture of Actel's antifuse FPGA combinatorial cells is based on MUX blocks. If the routed clock network is connected to the signals feeding the data input of the MUX blocks (i.e. D0 through D4 in eX C-cell architecture), BUFF insertion is not needed. However, if the routed clock network drives the signals connected to the selection lines of the MUX blocks (i.e. A0 and B0 in eX C-cell architecture), Designer software will insert BUFF. The place-and-route tool issues a warning message when it carries out the automatic BUFF insertion.

In some cases, especially in designs which contain a large number of clock networks, it is necessary to implement clock networks using balanced buffer trees that are made of local routing resources. It is important to equalize the fanout for different branches of the clock tree to reduce clock skew between the branches. This can be done by using Actel Silicon Expert software, included on the Designer CD. The software will automatically balance the fanout of each branch, thus reducing clock skew.

There is one important factor in assigning signals to QCLK global networks. Since each QCLK network only spans a quadrant of the chip, a single macro cannot be driven by more than one QCLK network unless the networks are tied to each other. Designer will automatically tie quadrants together if the fanout for an assigned clock is greater than one quadrant.

However, Designer also automatically assigns the quadrant which the clock network will reside in. In some cases, the user wants the signal to be in a specific quadrant of the chip. There are three approaches to perform user specified QCLK assignment. If the driving signal is connected to an external input, the user can simply assign the signal to the desired QCLK input pin (via PinEdit or Pin file). By doing this the place-and-route tool is forced to assign the specified quadrant network to the desired input. The other two approaches should be taken after a preliminary layout. They require the use of ChipEdit and are especially useful when the driving signal is internal. One of them is to select and drag and drop one of the macros in the used QCLK network into the unused desired quadrant network. Then, the user needs to fix this placement in ChipEdit, commit the changes and do the place and route again. Since the new placement of that specific macro is fixed, the placer is forced to assign all other related (eventually the whole quadrant) macros to the new quadrant of the chip. The last approach is to simply drag and drop the used quadrant macro into the unused, desired one. This can be done in ChipEdit. Note that the new placement should be fixed and committed before exiting ChipEdit. Figure 7 on page 7 indicates two of the quadrant network macros.

Board Level Considerations

The shape of the clock signal's input to the FPGA is very important for proper functionality of the device. One important characteristic of an input clock signal is its slew rate. Actel's antifuse FPGAs have different slew-rate requirements for their clock input. The clock slew-rate requirements can be found in the device datasheet. If the slew rate of the clock signal is slower than the device requirement, the logic of the clock signal after the input buffer is unknown and will result in an improper functionality.

Another important parameter affecting the external clock signal shape is distortion. For example, improper line termination of the clock path can result in uncontrolled reflections (similar to wave reflection in a wave guide).

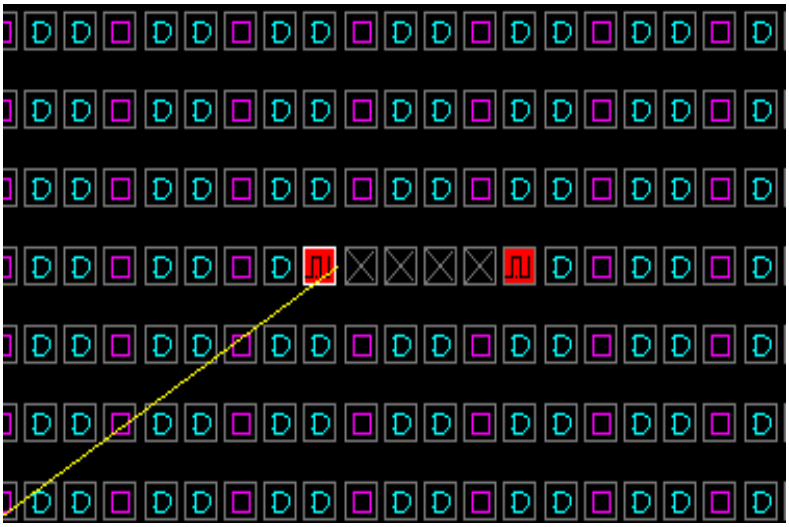

Figure 7 • *Quadrant Network Macros*

These uncontrolled reflections of the clock signal on the termination points might result in unwanted spikes on the clock. These spikes might be taken by FPGA logic as active clock edges which will result in mis-functionality of the design. If the clock line is not properly terminated, Actel recommends AC termination of the clock line which involves placing a resistor and capacitor pulled down to ground at the clock input of the device as shown in Figure 8 on page 7. This RC filter will stop the unwanted spikes from propagating into the FGPA.

The R and C values follow a general rule:

R should be equal to Z0, where Z0 is the impedance of the clock line. By selecting the proper value for R, the reflection coefficient of the line will cancel out the reflected signals. In other words, the reflections of the clock signal will be absorbed at the termination.

The C value should be chosen so that the RC-time constant is approximately 1/3 of the clock period. By doing this, the clock edges will be fast enough and acceptably noise free.

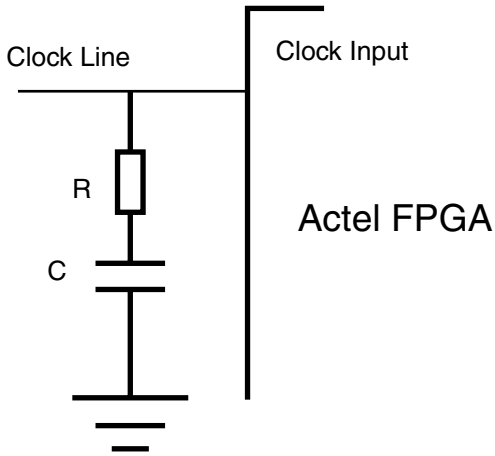

Figure 8 • *AC Termination at the Clock Input*

Conclusion

Actel devices provide different clock network resources for various applications. Utilizing the appropriate network enables users to achieve very high performance without going through extensive logic level reduction in their design. Actel global clock networks provide different levels of flexibility to fit best into various applications without sacrificing the efficiency of the design.

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