# Power-Up Behavior of ProASIC 500K Devices

## Introduction

Actel's ProASIC Flash family offers a number of desirable characteristics during power up. ProASIC family devices remain live at power up, and no configuration device is required due to the nonvolatile structure of Actel FPGAs. In other words, Actel devices retain the programmed design during power-up/down cycles. In addition, ProASIC devices draw very low transient currents compared to SRAM-based FPGAs during power-up cycles, which reduces the need for board level protection. Tristated I/Os during power up make the ProASIC family devices suitable for applications in which the user applies voltages to the I/Os even during the power-up sequence.

This application note focuses on the power-up characterization results and discusses aspects of I/O behavior such as power-up sequencing and output functionality.

For a better perception of the ProASIC family devices I/O behavior during power-up cycles, it would be useful to be familiar with the required power supply voltages and their interactions. ProASIC devices have two main power supplies: $V_{DDL}$ and $V_{DDP}$. $V_{DDL}$ provides the voltage supply for the array, and should always be set at 2.5V±8%. $V_{DDP}$ supplies the device I/O modules, and can be set to either 2.5V±8% or 3.3V±9%. Based on the value of $V_{DDP}$, I/Os can be configured to support multiple standards. For more information on this, refer to the *ProASIC 500K Family* datasheet.

The internal circuitry of the ProASIC devices establishes an interaction between the two power supplies during the power-up sequence. A p-n junction diode exists between $V_{DDL}$ and $V_{DDP}$ with its anode connected to $V_{DDL}$ as shown in Figure 1.

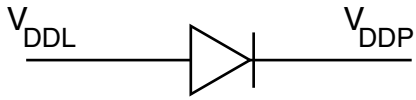


***Figure 1 •*** *P-N Junction Diode Between $V_{DDL}$ and $V_{DDP}$*

Therefore, when $V_{DDL}$ ramps up first, the $V_{DDP}$ will be pulled up to a diode voltage drop below $V_{DDL}$. This diode will be reverse-biased (and therefore ineffective) once $V_{DDP}$ reaches a value higher than $V_{DDL}$-0.7V. Another interaction of $V_{DDL}$ and $V_{DDP}$ during power up happens in I/O modules, since both supplies are required to support mixed-voltage I/O operation.

Note that all the characterizations and measurements in this document have been carried out in a laboratory environment and do not reflect worst-case conditions.

## Transient Current

During the power-up sequence, when $V_{DDL}$ reaches about 1V, the device draws a transient current. Due to the internal architecture of the ProASIC family devices, the peak value of the transient current is much smaller than in SRAM-based FPGA families.

As the $V_{DDL}$ rises during power up, the internal switches and logic start to turn on, resulting in a transient peak current. This current has been characterized for ProASIC family devices and does not exceed 38mA (with no decoupling capacitor attached to the power supplies). Table 1 indicates the typical transient current for different power-up sequences. $V_{DDP}$ is 3.3V and $V_{DDL}$ is 2.5V in these tests.

***Table 1 •*** *Transient Current in Different Power Up Conditions*

| | Power-Up Ramp Time | | | | | |
|---|---|---|---|---|---|---|
| **Power-Up Sequence** | **10µs** | **100µs** | **500µs** | **1ms** | **10ms** | **100ms** |
| **$V_{DDL}$ leads $V_{DDP}$ by 750ms** | 35.1 | 13.2 | 6.0 | 4.8 | 4.9 | 6.2 |
| **$V_{DDL}$ leads $V_{DDP}$ by 100ms** | 36.8 | 13.3 | 5.6 | 4.6 | ** | ** |
| **Simultaneous** | 21.4 | 9.5 | 4.1 | 3.1 | ** | ** |
| **$V_{DDP}$ leads $V_{DDL}$ by 100ms** | 11.6 | 3.3 | 2.2 | 2.5 | 2.1 | 2.0 |
| **$V_{DDP}$ leads $V_{DDL}$ by 750ms** | 11.8 | 3.4 | 2.5 | 2.5 | 2.2 | 2.15 |

***Note:*** **$V_{DDP}$=3.3V, $V_{DDL}$=2.5V*
***Less than 2 mA*

As shown in Table 1 on page 1, the transient current is extremely low compared to SRAM-based FPGAs. The transient current increases as the ramp time decreases. The characterization shows that the transient current occurs when the $V_{DDL}$ reaches the range of 0.7 to 1.2V. Figure 2 shows a sample transient current during the power-up sequence.

Experiments show that the transient current peak value also changes with decoupling capacitors. Higher decoupling capacitors result in higher transient current peaks. Note that there is no minimum requirement for the number or value of decoupling capacitors, and they vary from one design to another. The transient currents, shown in Table 1 on page 1, have been measured without decoupling capacitors.

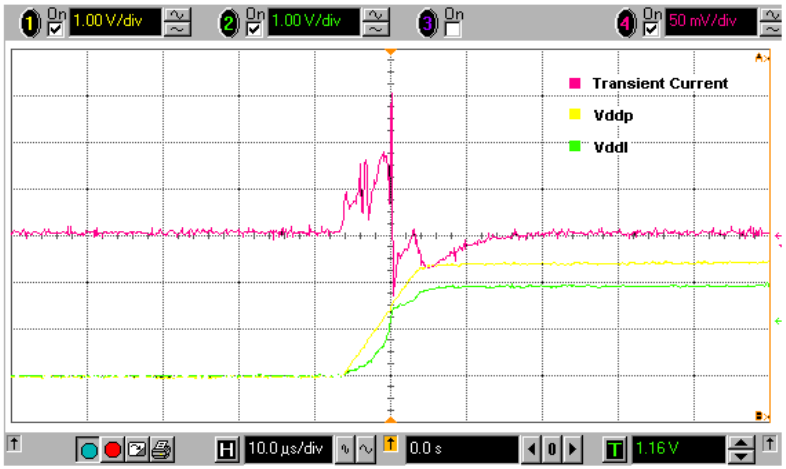


***Figure 2 •*** *Transient Current for Simultaneous Power Up of $V_{DDL}$ with 10ms Ramp Rate*

## Power-Up Behavior

Based on the different operating modes, the power-up sequences can be categorized in three ways:

- Case 1: $V_{DDL}$ and $V_{DDP}$ power-up simultaneously
- Case 2: $V_{DDL}$ leads $V_{DDP}$
- Case3: $V_{DDP}$ leads $V_{DDL}$

In pure 2.5V operation mode, the power-up condition will be Case 1 if $V_{DDP}$ and $V_{DDL}$ are tied together. In this case, the I/Os will remain tristated until the voltage level reaches the operating level (around 1V). After that, they become functional and will reflect the logic defined by the core. The logic on the outputs may be incorrect while the proper logic propagates from inputs to the outputs. Therefore, a short glitch might be expected on the outputs. The width of the glitch will be equal to the propagation delay time. The voltage level of the power supply at which the device becomes functional is nearly independent of the ramp-up rate.

There is Power-On-Reset (POR) circuitry in ProASIC devices which provides a POR signal to the I/O JTAG registers. In Case 1, the POR signal may not be generated. However, if the JTAG is not used or the JTAG reset is performed via the TRST pin, Case 1 imposes no power-up sequence restrictions.

In mixed-voltage operation (or in the single voltage operation when power supplies are not tied together), the power-up behavior of the ProASIC device family depends on its power-up sequence but not the ramp rates (except for the transient current). The internal circuitry between the $V_{DDL}$ and $V_{DDP}$ voltage sources requires more attention to the power-up sequence.

As mentioned earlier, a p-n junction diode exists between $V_{DDL}$ and $V_{DDP}$. This diode turns on if $V_{DDL}$ ramps up first. In this case, the diode will be forward-biased and will try to pull up $V_{DDP}$ to the $V_{DDL}$-0.7V level. If $V_{DDP}$ is pinned to ground before starting its power up, an excessive current will flow through the forward biased diode, which will damage the diode circuitry and the device functionality. However, if the board-level circuitry of $V_{DDP}$ is capable of being pulled up, then the p-n junction will not be forward-biased if $V_{DDL}$ powers up first. Figure 3 on page 3 indicates these cases.

When $V_{DDL}$ is powered up first, the POR circuit may not function correctly. However, the JTAG circuitry can also be asynchronously reset by asserting TRST low after power up or at any time during operation. If JTAG is not used and TRST is grounded, then the POR circuitry is not an issue during power up. In this case, if the $V_{DDP}$ source was not pinned to the ground before power up, then powering up the $V_{DDL}$ would not cause any problems since the p-n junction would not be forward-biased.

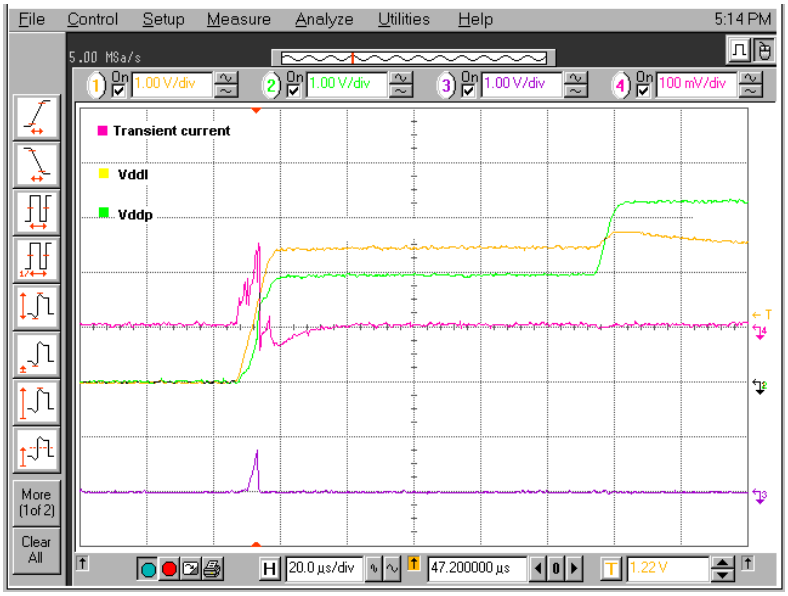


***Figure 3 •*** *Transient Current when $V_{DDL}$ Powers Up before $V_{DDP}$*

Based on the above discussion, the power-up behavior of ProASIC devices in Case 2 and Case 3 can be described as follows.

In Case 2, I/Os remain tristated before they become functional. The POR circuitry does not function, and the I/O JTAG registers will not be reset. However, if JTAG is not used, this will not be an issue. The user should note that the JTAG registers can also be reset using the TRST pin after power up but the I/O status will be unknown before the reset is performed. Furthermore, if the $V_{DDP}$ is pinned to ground while $V_{DDL}$ powers up, the diode circuitry between the voltage supplies will be damaged. After the I/Os become functional, as described in Case 1, a glitch might be experienced on the outputs.

In Case 3, since $V_{DDP}$ powers up first, the POR signal will be generated properly, and the p-n junction diode will be reversed-biased and remain safe. As in the previous cases, a glitch on the outputs may be expected.

## Conclusion

The transient current, which appears on the power supplies during power up, is extremely low in ProASIC devices. Moreover, the ProASIC device family I/Os are tristated during power up and before the device becomes functional. However, when power supplies power up separately, there are a few conditions that should be taken into account during power up. If JTAG is used in the device, $V_{DDP}$ must power up first for proper power-on-reset of JTAG registers. Due to the existence of a p-n junction diode between $V_{DDP}$ and $V_{DDL}$, the I/O power-supply ($V_{DDP}$) should power up first to avoid excessive current flow through the junction (if $V_{DDP}$ is pinned to ground during the power up), which may damage the internal circuitry of the device. Furthermore, the user should be aware of the possibility of unknown output states due to the propagation delay in the core logic. To avoid any damage to the device and proper functionality, Actel recommends that the $V_{DDP}$ power up before the core logic ($V_{DDL}$).

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