# Using ProASIC$^{PLUS}$ Clock Conditioning Circuits

## Introduction

The ProASIC$^{PLUS}$ devices include two clock-conditioning circuits on opposite sides of the die. Each clock conditioning circuit contains a Phase Locked Loop (PLL), several delay lines, clock multipliers/dividers, and all the circuitry for interconnection of the external bidirectional global pads and LVPECL pads to the global low-skew network.

The clock conditioning circuit allows users to perform the following functions:

- Clock phase adjustment as the PLL includes a multi-phase VCO
- Clock delay minimization using the various delay elements inserted in different paths
- Clock/frequency synthesis using the different dividers around the PLL
- Any combination of the above

Additionally, users can balance adjust the duty cycle of an incoming clock. The circuitry offers the flexibility to bypass the PLL core and to use the surrounding dividers and the delay elements only.

ProASIC$^{PLUS}$ PLLs allow users to configure them either statically or dynamically. For a PLL static configuration, the user can invoke ACTgen to set the various parameters. In dynamic mode, designers are able to set all the configuration parameters using either the external JTAG port or an internally-defined serial interface. The dynamic-mode PLL can be switched to static mode during operation by just changing a mode selection bit. This way the customer can have one stable static configuration, yet for selected sequences of events, he can switch to dynamic mode and run the clock at a different frequency if required. Repeating the whole design flow from rewriting the HDL code to programming the device with the new configuration is not necessary. Additionally, another benefit of using such a feature is that it allows users to compensate for temperature drift or other external changes.

## ProASIC$^{PLUS}$ PLL-Core Characteristics

The general characteristics of the PLL core are as follows: (For further details and characterized timing numbers, please refer to the *ProASIC$^{PLUS}$ APA Family* data sheet.)

- Input frequency range ($f_{in}$) 1.5 to 240 MHz
- Feedback frequency range ($f_{fb}$) 1.5 to 240 MHz
- Output frequency range ($f_{out}$) 6 to 240 MHz
- Maximum output clock jitter 200ps at 50ps jitter of $f_{in}$
- Maximum acquisition time 20µs
- Delay Line Programmable in 250ps increments from -4ns to +8ns; at 2.5V, 25 ºC
- Output Phase Shift 0, 90, 180, and 270 degrees
- Output duty cycle 50%
- Supply voltage 2.3 - 2.7V
- Analog supply voltage 2.3 - 2.7V
- Power Dissipation 10mW

## Clock Conditioning Circuit Features

This section introduces various features of the clock-conditioning block, discusses the various use models, and briefly describes the interface to the various external pads.

### Architecture

Figure 1 on page 2 illustrates the internal architecture of the ProASIC$^{PLUS}$ clock conditioning circuitry. Refer to the following sections for details regarding the use of the different elements of the block diagram.

## Interface and Access to the Global Network

The clock-conditioning block allows the connection from the ProASIC$^{PLUS}$ bidirectional global pads, the differential LVPECL pair, or even an internally generated signal to the global low-skew network and/or the PLL reference clock. The circuitry offers the possibility of driving the global networks with the outputs from the PLL core. The two-per-side global pads will only connect to the global networks or PLL on the same side and can be driven by different outputs from the same PLL core (Figure 2 on page 3). For example, one global clock network may be driven directly from the output clock of the PLL, whereas the other global clock network could be driven from a phase-shifted, a time-delayed/advanced, or a divided version of the same output clock.

Illustration B in Figure 2 on page 3 shows a feedback input and two other clock inputs of the PLL core. The first one, CLK, is the primary input clock, while CLKA, the second

input clock, is used as a reference clock for the secondary output clock of the PLL core. The CLKA input clock is used only when the PLL is in bypass mode.

### Configurability

As stated earlier, the clocking circuitry is fully reconfigurable using either Flash configuration bits (set in the programming bit-stream) or a simple asynchronous interface (dynamically accessible from internal user registers or the JTAG interface). This allows parameters, such as the PLL divide ratios, to be modified during operation without the need to restart the design cycle from the beginning. Refer to Actel's web site for future application notes regarding details on dynamic reconfiguration mechanisms and the needed configuration bits.

## Detailed Application Information

### Clock Division and Multiplication

Besides the PLL, the block contains four programmable dividers which are depicted in Figure 3 on page 3.

- The first divider "÷n" is located in the input path to provide integer division factors ranging from 1 up to and including 16.
- A second divider "÷m" is located in the feedback path, allowing multiplication of the incoming clock by factors ranging from 1 to 64.
- Two other dividers, "÷u" and "÷v," are located in the paths of the two output clocks, CLKA and CLKB, of the PLL. They allow further division of these outputs by factors of 1, 2, 3, and 4.

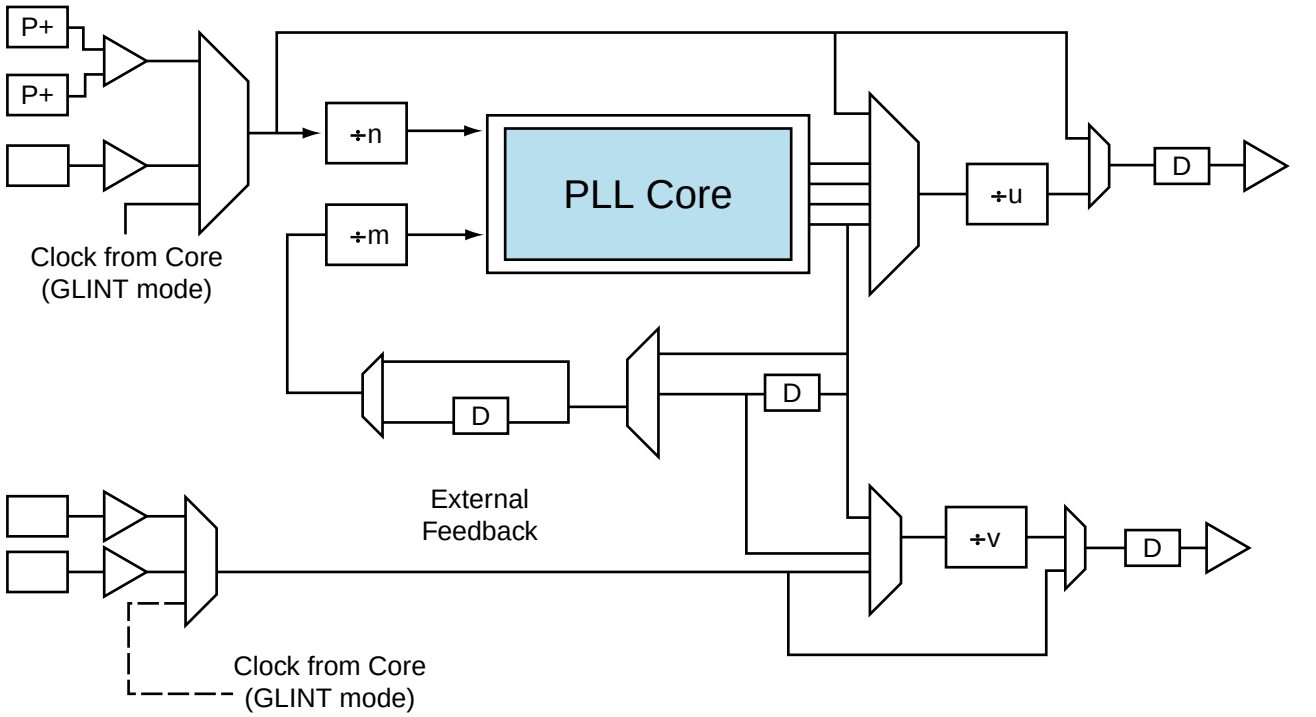


***Figure 1 •*** *Detailed Structure of the ProASIC$^{PLUS}$ Clock-Conditioning Circuitry*

As a consequence, the primary output clock frequency is given by

$$GLB = CLKOUTPLL \div u$$

and the secondary output clock frequency is given by

$$GLA = CLKOUTPLL \div v$$

In other words, the GLB and GLA frequencies are related according to the following equation:

Equation 1:

$$GLB = (u \times GLA) \div v$$

Overall, the user is able to define a wide range of multiplication and division factors. The GLB's frequency can be derived from the CLK frequency using the following equations:

Equation 2:

$$GLB = [m \div (n \times u)]$$

Equation 3:

$$GLA = [m \div (n \times v)]$$

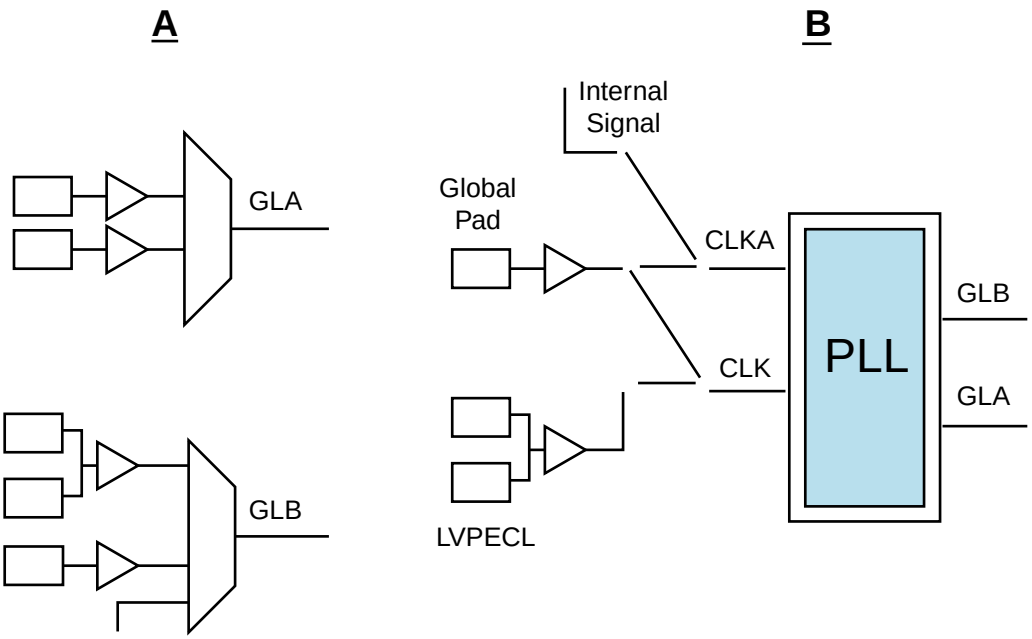


***Figure 2 •*** *External and Internal Interface to the Global Network (GLA and GLB) and to the PLL Reference Clock.*

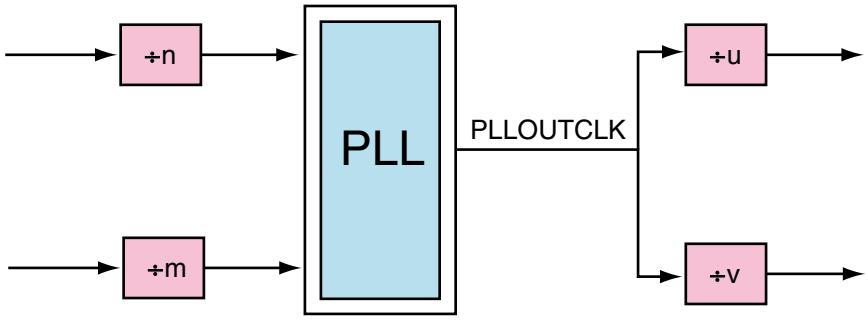


***Figure 3 •*** *Simplified Block Diagram of the Clock-Conditioning Block*

It is well known that arbitrary values of GLA and GLB cannot be synthesized for a given value of CLK. Equations 1, 2, and 3 allow users to check all the possible combinations of GLA and GLB frequencies.

### De-Skewing

The clock-conditioning block also performs positive and negative clock delay operations. Delay elements are placed in the output clock paths as well as in the feedback path. They allow up to 8ns delay with increments of 250ps. As shown in Figure 4 on page 4, these delays can be positive or negative. Using a delay element in the output clock path results in a positive output clock delay relative to the input reference clock CLK. Positive delay in the feedback path is equivalent to negative delay of the output clock, i.e. advancing the output clock relative to the input reference clock. This feature allows users to remove the delay due to the input clock pad, to meet setup time requirements, or to delay the clock to meet the clock-to-out timing requirements.

### Phase Shift

The PLL Core allows users to select one of 4 clock phases of the primary clock GLB – 0, 90, 180, and 270 degrees. The secondary clock GLA cannot be phase shifted as described in Figure 4 on page 4 and is tied to the 0° output phase of the PLL. The setting of the multiplexer selection lines is performed by the software and is transparent to users.

### Bypass Modes

The clock conditioning circuit allows GLA, GLB, or both to bypass the PLL core. This section describes the different ways to bypass the PLL core and covers the various possibilities of manipulating the input clock even when the PLL is bypassed

### GLB in Bypass Mode

As briefly depicted in Figure 5, the input clock can still be divided, delayed, or simultaneously divided and delayed. The setting of the control signals of various multiplexing units is transparent to the users as the software takes care of them.

Examples of the bypass mode of GLB are depicted in Figure 5 as dashed lines. Notice that the "÷n" divider is also bypassed, and divider "÷u" can be used in combination with the delay element.

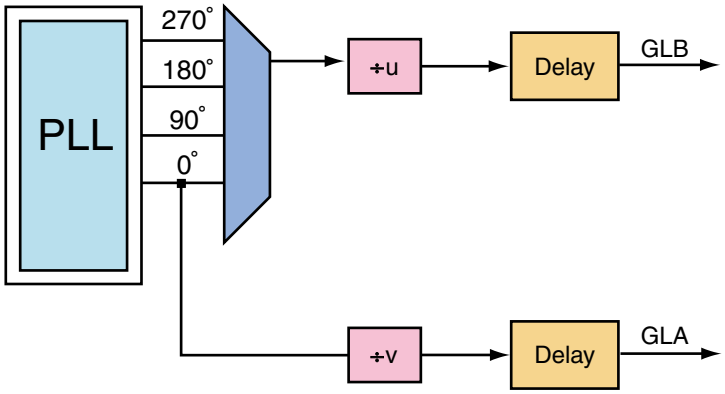


***Figure 4 •*** *Phase Shift of Primary Clock*

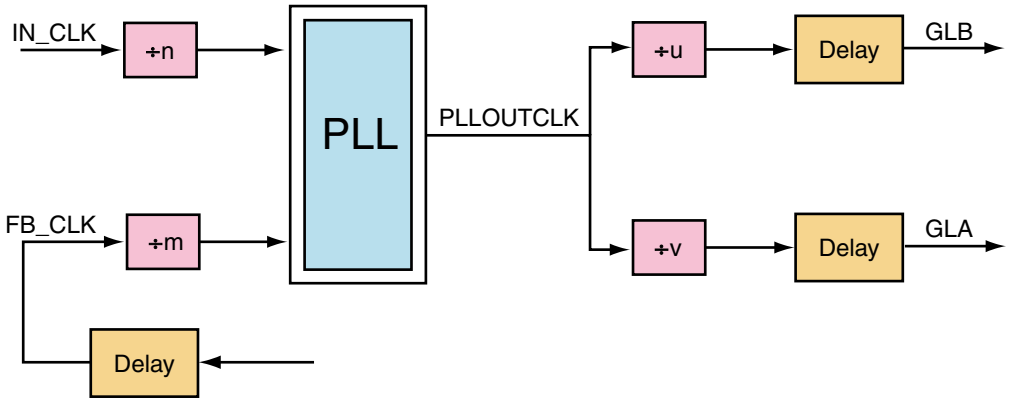


***Figure 5 •*** *Bypass Mode of the Primary Clock GLB*

### GLA in Bypass Mode

The scheme is similar to the one presented in the previous section for the primary output clock of the clock-conditioning circuitry.

### GLA and GLB Bypass Mode

In this mode the PLL core and the divider "÷n" are completely bypassed and the PLL core is switched off to save power. Dividers "÷u" and "÷v" can be used in combination with the delay elements to divide and/or delay the reference clock CLK. Additionally, the secondary output clock can have its own incoming reference clock as described in Figure 2 on page 3.

## Lock Function

A "Lock" signal is provided to indicate that the PLL has locked onto the incoming clock signal. Users can employ the "Lock" signal as a soft reset of the logic driven by GLB and/or GLA.

If the PLL is in bypass mode, an internal signal is automatically set to switch off the PLL core to avoid unnecessary power dissipation. The place and route tool configures this signal using a Flash bit. Notice that this signal is part of the dynamically controllable signal list for the aforementioned dynamic reconfiguration of the PLL.

### Internal and External PLL Feedback

The clock-conditioning circuitry allows the user to implement the feedback clock signal using either the output of the PLL, an internally generated clock or an external clock, as illustrated in Figure 6.

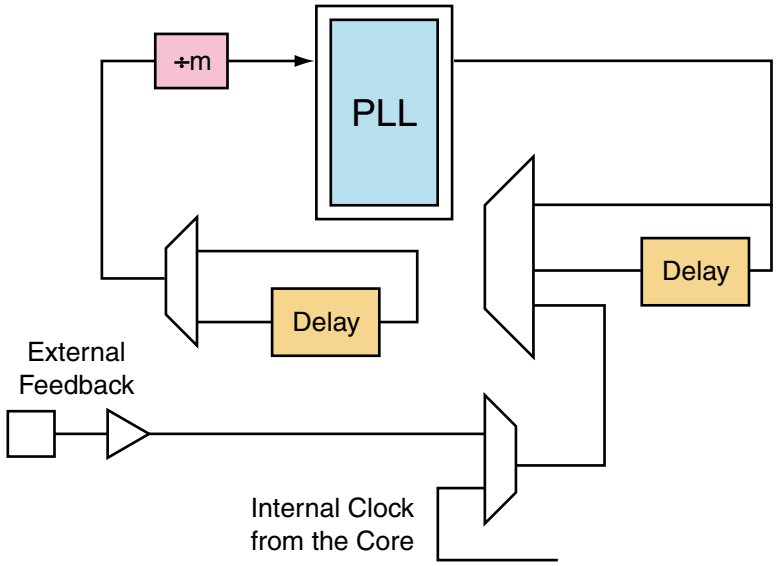


*Figure 6 • Block Diagram of the Feedback Circuitry*

## Integration of ProASIC[PLUS] PLL in an HDL Design

### The Primitive Port List

The following is a simplified Verilog description of the PLL primitive. It is intended to show the port list.

*module PLLCORE (GLA, GLB, LOCK, SDOUT, CLK, CLKA, EXTFB, SCLK, SSHIFT, SDIN, SUPDATE, MODE, FINDIV, FBDIV, OADIV, OBDIV, OAMUX, OBMUX, FBSEL, FBDLY, XLDYSEL, DLYA, DLYB, STATASEL, STATBSEL);*

***input*** *CLK, CLKA, EXTFB, SCLK, SSHIFT, SDIN, SUPDATE, MODE;*

***input*** *[4:0] FINDIV;*

***input*** *[5:0] FBDIV;*

***input*** *[1:0] OBDIV;*

***input*** *[1:0; OADIV;*

***input*** *[1:0] OAMUX;*

***input*** *[2:0] OBMUX;*

***input*** *[1:0] FBSEL;*

***input*** *[3:0] FBDLY;*

***input*** *[1:0] DLYA;*

***input*** *[1:0] DLYB;*

***input*** *XDLYSEL;*

***input*** *STATASEL;*

***input*** *STATBSEL;*

***output*** *GLA, GLB, LOCK, SDOUT;*

***endmodule***

The description of the PLL core output ports is as follows:

| | |
|---|---|
| GLB | Primary clock output |
| GLA | Secondary clock output |
| LOCK | PLL lock signal (when low the PLL is not locked) |
| SDOUT | Output of serial interface shift register |

The input ports can be divided into the following categories:

- Input Clocks
  - CLK — Input clock for primary clock
  - CLKA — Input clock for secondary clock. As explained in "ProASICPLUS PLL-Core Characteristics" on page 1 this input clock is used only in bypass mode.
  - EXTFB — External Feedback. Connects the output of the external feedback PAD to this port.
- Dividers
  - FINDIV [4:0] — Five-bit input divider. The range is from 1 (encoded as "00000") to 32 (encoded as "11111").
  - FBDIV [5:0] — Six-bit divider in the feedback path. It is actually a multiplier of the input frequency. The division values range from 1 (encoded as "000000") to 64 (encoded as "1111111").

  - OBDIV [1:0] Two-bit divider in primary clock (GLA) output path. The division values range from 1, encoded as "00," to 4.
  - OADIV [1:0] Two-bit divider in secondary clock (GLB) output path. The division values range from 1 to 4.
- Delays
  - DLYA[1:0] Additional delay value for GLA output. 00 means no delay.
  - DLYB[1:0] Additional delay value for GLB output. 00 means no delay.
  - FBDLY [3:0] Feedback delay values. The feedback delay values can be selected in 250ps steps "0000" encodes 250ps while "1111" means 4ns.
- Global Network and Feedback Path Multiplexing

The setting of these select lines is performed by the software and is completely transparent to the user. The description is provided for completeness of the presentation.

OBMUX [2:0] Global multiplexing in GLB path. The various values of the selection and their significance are as follows:
000 – Select Bypass B
001 – Select Global MUXB out
010 – Select output of Delay Line
011 – Reserved
100 – Select Phase 0 of VCO for primary output clock
101 – Select Phase 90 of VCO for primary output clock
110 – Select Phase 180 of VCO for primary output clock
111 – Select Phase 270 of VCO for primary output clock

OAMUX [1:0] Global multiplexing in GLA path.
00 – Select Bypass A
01 – Select Global MUX A out
10 – Select Output of Delay Line
11 - Select Phase 0 of VCO

FBSEL[1:0] Selection of the PLL feedback clock
00 – Ground MUX input. Used for standby mode in Standby logic block
01 – Selects output of the delay line in the internal feedback path
10 – Selects phase 0 of VCO output and skips delay elements in the internal feedback path
11 – Selects the external feedback that can be an internal net or an external input.

**Input Multiplexing**

STATASEL, STATBSEL Static Multiplexor selection for CLKA and CLK inputs of the PLL (See illustration B in Figure 2 on page 3.)

**PLL Configuration Mode**

MODE indicates dynamic or static mode of the PLL. If set to "0," the PLL configuration mode is static.

All the other inputs, namely SCLK, SSHIFT, SDIN, SUPDATE, and XDYSEL, are used when the dynamic configuration is selected and will be described in a separate application note.

## The PLL Generation

ACTgen, the Actel macro-generator, helps users to set the various parameters of the PLL and to generate HDL and EDIF description files. Figure 7 on page 7 shows the main menu for the PLL macro generation.

The PLL generation tool offers different options that are described briefly in the following subsections. For more details, please refer to the *Guide to ACTgen Macros*.

The "Output" sub-window allows users to select the output file name and format. The tool generates VHDL, Verilog, or EDIF file formats.

The Configuration Tab helps the user to select and set the following parameters:

- PLL Configuration Mode to be either static or dynamic
- The PLL Feedback clock to be internal, de-skewed, or external
- The output clocks to be either primary, secondary, or both
- The Input Clock Frequency (must be within the 1.5 - 240 MHz range)
- The "Primary Clock" sub-dialog box allows the user to specify the output frequency, the delay, the phase shift (if any), and whether or not the PLL is bypassed.
- The "Secondary Clock" sub-dialog box helps the user to specify the output frequency, the delay (if any), and whether or not the PLL is bypassed. Notice that if the PLL is bypassed, the user has the opportunity to specify a different input clock frequency for the secondary output clock (see Figure 1 on page 2).

The bottom of the main menu is a trace window where the tool provides useful information on the PLL generation. Please read these messages carefully in case the tool fails to generate the correct combination of input and output frequencies. For more information on the wide range of combinations, please use Equations 1, 2, and 3 provided in "Clock Division and Multiplication" on page 2.

The "Port" Tab of Figure 8 helps the user customize the port names to fit his design signal names. Notice that some ports are unavailable because of the configuration options specified in the Configuration Tab described earlier.

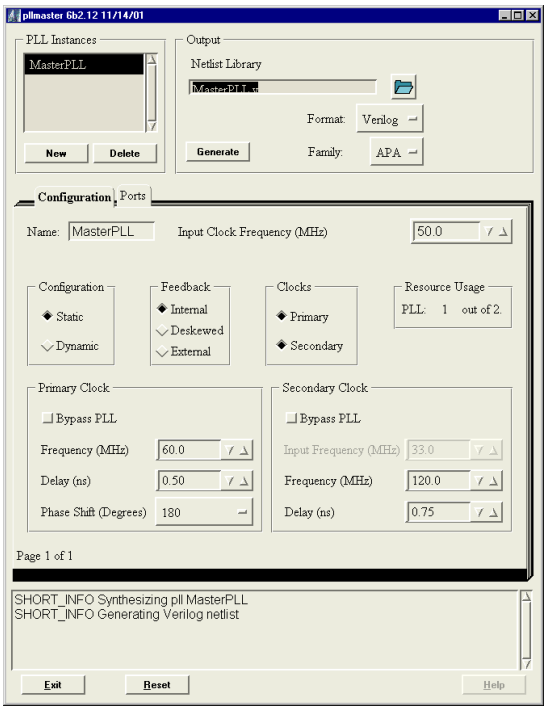


***Figure 7 •*** *Main Menu of the PLL Generation Tool*

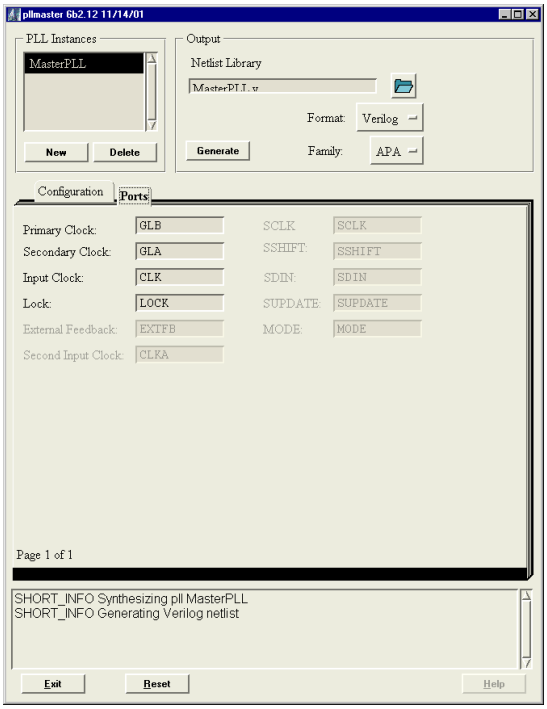


***Figure 8 •*** *Ports Tab for PLL Ports Names Customization*

After setting all the needed parameters, users can generate the HDL or EDIF description by clicking the "Generate" button. Additionally, users can generate several PLL configurations. ACTgen allows them to save the session results and messages in a "log" file.

The following is a Verilog HDL description of a legal PLL core configuration and the surrounding circuitry. Notice that the file header provides a summary of all the user parameter settings.

```
'timescale 1ns/10ps
// Name = MasterPLL
// configuration = static
// clocks = secondary
// feedback = external
// part family = APA
// input clock frequency = 50 MHz
// feedback select = 3
// feedback delay line = 2
// primary clock frequency = 60 MHz
// primary clock delay = 0.5 ns
// primary clock phase shift = 180 degrees
// input clock divider = 5
// feedback divider = 12
// feedback select = 3
// primary clock divider = 2
// primary clock select = 6
// primary clock delay line = 2
// secondary clock frequency = 120 MHz
// secondary clock delay = 0.75 ns
// secondary clock divider = 1
// secondary clock select = 2
// secondary clock delay line = 0
module MasterPLL (GLB, GLA, EXTFB, LOCK, CLK);
output GLB;
output GLA;
input EXTFB;
output LOCK;
input CLK;
PLLCORE U0(.GLA(GLA), .GLB(GLB), .LOCK(LOCK),
.SDOUT(n1), .CLK(CLK), .CLKA(VSS), .EXTFB(EXTFB),
.SCLK(VSS), .SSHIFT(VSS), .SDIN(VSS), .SUPDATE(VSS),
.MODE(VSS), .FINDIV4(VSS), .FINDIV3(VSS),
.FINDIV2(VDD), .FINDIV1(VSS), .FINDIV0(VSS),
.FBDIV5(VSS), .FBDIV4(VSS), .FBDIV3(VDD),
.FBDIV2(VSS), .FBDIV1(VDD), .FBDIV0(VDD),
.OADIV1(VSS), .OADIV0(VSS), .OBDIV1(VSS),
.OBDIV0(VDD), .OAMUX1(VDD), .OAMUX0(VSS),
.OBMUX2(VDD), .OBMUX1(VDD), .OBMUX0(VSS),
.FBSEL1(VDD), .FBSEL0(VDD), .FBDLY3(VSS),
.FBDLY2(VSS), .FBDLY1(VDD), .FBDLY0(VSS),
.XDLYSEL(VSS), .DLYA1(VSS), .DLYA0(VSS),
.DLYB1(VDD), .DLYB0(VSS), .STATASEL(VSS),
.STATBSEL(VSS));
PWR U1(.Y(VDD));
GND U2(.Y(VSS));
endmodule
```

### Integration in an HDL Flow

The integration of the generated PLL module is similar to any VHDL component or Verilog module instantiation in a larger design; i.e., there is no special requirement that users need to take into account to successfully synthesize their designs.

For simulation purposes, users need to refer to the VITAL or Verilog library that includes the functional description and the associated timing parameters.

These libraries are available under

```
<Designer_Installation_Directory>\lib\vtl\95
\apa.vhd
```

```
<Designer_Installation_Directory>\lib\vlog\a
pa.v
```

## Board-Level Considerations

The "analog" voltages of the PLL are AVDD and AGND. If the PLL is to be used, the analog ground can be connected to the system ground, while AVDD should be tied to noise-free 2.5V.

If the design does not use the PLLs, the place-and-route tools will disable the PLLs to reduce the device power consumption. The board recommendation is to float the AVDD and to ground AGND. This recommendation helps reduce the noise on the board as well as the power supply needs.

If the PLLs are to be used, board layout designers need to be careful with the analog power pins. These pins must be kept free during place and route of the design. On the board, designers need to add an RC filter (5Ω, 200nF ceramic) in front of the analog power. Actel recommends placing the RC filter close to the package pin and minimizing inductance on the capacitor, resistor, and traces.

http://www.actel.com

**Actel Europe Ltd.**
Maxfli Court, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
**Tel:** +44 (0)1276 401450
**Fax:** +44 (0)1276 401590

**Actel Corporation**
955 East Arques Avenue
Sunnyvale, California 94086
USA
**Tel:** (408) 739-1010
**Fax:** (408) 739-1540

**Actel Asia-Pacific**
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
**Tel:** +81-(0)3-3445-7671
**Fax:** +81-(0)3-3445-7668

5192688-0/1.02