ProASIC^{PLUS} Evaluation Board

User's Guide

Actel

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Introduction

Thank you for purchasing Actel's ProASIC^{PLUS} Evaluation Board.

The purpose of this user's guide is to provide you with information so you can easily evaluate the ProASIC^{PLUS} devices.

This is the first release of the user's guide. The most up-to-date version of this guide is available at:

http://www.actel.com/products/tools/hw.html

Document Contents

Chapter 1 - Contents and System Requirements describes the contents of the ProASIC^{PLUS} Evaluation Kit.

Chapter 2 - Setup and Self Test describes how to setup the ProASIC^{PLUS} Evaluation Board and how to perform a self test.

Chapter 3 - Hardware Description describes the components of the ProASIC^{PLUS} Evaluation Board.

Appendix A - Board Connections lists a board connection table.

Appendix B - Board Schematics show illustrations of the ProASIC^{PLUS} Evaluation Board.

Appendix C - Product Support describes our support services.

Document Assumptions

This user's guide assumes the following:

- You intend to use Actel's Libero software.
- You have installed and are familiar with Actel's Libero software.
- You are familiar with the VHDL or Verilog hardware description language.
- You are familiar with UNIX workstations and operating systems or PCs and Windows operating systems.

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Contents and System Requirements

This chapter describes the differences between the three versions of the ProASIC^{PLUS} evaluation board. This chapter also details the contents of the ProASIC^{PLUS} evaluation kit and provides power supply and software system requirements.

Evaluation Kit Contents

The ProASIC^{PLUS} evaluation kit has three board versions.

Note: There is no socket on these boards.

APA-EVAL-BRD1

This board contains all the surrounding circuitry, but no APA device. For this board, it is assumed that you will acquire a device and solder it to the board yourself. This allows you to use the board with any device in the APA family.

APA-EVAL-BRD300

Same as BRD1 but with an APA300 device mounted.

APA-EVAL-BRD075

Same as BRD1 but with an APA075 device mounted.

When you purchase any of the above board versions, you also receive the following:

- Evaluation board - one of the three listed above
- The ProASIC^{PLUS} Evaluation Board User's Guide
- Customer Letter
- CD with design examples

For the CD contents, review the ReadMe.doc file at the top level of the CD. As more design examples become available, the CD contents will change. For the latest design examples, refer to the Hardware Tools section of the Actel website:

http://www.actel.com/products/tools/hw.html

Power Supply and Software Requirements

This section describes power supply and software requirements for the ProASIC^{PLUS} evaluation kit.

Power Supply

The ProASIC^{PLUS} evaluation board requires the following:

- Wall mount power supply
- 9V, 500mA supply with 2.1mm female connector P5 type
- Digikey part number T413-P5P-ND for US
- Digikey part number T408-P5P-ND for Europe

Software

Each ProASIC^{PLUS} evaluation board requires a different version of the software.

APA-EVAL-BRD075

This board can use the free evaluation Libero Silver version, which does not include simulation. To include simulation, use the Libero Gold version.

APA-EVAL-BRD300

This board requires a full Libero Platinum license.

APA-EVAL-BRD1

With the blank board, you can select any device from the ProASIC^{PLUS} family in a 208 PQFP footprint and solder it to the board yourself.

Use the appropriate software for the device you choose. For software support details, refer to the Actel Website:

http://www.actel.com/products/tools/support.html

2 Setup and Self Test

Software Installation

Since this package does not include software, this guide does not provide software installation instructions. For software installation instructions, refer to the Actel Installation and Licensing Guide at:

http://www.actel.com/products/tools/libero/docs.html

Testing the Evaluation Board

If the evaluation board is shipped directly from Actel, it contains a test program that determines if the board works properly.

To test the evaluation board:

1. **Supply power to the board.**
2. **Turn on the ON/OFF switch.**
3. **Perform the actions described in** Table 2-1**.**

Table 2-1. Evaluation Board Test

Action	Result	Pass/Fail
Press PB1 multiple times, but not too fast	A sequence of LEDs light up	Pass
Press and hold SW1	All LEDs are unlit	Pass
Press and hold SW2	All LEDs light up except DS1	Pass
Press and hold SW3	A random sequence of LEDs light up while you hold the switch	Pass
Press and hold SW4	The LED is lit/unlit in a 01101010 pattern	Pass
Any two switches are pressed together	Creates a 00100110 pattern.	Pass

Programming the Test file

If you want to retest the evaluation board, you can reprogram the board using the test program at any time. Use the STAPL file test.stp or the bitstream file test.bit. These files are included on the Evaluation Kit CD. Table 2-2 describes the actions you should perform when retesting your evaluation board.

This design is currently implemented for the APA300 device. If you have a device of a different size, you can recompile the design into other device sizes. The design files are available under actelprj/eval in the Evaluation Kit CD.

For instructions on programming the device using Flash Pro, refer to the Flash Pro User's Guide at:

http://www.actel.com/techdocs/manuals/docs/flashproUG.pdf

Table 2-2. Retesting the Evaluation Board

Action	Result	Pass/Fail
Press PB1 multiple times, but not too fast	Count sequence should be visible on the LED	Pass
Press and hold SW1	All LEDs are unlit	Pass
Press and hold SW2	All LEDs are lit	Pass
Press and hold SW3	Count sequence runs while you hold the switch	Pass
Press and hold SW4	LED is lit/unlit alternately in a 10101010 pattern	Pass
Any two switches are pressed together	Creates a 00110011 pattern	Pass

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Hardware Description

This chapter describes the components of the evaluation board. See Figure 3-1 for a schematic of the evaluation board.

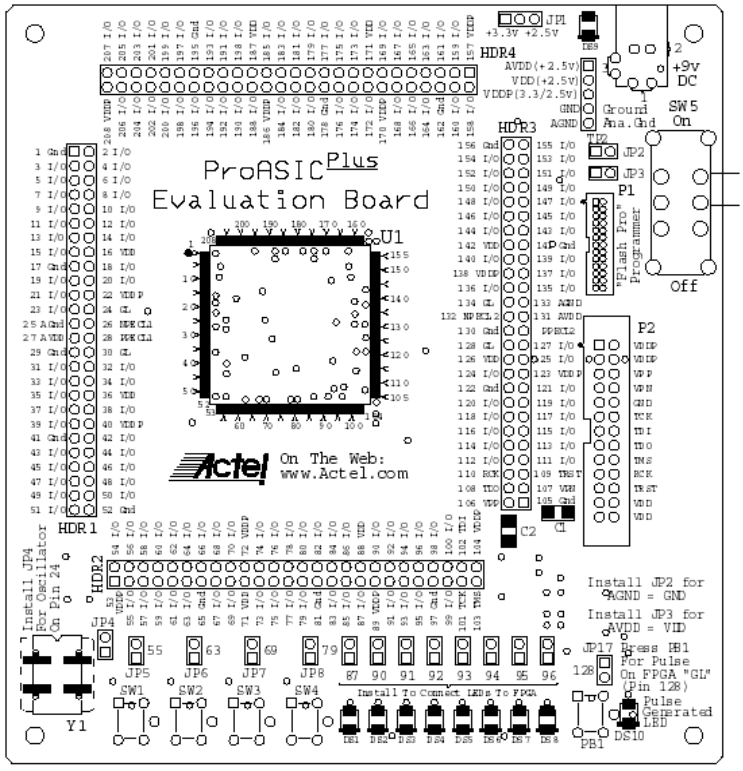

Figure 3-1. ProASIC Plus Evaluation Board

The ProASIC Plus evaluation board consists of the following:

- Wall mount power supply connector, with switch and LED indicator
- Jumper to select between 2.5V and 3.3V I/O voltages
- 40MHz oscillator and manual clock option

- Small program header (compatible with both Flash Pro and Silicon Sculptor)
- Four switches (provides input to the device)
- eight LED (driven by outputs from the device)
- Jumpers (allows disconnection of all external circuitry from the FPGA)

For further information, refer to the following appendices:

Appendix A – Board Connections

Appendix B – Board Schematics

Power Supplies

The evaluation board requires the following power supplies:

- Wall mount power supply
- 9V, 500mA supply with 2.1mm female connector P5 type

  Digikey part number T413-P5P-ND for US

  Digikey Part Number T408-P5P-ND for Europe
- The power is controlled by an On/Off switch.
- An LED DS9 indicates the presence of a working wall mount supply

  JP1 can be used to select either 3.3V or 2.5V for the Device I/O Voltage

  JP2 connects AGND to GND for the use of the PLL.

  JP3 connects AVDD to VDD for the use of the PLL.

  Note: The five pin header next to the power supply connection can also be used to drive power to the board from a lab supply.

Programming Headers

A small form programming header, which is suitable to use with both the Flash Pro and Silicon Sculptor II is supplied with the board. The footprint for the large programming header is on the board, but has not been populated.

When using Flash Pro, use the STAPL(.STP) file to program the device.

Silicon Sculptor II requires the ISP programming adapter module SMPA-ISP-ACTEL-2-KIT, then you can use either the bitstream (.BIT) file or STAPL (.STP) file.

Clock Circuits

The evaluation board has two clock circuits, the 40MHz oscillator and the manual clock.

40MHz Oscillator

The 40MHz oscillator on the board is connected to JP4. JP4 connects the clock to pin 24 of the devices. Pin 24 is a global input pin.

To use pin 24 for a different clock signal, disconnect JP4.

If you want to use a different Clock Frequency, purchase the Crystal from Epson programmed to a variety of frequencies. The SG-8002JC40.000M-PCC from Epson is also available through Digikey.

Manual Clock

When activated, the manual clock button (PB1) lights DS10 the pulse generated LED and generates a pulse. This is connected to JP17. JP17 connects to pin 128 of the device. Pin 128 is a global input pin.

If you want to use pin 128 for a different clock signal, disconnect JP17.

LED Device Connections

Eight LED are connected to the device via jumpers. If the jumpers are in place, the device I/O can drive the LED. The LED changes based on the following output:

- A 1 on the output of the device lights the LED.
- A 0 on the output of the device switches off the LED.
- An unprogrammed or tristated output may show a faintly lit LED

Table 3-1 lists the LED/device connections.

If you want to use the device I/O for other purposes, remove the jumpers.

Table 3-1. LED Device Connections

LED	Device Connection
DS1	87
DS2	90
DS3	91
DS4	92
DS5	93
DS6	94
DS7	95
DS8	96

Switches Device Connections

Four switches are connected to the device via jumpers. If the jumpers are in place the device I/O can be driven by the following switches:

- Pressing the switch drives a 1 into the device. The 1 continues to drive while you hold the switch.
- Releasing the switch drives a zero into the device.

Table 3-2 lists the switch/device connections.

If you want to use the device I/O for other purposes, remove the jumpers.

Table 3-2. Switch Device Connections

Switch	Device Connection
SW1	55
SW2	63
SW3	69
SW4	79

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Board Connections

This appendix lists a table for board connections.

Table A-1 shows the board connections.

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
1	GND	GND	GND	GND	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
16	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
17	GND	GND	GND	GND	GND	GND	GND	GND

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
18	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
24	GL	GL	GL	GL	GL	GL	GL	JP4
25	AGND	AGND	AGND	AGND	AGND	AGND	AGND	JP2
26	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
27	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	JP3
28	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)
29	GND	GND	GND	GND	GND	GND	GND	GND
30	GL	GL	GL	GL	GL	GL	GL	GL
31	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
36	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
37	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
38	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP5
56	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
59	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP6
64	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP7
70	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
71	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP8

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
80	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP9
88	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
89	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP10
91	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP11
92	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP12
93	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP13
94	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP14
95	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP15
96	I/O	I/O	I/O	I/O	I/O	I/O	I/O	JP16
97	GND	GND	GND	GND	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
101	TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK
102	TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI
103	TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
105	GND	GND	GND	GND	GND	GND	GND	GND
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO
109	TRST	TRST	TRST	TRST	TRST	TRST	TRST	TRST
110	RCK	RCK	RCK	RCK	RCK	RCK	RCK	RCK
111	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
122	GND	GND	GND	GND	GND	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
126	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
127	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
128	GL	GL	GL	GL	GL	GL	GL	JP17
129	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)	PPECL (I/P)
130	GND	GND	GND	GND	GND	GND	GND	GND
131	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	JP3
132	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL	NPECL
133	AGND	AGND	AGND	AGND	AGND	AGND	AGND	JP2
134	GL	GL	GL	GL	GL	GL	GL	GL
135	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND	GND	GND	GND	GND

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
142	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
143	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND	GND	GND	GND	GND
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND	GND	GND	GND	GND

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
163	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
172	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
184	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
185	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
188	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND	GND	GND	GND	GND
196	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

Table A-1. Board Connections

Pin No.	APA 075	APA 150	APA 300	APA 450	APA 600	APA 750	APA 1000	Board Connect
205	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

B

Board Schematics

This appendix shows illustrations of the ProASIC Evaluation Board.

Figure B-1 shows a board schematic.

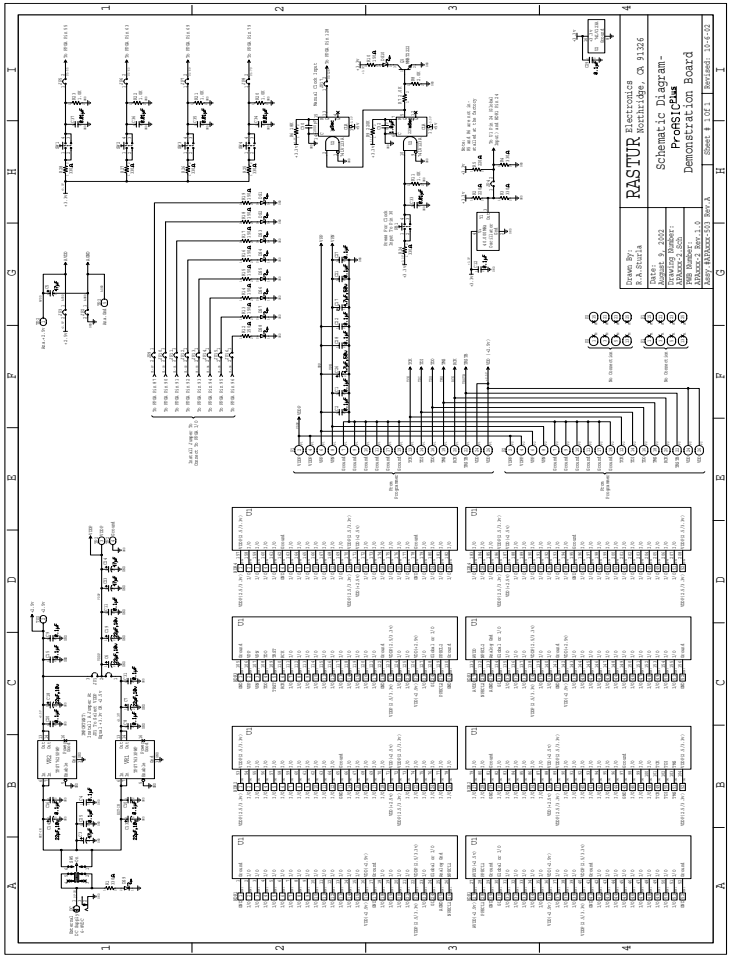

Figure B-1. Board Schematic

Figure B-2 shows a schematic of the ProASIC^{PLUS} Evaluation Board.

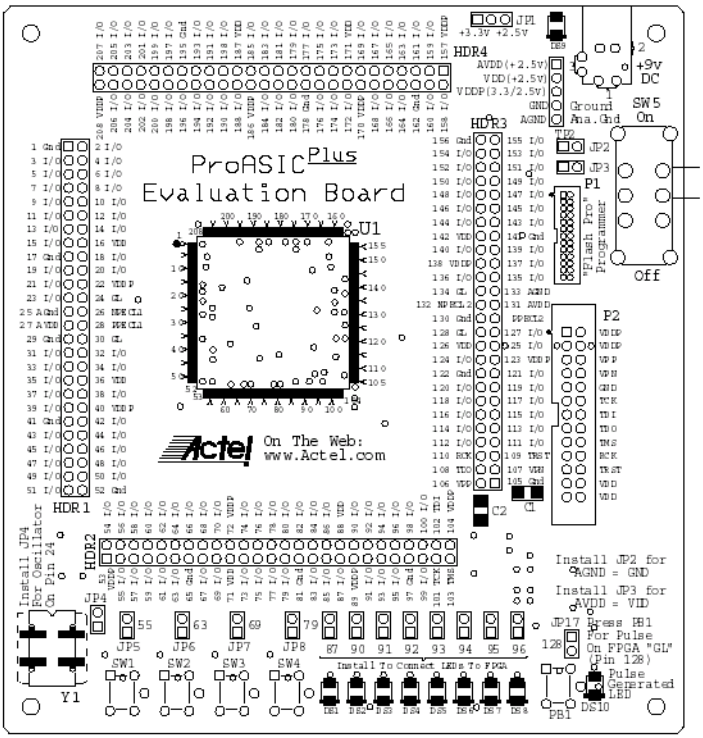

Figure B-2. ProASIC ^{PLUS} *Evaluation Board*

Figure B-3 shows a board schematic.

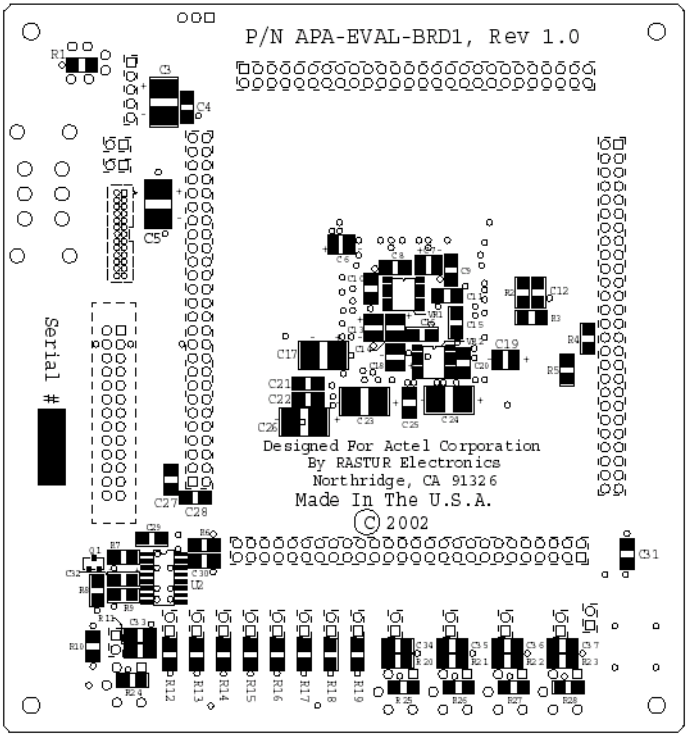

Figure B-3. Board Schematic

C

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480
From Southeast and Southwest U.S.A., call (408) 522-4480
From South Central U.S.A., call (408) 522-4434
From Northwest U.S.A., call (408) 522-4434
From Canada, call (408) 522-4480
From Europe, call (408) 522-4252 or +44 (0) 1276 401500
From Japan, call (408) 522-4743
From the rest of the world, call (408) 522-4743
Fax, from anywhere in the world (408) 522-8044

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Website

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(408) 522-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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