RT54SX-S
RadTolerant FPGAs for Space Applications

Special Features for Space

- First Actel FPGA Designed Specifically for Space Applications
- Up to 2,012 SEU Hardened Flip-Flops Eliminate Software TMR Necessity (LET th > 40, GEO SEU Rate < 10^{-10} upset/bit-day)
- Up to 100 krad (Si) Total Ionizing Dose (TID) Parametric Performance Supported with Lot-Specific Test Data
- Single Event Latch-Up Immunity
- Pin Compatibility Allows Prototyping with Commercial SX-A and Mission Implementation with Radiation-Tolerant RT54SX-S
- Deterministic Power-Up with Support for Hot-Swapping Capabilities
- Cold-Sparing Capability
- Devices Available from TM1019.5-tested Pedigreed Lots
- Slow Slew Rate Option

Standard Features

- Very Low Power Consumption (Up to 68 mW at Standby)
- Configurable I/O Support for 3.3V/5V PCI, LVTTL, TTL, and CMOS
- 3.3V and 5V Mixed Voltage Operation with 5V Input Tolerance and 5V Drive Strength
- QML Certified Devices
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Configurable Weak Resistor Pull-up or Pull-down for Tristated Outputs at Power-Up
- 100% Circuit Resource Utilization with 100% Pin Locking
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Dedicated JTAG Reset (TRST) Pin
- Deterministic, User-Controllable Timing
- JTAG Boundary Scan Testing In Compliance with IEEE Standard 1149.1
- 0.25µm Metal-to-Metal Antifuse Process Generation

Leading Edge Performance

- 230 MHz System Performance
- 8.7 ns Input Clock to Output Pad
- 310 MHz Internal Performance

Specifications

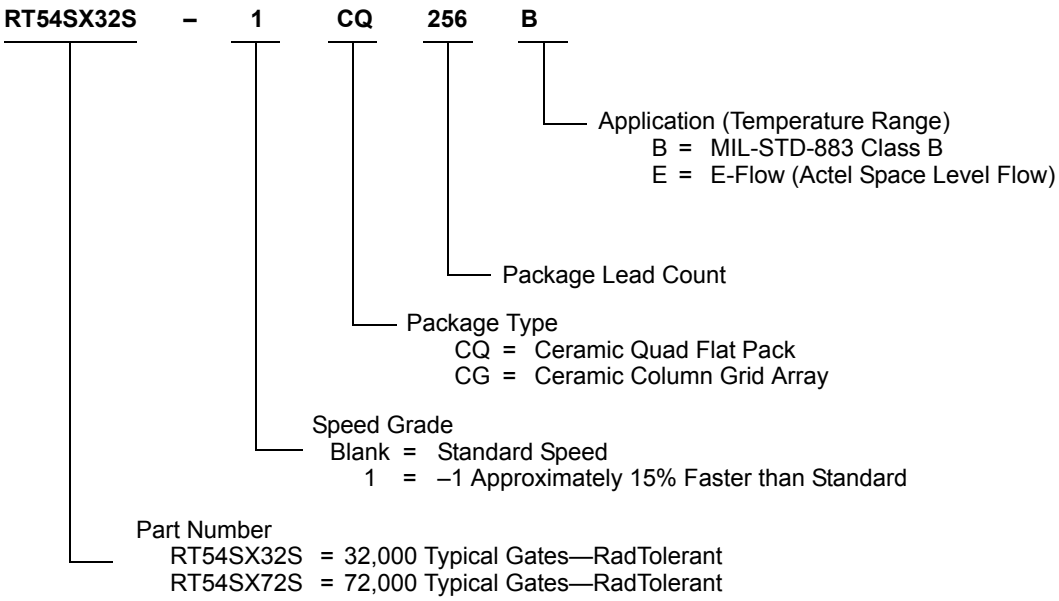
- 48,000 to 108,000 Available System Gates
- Up to 227 User-Programmable I/O Pins (package dependent)

RT54SX-S Product Profile

Device	RT54SX32S	RT54SX72S
Capacity		
Typical Gates	32,000	72,000
System Gates	48,000	108,000
Logic Modules	2,880	6,036
Combinatorial Cells	1,800	4,024
SEU Hardened Register Cells (Dedicated Flip-Flops)	1,080	2,012
Maximum Flip-Flops	1,980	4,024
Maximum User I/Os	227	212
Clocks	3	3
Quadrant Clocks	0	4
Clock-to-Out Delay	8.7 ns	11.0 ns
Input Set-Up Time (External)	–1.3 ns	–3.3 ns
Speed Grades	Std, –1	Std, –1
Package (by pin count)		
CQFP	208, 256	208, 256
CCGA		624

**See Actel's website for the latest version of the datasheet. This datasheet is web-only.*

Ordering Information



Product Plan

	Speed Grade		Application	
	Std	–1*	B	E
RT54SX32S Devices				
208-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
RT54SX72S Devices				
208-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔
256-Pin Ceramic Column Grid Array (CCGA)	✔	✔	P	P

Contact your Actel sales representative for product availability.

Applications: B = MIL-STD-883 Class B
E = E-flow (Actel Space Level Flow)
*✔ = Available * Approximately 15% Faster than Standard*
P = Planned

Ceramic Device Resources

Device	User I/Os (including clock buffers)		
	CQFP 208-Pin	CQFP 256-Pin	CCGA 624-Pin
RT54SX32S	173	227	–
RT54SX72S	170	212	TBD

Radiation Survivability

The RadTolerant SX-S devices have varying total dose radiation survivability. The ability of these devices to survive radiation effects is both device and lot dependent. The user must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

Total dose results are summarized in two ways. The first summary is indicated by the maximum total dose level achieved before the device fails to meet an individual performance specification, but remains functional. For Actel FPGAs, the parameter that first exceeds the specification is I_{CC} (standby supply current). The second summary is indicated by the maximum total dose achieved prior to the functional failure of the device.

Actel provides total dose radiation test data on each lot offered for sale. Reports are available on our website or from Actel's local sales representatives. Listings of available lots and devices can also be provided.

For a radiation performance summary, see *Radiation Performance of Actel Products* at http://www.actel.com/hirel. This summary also shows single event upset (SEU) and single event latch-up (SEL) testing that has been performed on Actel FPGAs.

All radiation performance information is provided for information purposes only and is not guaranteed. Total dose effects are lot-dependent, and Actel does not guarantee that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors including, but not limited to, characteristics of the orbit, radiation environment, proximity to the satellite exterior, the amount of inherent shielding from other sources within the satellite and actual bare die variations. For these reasons, it is solely the responsibility of the user to determine whether the device will meet the requirements of the specific design.

QML Certification

Actel has achieved full QML certification demonstrating that quality management procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military, and space applications.

Many suppliers of microelectronic components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for high quality, reliable, and cost-effective logistics support throughout QML products' life cycles.

RT54SX-S – A New Design for Space Applications

The architecture of the RT54SX-S devices is an enhanced version of Actel's SX-A device architecture. For more information about the SX-A device architecture, see the "Background on the Family Architecture" section on page 5.

Featuring SEU hardened D flip-flops that offer the benefits of Triple Module Redundancy (TMR), the RT54SX-S family is a unique product offering for space applications. The RT54SX-S devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility in Japan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

SEU Hardened DFF Description

In order to meet the stringent SEU requirements of a LET th greater than 40MeV-gm/cm^2, the internal design of the R-cell was modified without changing the functionality of the cell. Figure 1 shows basic R-cell functionality.

Figure 2 illustrates a simplified representation of how the D flip-flop in the R-cell is implemented in the SX-A architecture. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output to the input stage. The potential problem in a space environment is that either of the latches can change state when hit by a particle with enough energy.

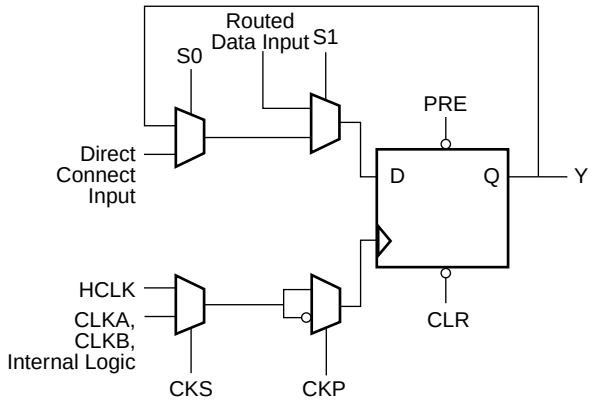


Figure 1 • *R-Cell Functional Diagram*

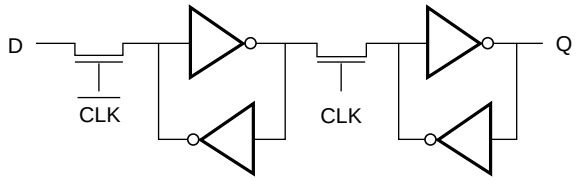


Figure 2 • *SX-A R-Cell Implementation of D Flip-Flop*

To achieve the SEU requirements, the D flip-flop in the RT54SX-S R-cell is enhanced (Figure 3). Both the master and slave "latches" are actually implemented with three latches. The feedback path of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch.

Figure 4 is a simplified schematic of the test circuitry that has been added to test the functionality of all the components of the flip-flop. The inputs to each of the three latches are independently controllable so the voting circuitry in the feedback paths can be exhaustively tested. This testing is performed on an unprogrammed array during wafer sort, final test and post burn-in test. This test circuitry cannot be used to test the flip-flops once the device has been programmed.

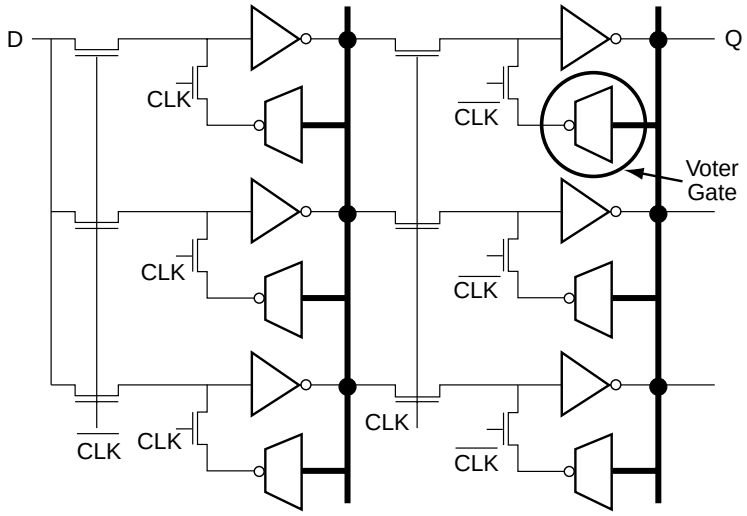


Figure 3 • *RT54SX-S R-Cell Implementation of D Flip-Flop Using Voter Gate Logic*

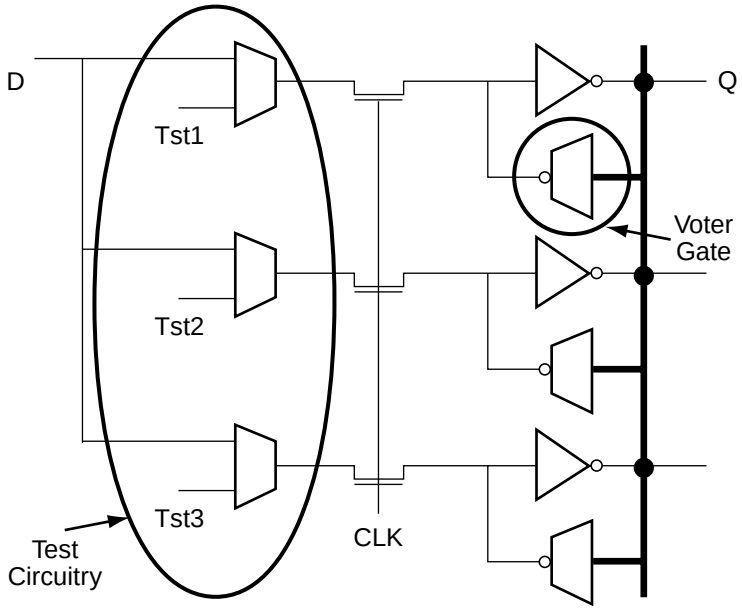


Figure 4 • *R-Cell Implementation— Test Circuitry*

Background on the Family Architecture

The RT54SX-S architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of high reliability applications.

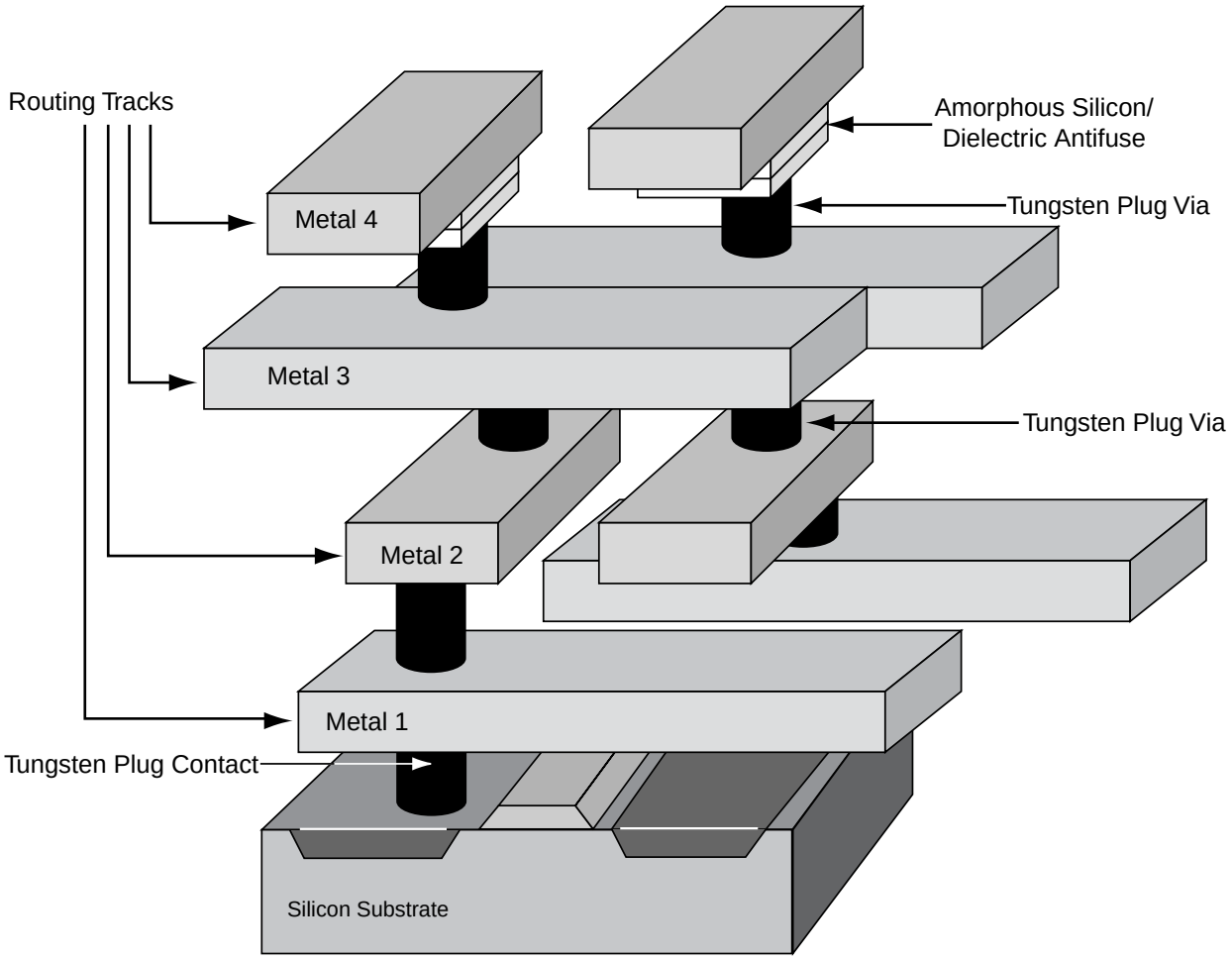
Programmable Interconnect Element

The RT54SX-S family incorporates up to three layers of metal interconnect (four metal layers in RT54SX72S) and provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers (Figure 5). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the RT54SX-S family abundant routing resources and provides excellent protection against design theft. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. Additionally, since RT54SX-S is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

The RT54SX-S interconnect (i.e., the antifuses and metal tracks) also has lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry for the radiation tolerance offered.



Note: RT54SX72S has four layers of metal with the antifuse between Metal 3 and Metal 4. RT4SX32S has three layers of metal with antifuse between Metal 2 and Metal 3.

Figure 5 • *RT54SX-S Family Interconnect Elements*

Logic Module Design

The RT54SX-S family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's RT54SX-S family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1 on page 3). The R-cell registers feature programmable clock polarity, selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the RT54SX-S FPGA. The clock source for the R-cell can be chosen from the hard-wired clock, the routed clocks, or the internal logic.

The C-cell implements a range of combinatorial functions up to 5 inputs (Figure 6). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options (as in previous architectures) to more than 4,000 in the RT54SX-S architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

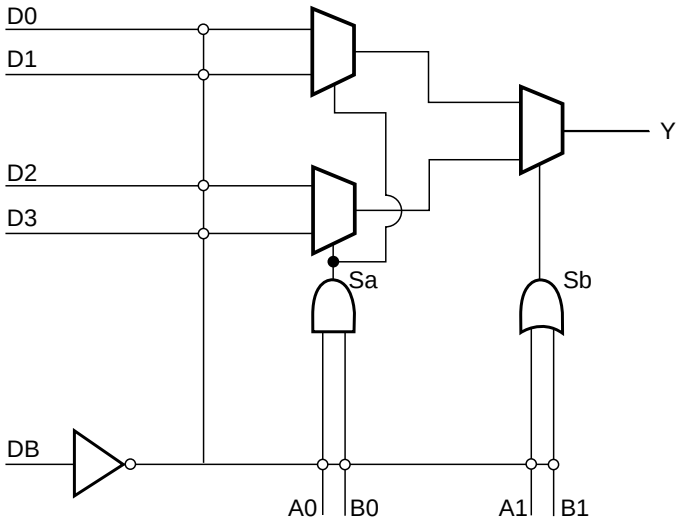


Figure 6 • C-Cell

Chip Architecture

The RT54SX-S family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters (Figure 7 on page 7). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. RT54SX-S devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 8 on page 7 and Figure 9 on page 8). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1ns.

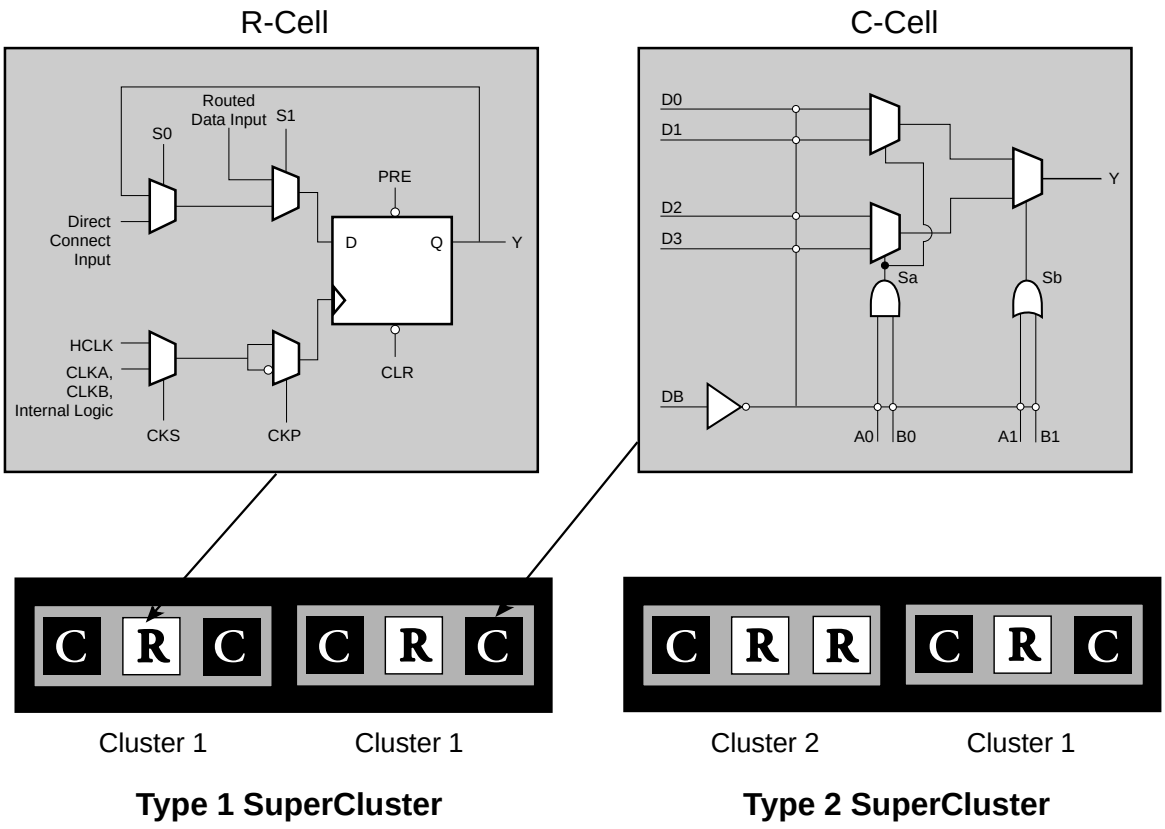


Figure 7 • *Cluster Organization*

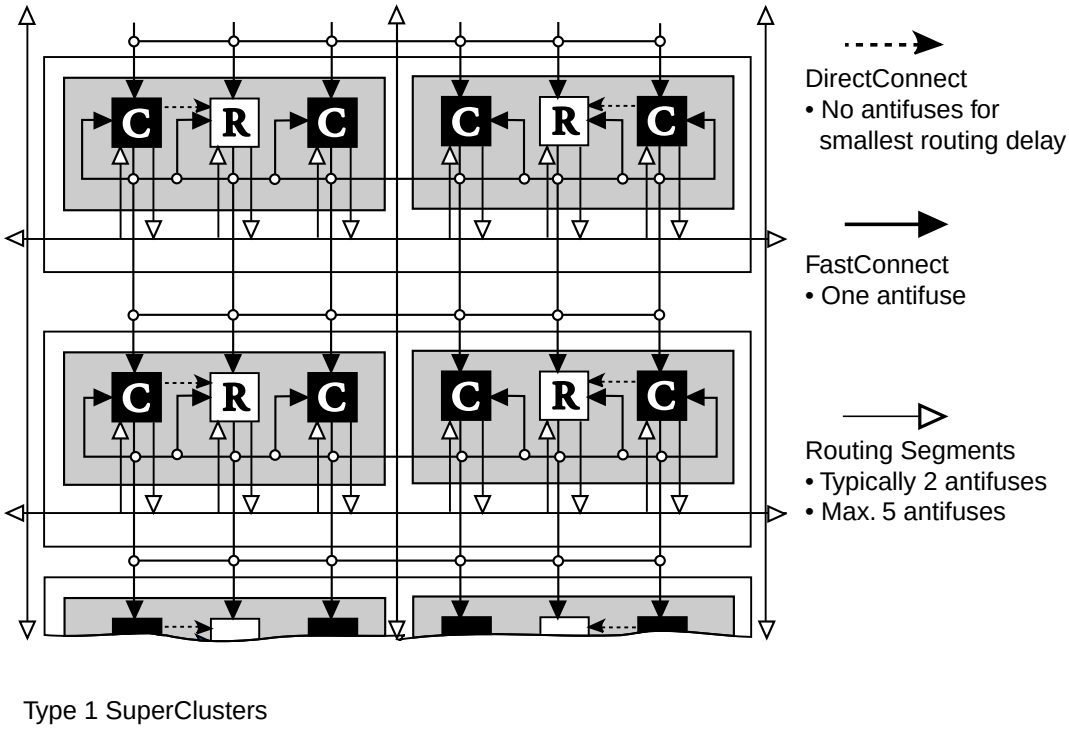


Figure 8 • *DirectConnect and FastConnect for Type 1 SuperClusters*

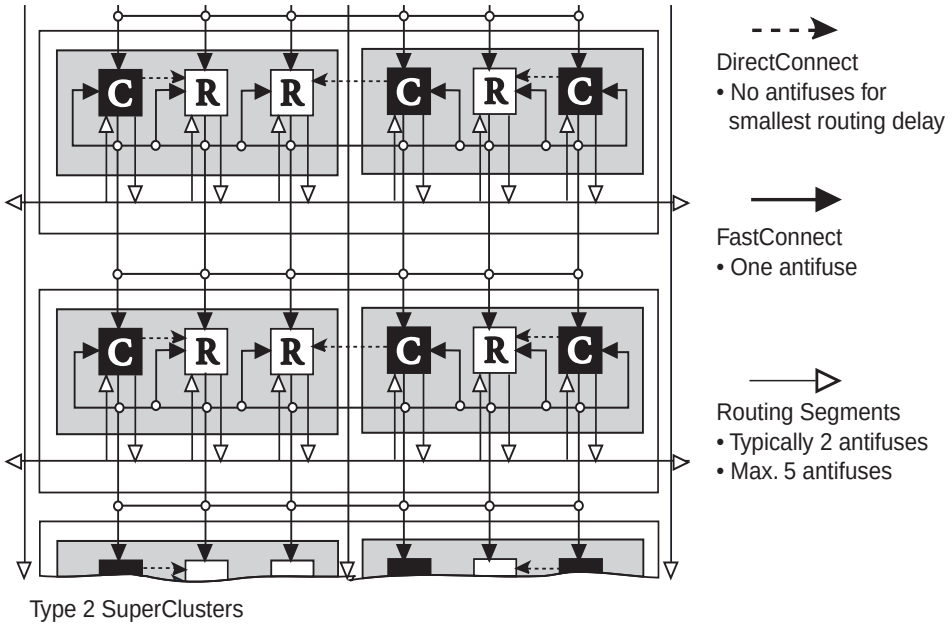


Figure 9 • *DirectConnect and FastConnect for Type 2 SuperClusters*

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum interconnect propagation delay of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 8.7 ns clock-to-out (pad-to-pad) performance of the RT54SX-S devices. The hard-wired clock is tuned to provide clock skew of less than 0.3 ns worst case. If not used, this pin must be set as LOW or HIGH on the board. It must not be left floating. Figure 10 shows the clock circuit used for the constant load HCLK.

Table 1 • *RT54SX-S Clock Resources*

	RT54SX32S	RT54SX72S
Routed Clocks (CLKA, CLKB)	2	2
Hardwired Clocks (HCLK)	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	4

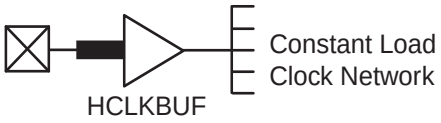


Figure 10 • *RT54SX-S HCLK Clock Pad*

The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the RT54SX-S device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, then these pins must be set as LOW or HIGH on the board. They must not be left floating (except in HiRel A54SX72A, where these clocks can be configured as regular I/Os). Figure 11 on page 9 describes the CLKA and CLKB circuit used in RT54SX32S where these clocks can be used as I/Os.

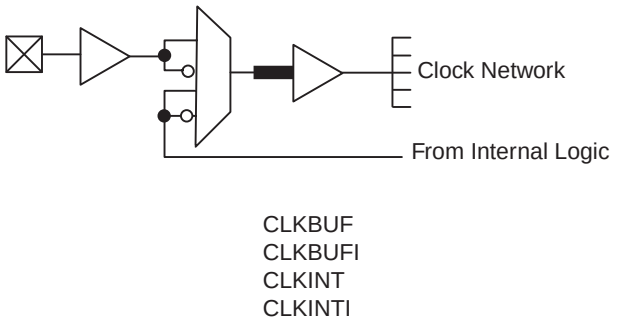


Figure 11 • RT54SX-S Routed Clock Structure (excluding RT54SX72S)

In addition, the RT54SX72S device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. If QCLKs are not used as quadrant clocks, they will behave as regular I/Os. The CLKA, CLKB, and QCLK circuits for RT54SX72S are shown in Figure 12. For more information, refer to the "Pin Description" section on page 35.

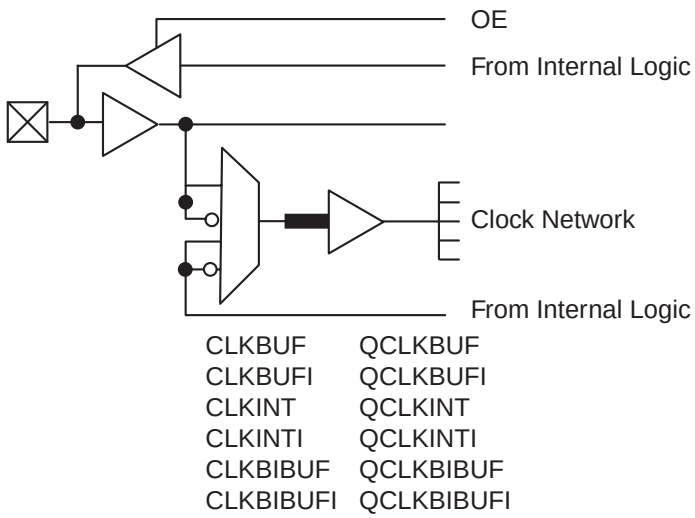


Figure 12 • RT54SX72S Routed Clock and QClock Structure

Other Architectural Features

Technology

Actel's RT54SX-S family is implemented in high-voltage twin-well CMOS using 0.25µm design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals, and has a programmed ("on" state) resistance of 25Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables RT54SX-S devices to operate with internal clock frequencies up to 310 MHz, enabling very fast execution of even complex logic functions. Thus, the RT54SX-S family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an RT54SX-S device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

I/O Modules

Each I/O on a RT54SX-S device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards are allowed and can be set on an individual basis. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-output-pad timing as fast as 8.7 ns. In most FPGAs, I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in RT54SX-S FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn, enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by Designer software. Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O to a known state during power up. Just slightly before V_{CCA} reaches 2.5V, the resistors are disabled, so the I/Os will behave normally. For more information about the power-up resistors, please see Actel's application note

SX-A and RT54SX-S Devices in Hot-Swap and Cold Sparing Applications. See Table 2 and Table 3 for more information concerning I/O features.

RT54SX-S inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the RT54SX-S I/O may create a voltage divider. This voltage divider could pull the input voltage below spec for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5V to provide the logic '1' input, and V_{CCI} is set to 3.3V on the RT54SX-S device, the input signal may be pulled down by the RT54SX-S input.

Hot Swapping

RT54SX-S I/Os can be configured to be hot swappable in compliance with Compact PCI Specification. However, a 3.3V PCI device is not hot swappable. During power up/down, all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down. After the RT54SX-S device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for a RT54SX-S device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V. Refer to Actel's application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications* for more information on hot swapping.

Table 2 • I/O Features

Function	Description
Input Buffer Threshold Selections	• 5V: CMOS, PCI,TTL • 3.3V: PCI, LVTTL
Flexible Output Driver	• 5V: CMOS, PCI,TTL • 3.3V: PCI, LVTTL
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current (Power supplies are at 0V) • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable slew rate, high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. No slew is changed on the rising edge of the output or any inputs.
Power Up	Individually selectable pull-ups and pull-downs during power up (default is to power up in tristate) Enables deterministic power up of device V_{CCA} and V_{CCI} can be powered in any order

Table 3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-up Resistor Pull
TTL, LVTTL	Yes	Yes. Affects falling edge outputs only	Pull up or Pull down
3.3V PCI	No	No. High slew rate only	Pull up or pull down
5V PCI	Yes	No. High slew rate only	Pull up or pull down

Table 4 • Power-up Time at which I/Os Become Active

Ramp Rate	0.25V/µs	0.025V/µs	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
RT54SX32S	10	100	0.46	0.74	2.8	5.2	12.1	47.2
RT54SX72S	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Power Requirements

The RT54SX-S family supports either 3.3V or 5V I/O voltage operation and is designed to tolerate 5V inputs in each case (Table 5). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-powered architecture on the market.

Table 5 • *Supply Voltages*

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
RT54SX-S	2.5V	3.3V	5V*	3.3V
	2.5V	5V	5V	5V

Note: **3.3V PCI is not 5V tolerant.*

Boundary Scan Testing (BST)

All RT54SX-S devices are IEEE 1149.1 compliant. RT54SX-S devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible (Table 6). TRST and TMS cannot be employed as user I/Os in either mode.

Table 6 • *Boundary Scan Pin Functionality*

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10 kΩ on TMS

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; users cannot utilize them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To enter Dedicated mode, users need to reserve the JTAG pins in Actel Designer software. To reserve the JTAG pins, users can check the "Reserve JTAG" box in the "Device Selection Wizard" in Designer (Figure 13).

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/O or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

Figure 13 • *Device Selection Wizard*

To enter the Flexible mode, users need to un-check the "Reserve JTAG" box in the "Device Selection Wizard" in Designer. In Flexible mode, TDI, TCK and TDO pins may function as user I/O or BST pins. The functionality is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/O. The TDI, TCK, and TDO are transformed from user I/O into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to the Test-Logic Reset state, in the absences of TRST assertion, TMS must be high for at least five TCK cycles. An external 10 kΩ pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it HIGH by default.

Table 7 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 7 • *Boundary Scan Pin Configurations and Functionalities*

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Un-Checked	Test-Logic-Reset
Flexible (JTAG)	Un-Checked	Other

TRST Pin

TRST pin functions as a Dedicated Boundary Scan Reset pin. An internal pull-up resistor is permanently enabled on the TRST pin. Additionally, the TRST pin must be grounded for flight applications. This will prevent Single Event Upsets (SEU) in the TAP controller from inadvertently placing the device into JTAG mode.

Probing Capabilities

RT54SX-S devices also provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer Diagnostic Hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be

performed. Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When selecting the "Reserve Probe" box as shown in Figure 13 on page 11, the user direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This "reserve" option is merely a guideline. If the Layout tool requires that the PRA and PRB pins to be user I/Os to achieve successful layout, then the tool will employ these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the "Reserve Probe" option, Designer Layout will override the "Reserve Probe" option and place your user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 8 summarizes the possible device configurations for probing.

Table 8 • *Device Configuration Options for Probe Capability*

JTAG Mode	TRST	Security Fuse Programmed	PRA, PRB, TDO[1]	TDI and TCK[1]
Dedicated	LOW	No	User I/O[2]	Probing Unavailable
Flexible	LOW	No	User I/O[2]	User I/O[2]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports during probing. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

Development Tool Support

RT54SX-S devices are fully supported by Actel's line of FPGA development tools, including Actel's Designer software and Actel Libero Integrated Design Environment (IDE), the FPGA design tool suite. Designer Software, Actel's suite of FPGA development tools for PCs and Workstations, includes the ACTgen Macro Builder, timing driven place-and-route, timing analysis tools, and fuse file generation. Libero IDE is a design management environment that integrates the needed design tools, streamlines the design flow, manages all design and log files, and passes necessary design data between tools. Libero IDE includes, Synplify, ViewDraw, Actel's Designer Software, ModelSim HDL Simulator, WaveFormer Lite, and Actel's Silicon Explorer II.

RT54SX-S Probe Circuit Control Pins

The RT54SX-S RadTolerant devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 14 on page 13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit. Actel recommends that you use a series 70 Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

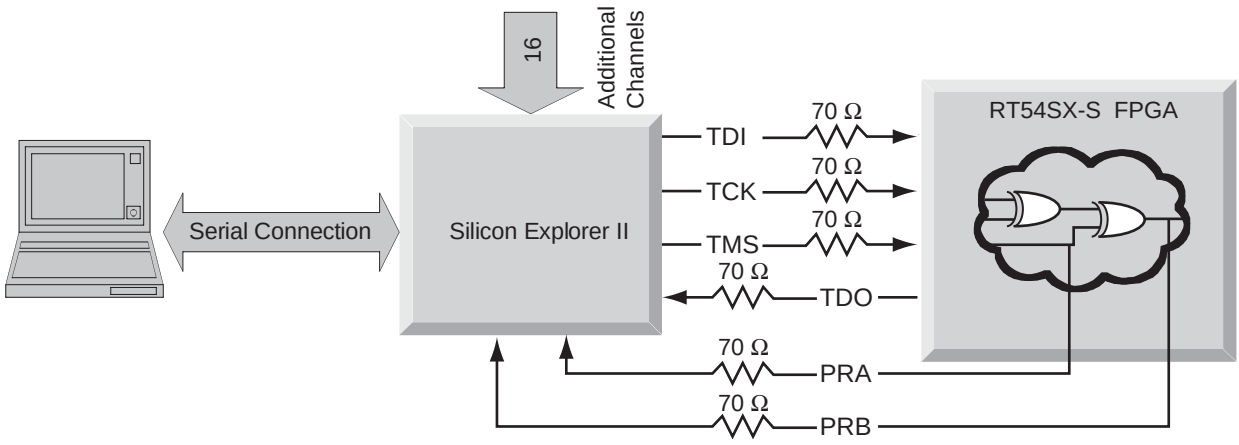


Figure 14 • Probe Setup

2.5V/3.3V/5V Operating Conditions

Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to + 6.0	V
V_O	Output Voltage	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Military	Units
Temperature Range*	–55 to +125	°C
2.5V Power Supply Tolerance	2.25 to 2.75	V
3.3V Power Supply Tolerance	3.0 to 3.6	V
5V Power Supply Tolerance	4.5 to 5.5	V

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

3.3V LVTTL and 5V TTL Electrical Specifications

Symbol	Parameter		Military Min.	Military Max.	Units
V_{OH}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -1mA)	0.9 V_{CCI}		V
	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -8mA)	2.4		V
V_{OL}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1mA)		0.1 V_{CCI}	V
	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12mA)		0.4	V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–20	20	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–20	20	µA
t_R, t_F	Input Transition Time			10	ns
C_{IO}	I/O Capacitance			10	pF
I_{CC}[1]	Standby Current			25	mA
IV Curve[2]	Can be derived from the IBIS model on the web.				

Notes:

1. *Individual device data is available in the www.actel.com/guru.*
2. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

5V CMOS Electrical Specifications

Symbol	Parameter		Military Min.	Military Max.	Units
V_{OH}	V_{CCI} = MIN, $V_I = V_{CCI}$ or GND	(I_{OH} = –20µA)	V_{CCI} - 0.1		V
V_{OL}	V_{CCI} = MIN, $V_I = V_{CCI}$ or GND	(I_{OL}= ±20µA)		0.1	V
V_{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$			0.3V_{CC}	V
V_{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		0.7V_{CC}		V
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–20	20	µA
t_R, t_F	Input Transition Time			10	ns
C_{IO}	I/O Capacitance			10	pF
I_{CC}[1]	Standby Current			25	mA
IV Curve[2]	Can be derived from the IBIS model on the web.				

Notes:

1. *Individual device data is available in the www.actel.com/guru.*
2. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

5V PCI Compliance for the RT54SX-S Family

The RT54SX-S family supports 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5V PCI Operation)

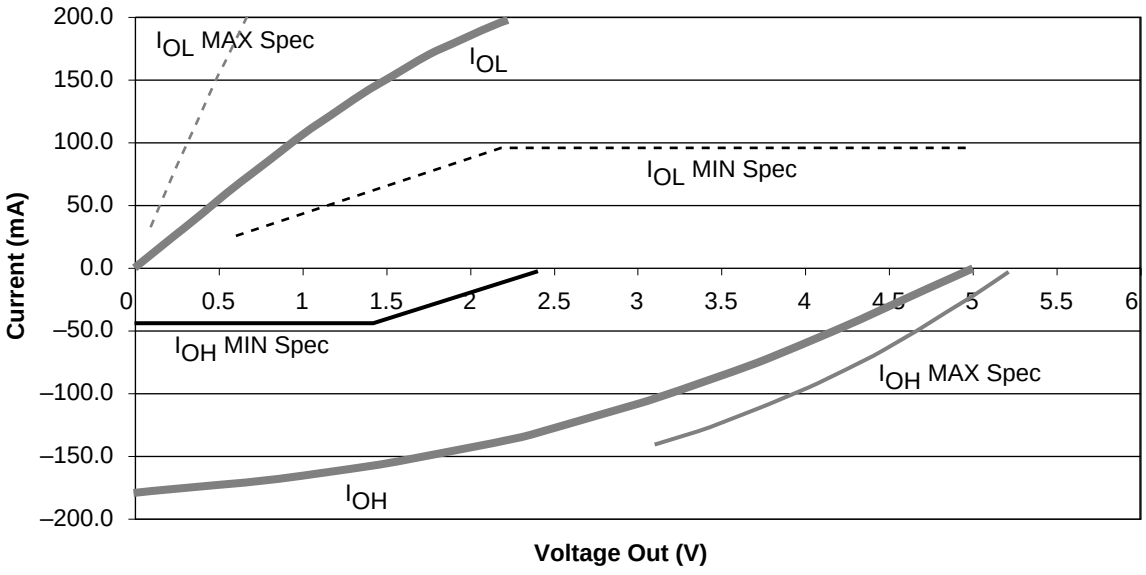
Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		4.5	5.5	V
V_{IH}	Input High Voltage[1]		2.0	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.).*

Figure 15 shows the 5V PCI V/I curve and the minimum and maximum PCI drive characteristics of the RT54SX-S family.

Figure 15 • *5V PCI Curve for RT54SX-S Family*



Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CCI} > V_{OUT} > 3.1V$$

Equation B

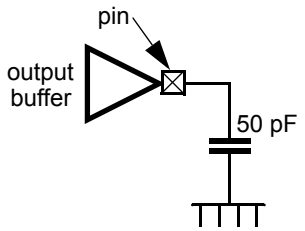
$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

AC Specifications (5V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]		Equation A on page 15	
	(Test Point)	$V_{OUT} = 3.1$ [3]		–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95		mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ [1, 3]		Equation B on page 15	
	(Test Point)	$V_{OUT} = 0.71$		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load[4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load[4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 15 on page 15. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification is not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective curves in Figure 15 on page 15. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both the maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



3.3V PCI Compliance for the RT54SX-S Family

The RT54SX-S family supports 3.3V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}/I_{IH}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$		±10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input V_{IN}.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean in general that components for expansion boards would need to use alternatives to ceramic PGA packaging.*

Figure 16 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the RT54SX-S family.

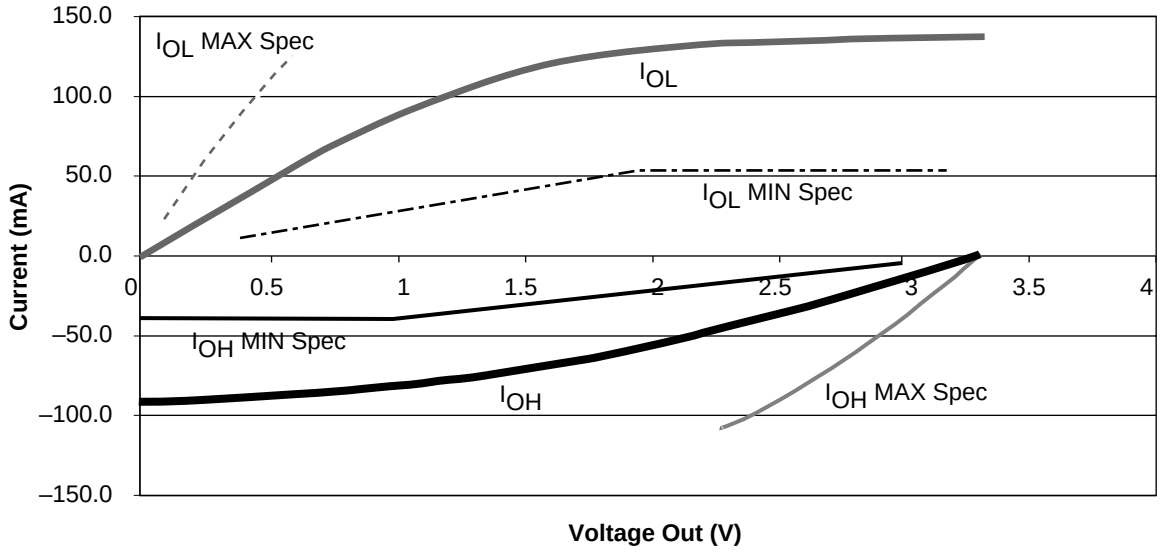


Figure 16 • 3.3V PCI Curve for RT54SX-S Family

Equation C

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } V_{CCI} > V_{OUT} > 0.7\ V_{CCI}$$

Equation D

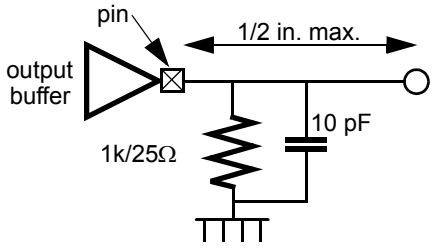
$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

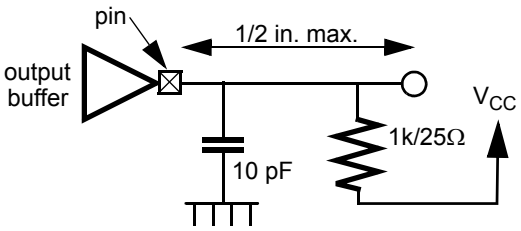
AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation C on page 17	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation D on page 17	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load[3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load[3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 16 on page 17. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification is not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective curves in Figure 16 on page 17. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*





Actel MIL-STD-883 Class B Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D or E, Y_1, Orientation Only	100%
4.	Particle Impact Noise Detection	2020, Condition A	100%
5.	Seal a. Fine b. Gross	1014	 100% 100%
6.	Visual Inspection	2009	100%
7.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
8.	Dynamic Burn-In	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
9.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
10.	Percent Defective Allowable	5%	All Lots
11.	Final Electrical Test	In accordance with applicable Actel device specification, which includes a, b, and c:	
	a. Static Tests (1) 25°C (Subgroup 1, Table I) (2) –55°C and +125°C (Subgroups 2, 3, Table I)	 5005 5005	100%
	b. Functional Tests (1) 25°C (Subgroup 7, Table I) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I)	 5005 5005	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I)	 5005	100%
12.	External Visual	2009	100%

Actel Extended Flow[1]

Step	Screen	Method	Requirement
1.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
2.	Internal Visual	2010, Condition A	100%
3.	Serialization		100%
4.	Temperature Cycling	1010, Condition C	100%
5.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
6.	Particle Impact Noise Detection	2020, Condition A	100%
7.	Radiographic	2012 (one view only)	100%
8.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
9.	Dynamic Burn-In	1015, Condition D, 240 hours @ 125°C or 120 hours @150°C minimum	100%
10.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11.	Static Burn-In	1015, Condition C, 72 hours @ 150°C or 144 hours @ 125°C minimum	100%
12.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
14.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
15.	Seal	1014	100%
	a. Fine		
	b. Gross		
16.	External Visual	2009	100%

Notes:

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Actel is offering this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 4 below.*
2. *MIL-STD-883, Method 5004 requires a 100 percent Radiation latch-up testing to Method 1020. Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.*
3. *Method 5004 requires 100 percent nondestructive bond path to Method 2003. Actel substitutes a destructive bond path to Method 2011 Condition D on a sample basis only.*
4. *Wafer lot acceptance comply to commercial standards only (requirement per Method 5007 is not performed).*

Junction Temperature (T_J)

The temperature that is selected in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 1, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

Where:

T_a = Ambient Temperature

ΔT = Gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Estimating Power Consumption better calculation

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics section below.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. θ_{ja} thermal characteristics are shown with two different air flow rates.

The maximum junction temperature is 150°C.

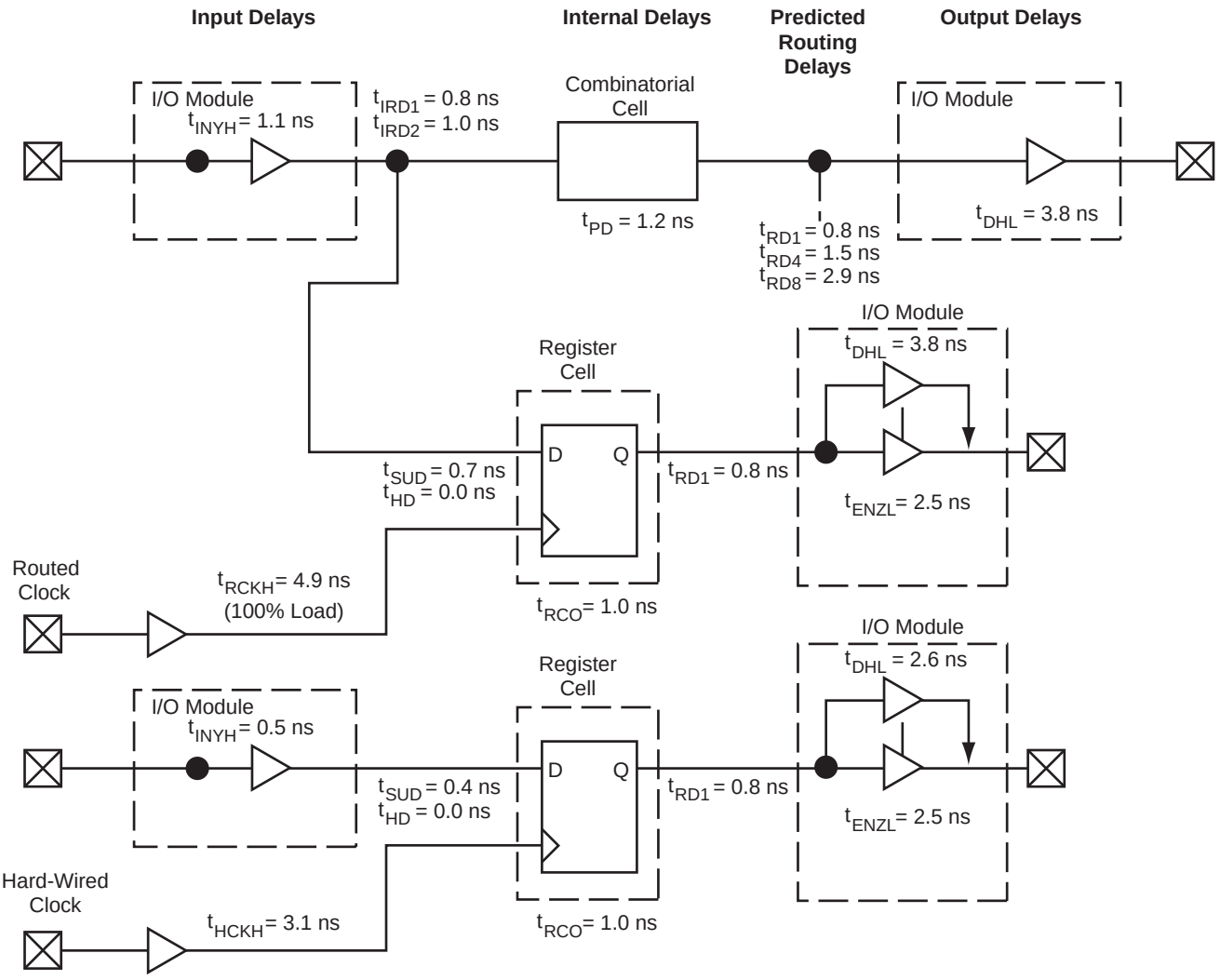
A sample calculation of the absolute maximum power dissipation allowed for a CQFP 208-pin package at military temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{22\text{°C/W}} = 1.14\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
RT54SX32S					
Ceramic Quad Flat Pack (CQFP)	208	6.3	22	14	°C/W
Ceramic Quad Flat Pack (CQFP)	256	6.2	20	10	°C/W
RT54SX72S					
Ceramic Quad Flat Pack (CQFP)	208	6.3	22	13	°C/W
Ceramic Quad Flat Pack (CQFP) with Heat Sink	256	6.2	19	9	°C/W
Ceramic Column Grid Array (CCGA)	624	TBD	TBD	TBD	TBD

For Power Estimator information, please go to http://www.actel.com/products/tools/index.html.

RT54SX-S Timing Model



Values shown for RT54SX32S, –1, 5V TTL worst-case military conditions.

Hard-Wired Clock

External Setup = $(t_{INYH} + t_{IRD2} + t_{SUD}) - t_{HCKH}$
= 1.1 + 1.0 + 0.7 – 3.1 = –0.3ns

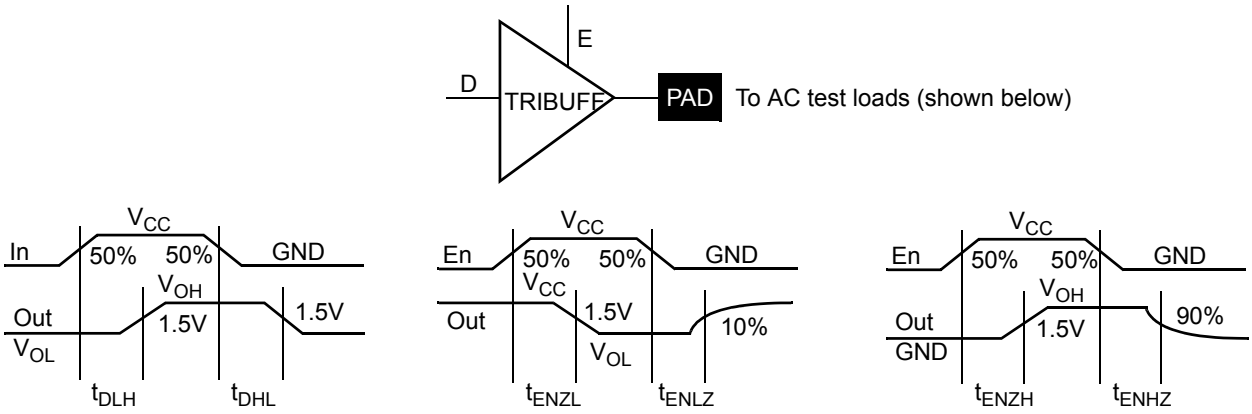
Clock-to-Out (Pad-to-Pad)
= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 3.1 + 1.0 + 0.8 + 3.8= 8.7 ns

Routed Clock

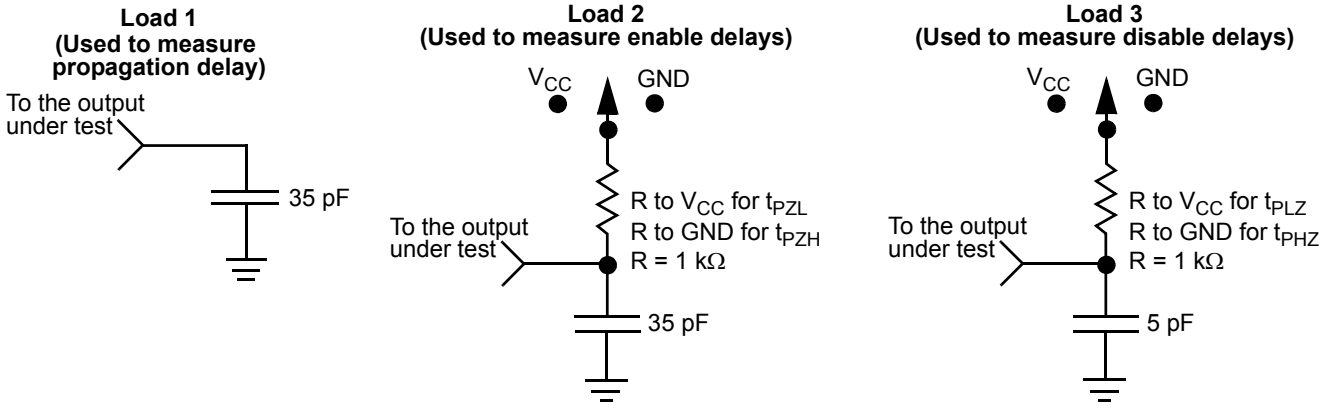
External Setup = $(t_{INYH} + t_{IRD2} + t_{SUD}) - t_{RCKH}$
= 1.1 + 1.0 + 0.7– 4.9= –2.1 ns

Clock-to-Out (Pad-to-Pad)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 4.9+ 1.0 + 0.8 + 3.8 = 10.5 ns

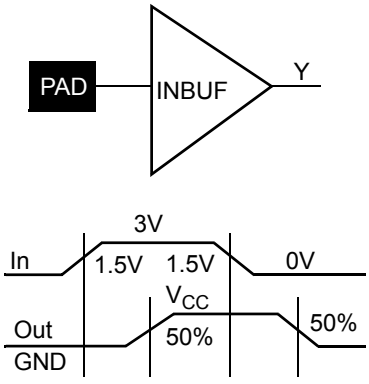
Output Buffer Delays



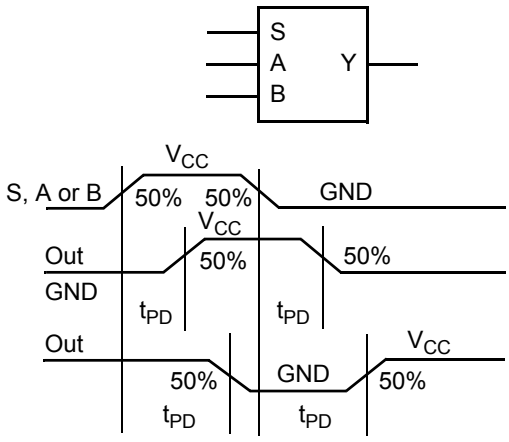
AC Test Loads



Input Buffer Delays

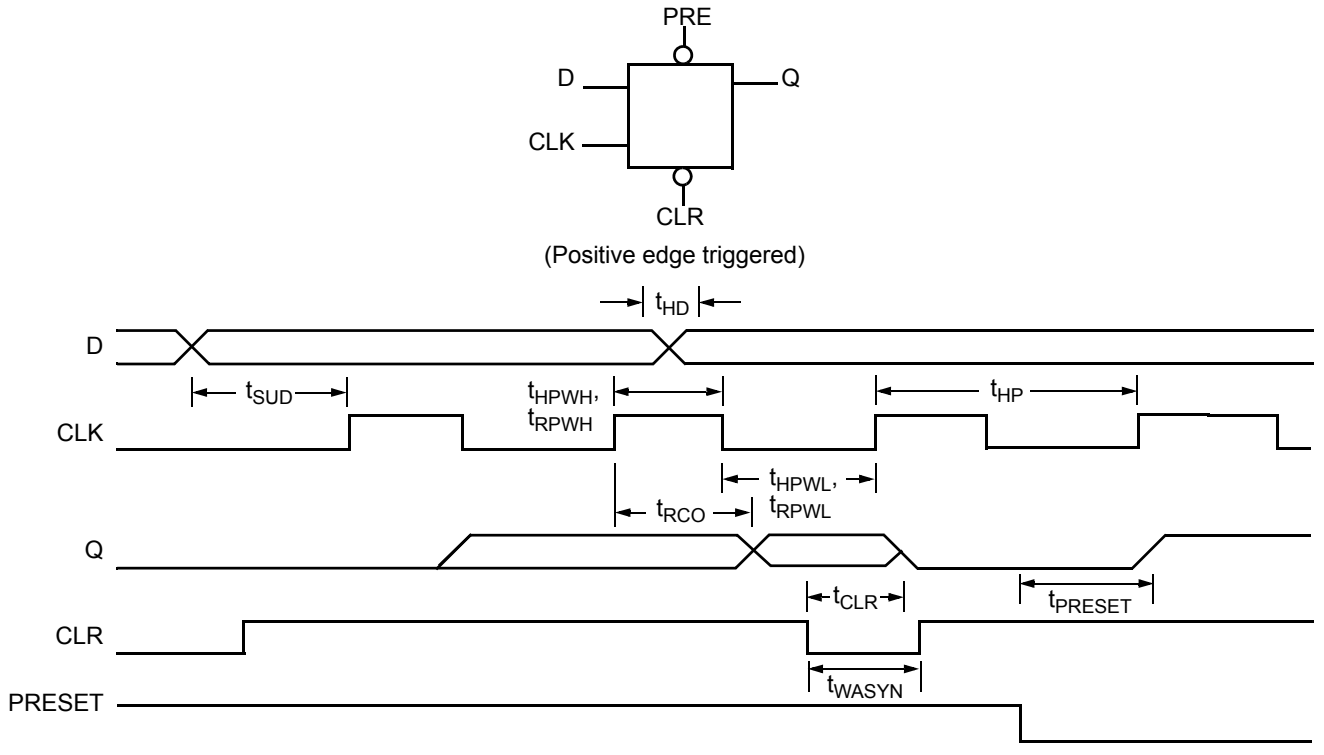


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

RT54SX-S device timing characteristics are in three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all RT54SX-S devices. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays in the data sheet specifications section.

Timing Derating

RT54SX-S devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Military, T_J = 125°C, V_{CCA} = 2.3V)

V_{CCA}	Junction Temperature (T_J)						
	–55	–40	0	25	70	85	125
2.3	0.68	0.69	0.75	0.77	0.86	0.90	1.00
2.5	0.64	0.65	0.70	0.72	0.81	0.84	0.93
2.7	0.60	0.61	0.66	0.68	0.76	0.79	0.88

RT54SX32S Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.2		1.4	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.4		0.4	ns
t_{RD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{RD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{RD12}	FO=12 Routing Delay		4.0		4.7	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.1	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		2.2		ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V PCI		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V PCI		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V LVTTL		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V LVTTL		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V PCI		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V PCI		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V TTL		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V TTL		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V CMOS		1.4		1.7	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V CMOS		1.3		1.5	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{IRD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{IRD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{IRD12}	FO=12 Routing Delay		4.0		4.7	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		4.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.1		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.5		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		5.0		ns
f_{HMAX}	Maximum Frequency		238		200	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.2		3.7	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.2		3.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		4.0		4.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.8		4.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.9		5.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.8		4.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.0	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.0	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.0	ns

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.1		3.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.5		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		5.0		ns
f_{HMAX}	Maximum Frequency		238		200	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.7		4.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.8		4.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.9		5.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.8		4.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.3	ns

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.0		3.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		3.0	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.03		0.04	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.015		0.015	ns/pF
3.3V LVTTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.9		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		13.7		16.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.9		3.4	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		12.7		14.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.7		4.4	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.7		4.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.033		0.04	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.02		0.02	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW – low slew		0.067		0.073	ns/pF

Notes:

1. *Delays based on 10pF loading and 25 Ω resistance.*
2. *Delays based on 35pF loading.*

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.`**	**Units**
5V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.1		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.2		5.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.8		3.3	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.2		3.8	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.9		5.8	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.1		4.9	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.022	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.032		0.04	ns/pF
5V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		10.0		11.8	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.5		3.0	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.0		10.6	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.4	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.4		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.6		4.4	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.017		0.023	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.031		0.037	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW – low slew		0.06		0.07	ns/pF
5V CMOS Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.5		4.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		10.0		11.8	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.71	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		8.8		10.4	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.5		4.7	ns

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

RT54SX72S Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.2		1.4	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.4		0.4	ns
t_{RD1}	FO=1 Routing Delay		0.9		1.0	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.0	ns
t_{RD4}	FO=4 Routing Delay		1.9		2.3	ns
t_{RD8}	FO=8 Routing Delay		3.7		4.3	ns
t_{RD12}	FO=12 Routing Delay		5.1		6.0	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.1	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		2.2		ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V PCI		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V PCI		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V LVTTL		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V LVTTL		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V PCI		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V PCI		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V LVTTL		1.1		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V LVTTL		1.1		1.3	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5V CMOS		1.4		1.7	ns
t_{INYL}	Input Data Pad-to-Y LOW 5V CMOS		1.3		1.5	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{IRD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{IRD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{IRD12}	FO=12 Routing Delay		4.0		4.7	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		5.8		1.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		5.8		6.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.6		4.3		ns
t_{HPWL}	Minimum Pulse Width LOW	3.6		4.3		ns
t_{HCKSW}	Maximum Skew		1.4		1.6	ns
t_{HP}	Minimum Period	7.2		8.6		ns
f_{HMAX}	Maximum Frequency		139		116	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		5.9		6.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		5.9		6.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		7.4		8.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		9.1		10.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.7		6.8		ns
t_{RPWL}	Min. Pulse Width LOW	5.7		6.8		ns
t_{RCKSW}	Maximum Skew (Light Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		3.5		3.7	ns

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		5.3		6.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		5.3		6.1	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.6		4.3		ns
t_{HPWL}	Minimum Pulse Width LOW	3.6		4.3		ns
t_{HCKSW}	Maximum Skew		1.4		1.6	ns
t_{HP}	Minimum Period	7.2		8.6		ns
f_{HMAX}	Maximum Frequency		139		116	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		5.7		6.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		5.7		6.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		6.8		8.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		9.1		10.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.7		6.8		ns
t_{RPWL}	Min. Pulse Width LOW	5.7		6.8		ns
t_{RCKSW}	Maximum Skew (Light Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		3.5		3.7	ns

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.0		3.6	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		15.0		17.7	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.5	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.3		10.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		3.0	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.03		0.04	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.015		0.015	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW – low slew		0.065		0.075	ns/pF
3.3V LVTTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.9		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		13.7		16.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.9		3.4	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		12.7		14.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.7		4.4	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.7		4.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.033		0.04	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.02		0.02	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW – low slew		0.067		0.073	ns/pF

Notes:

1. *Delays based on 10pF loading and 25 Ω resistance.*
2. *Delays based on 35pF loading.*

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.`**	**Units**
5V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.1		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.2		5.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.8		3.3	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.2		3.8	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.9		5.8	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.1		4.9	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.022	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.032		0.04	ns/pF
5V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		10.0		11.8	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.5		3.0	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.0		10.6	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.4	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.4		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.6		4.4	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.017		0.023	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.031		0.037	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW – low slew		0.06		0.07	ns/pF
5V CMOS Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.5		4.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		10.0		11.8	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.71	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		8.8		10.4	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.5		4.7	ns

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For RT54SX72S, these clocks can be configured as user I/O).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only for RT54SX72S. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock it will behave as a regular I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output levels are compatible with standard TTL, LVTTL, 3.3V/5V PCI or 3.3V/5V CMOS specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O*, PRB, I/O* Probe A/B

The probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK*, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 6 on page 11). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI*, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 6 on page 11). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO*, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 6 on page 11). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TMS* Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 6 on page 11). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. For flight requirements, the TRST pin needs to be hard-wired to GND.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See Table 5 on page 11.

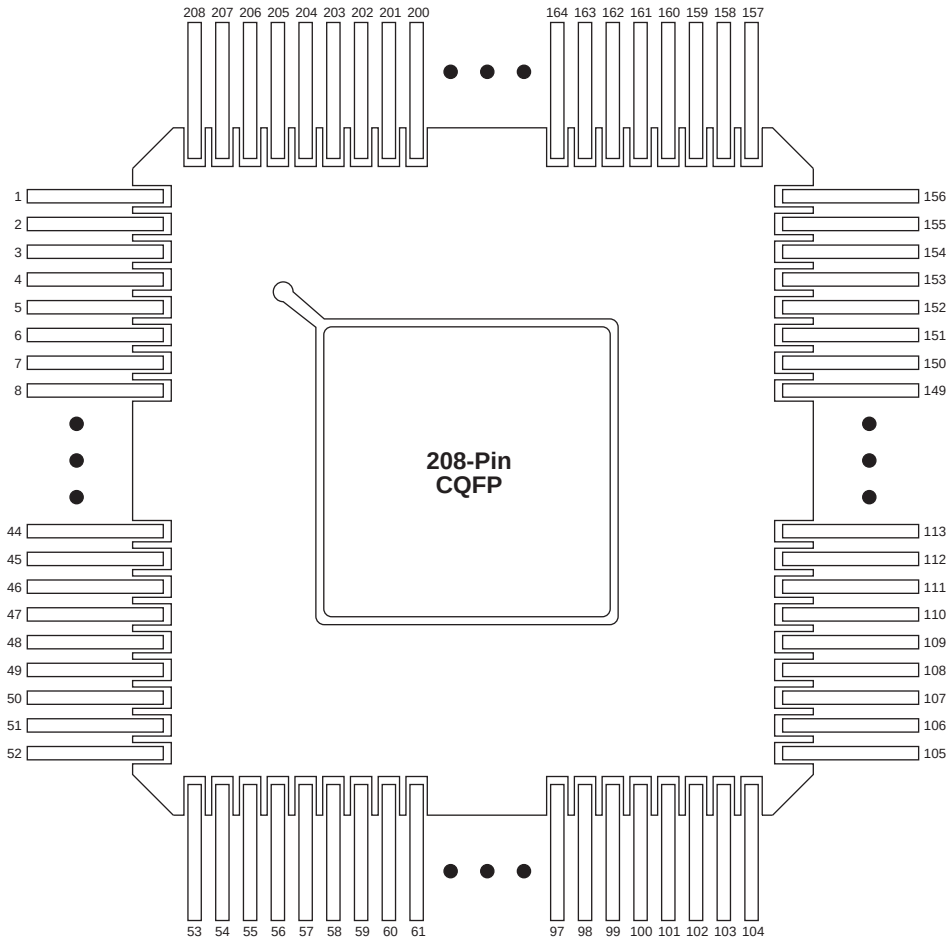
V_{CCA} Supply Voltage

Supply voltage for Array. See Table 5 on page 11.

** 70 Ω series termination should be placed on the board to enable probing capability.*

Package Pin Assignments

208-Pin CQFP (Top View)



208-Pin CQFP

Pin Number	RT54SX32S Function	RT54SX72S Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	V_{CCI}	V_{CCI}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	GND
19	I/O	V_{CCA}
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	NC	I/O
26	GND	GND
27	V_{CCA}	V_{CCA}
28	GND	GND
29	I/O	I/O
30	TRST	TRST
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	GND	GND
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	V_{CCI}	V_{CCI}
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	NC	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	QCLKA
75	I/O	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	V_{CCA}	V_{CCA}
79	GND	GND
80	NC	NC
81	I/O	I/O
82	HCLK	HCLK
83	I/O	V_{CCI}
84	I/O	QCLKB
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	V_{CCI}	V_{CCI}
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	TDO, I/O	TDO, I/O
104	I/O	I/O

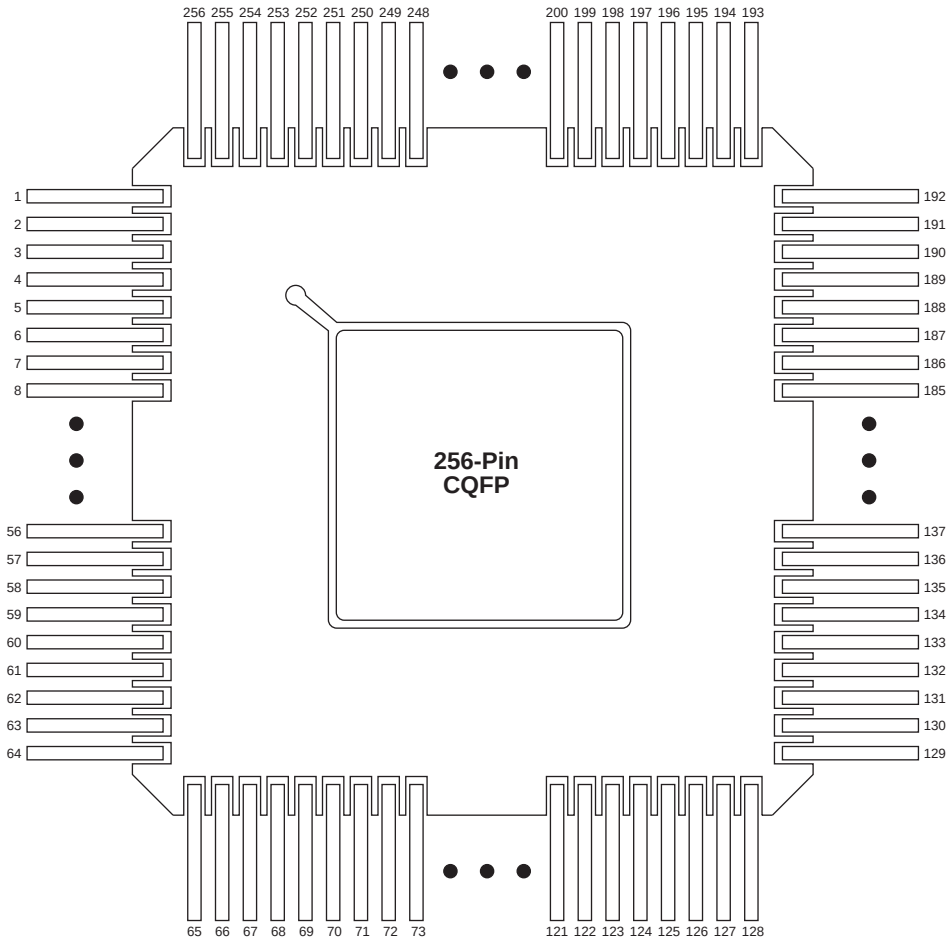
Note: *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

208-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
105	GND	GND
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	I/O	I/O
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}
116	I/O	GND
117	I/O	V_{CCA}
118	I/O	I/O
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	GND	GND
130	V_{CCA}	V_{CCA}
131	GND	GND
132	NC	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	I/O	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	V_{CCA}	V_{CCA}
146	GND	GND
147	I/O	I/O
148	V_{CCI}	V_{CCI}
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O
157	GND	GND
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	I/O	I/O
162	I/O	I/O
163	I/O	I/O
164	V_{CCI}	V_{CCI}
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	I/O	I/O
175	I/O	I/O
176	I/O	I/O
177	I/O	I/O
178	I/O	QCLKD
179	I/O	I/O
180	CLKA	CLKA
181	CLKB	CLKB
182	NC	NC
183	GND	GND
184	V_{CCA}	V_{CCA}
185	GND	GND
186	PRA, I/O	PRA, I/O
187	I/O	V_{CCI}
188	I/O	I/O
189	I/O	I/O
190	I/O	QCLKC
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	V_{CCI}	V_{CCI}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	RT54SX32S Function	RT54SX72S Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	V_{CCI}
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	V_{CCI}	V_{CCI}
29	GND	GND
30	V_{CCA}	V_{CCA}
31	GND	GND
32	I/O	I/O
33	I/O	I/O
34	TRST	TRST
35	I/O	I/O
36	I/O	V_{CCA}
37	I/O	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CCA}	V_{CCA}
47	I/O	V_{CCI}
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	GND
57	I/O	I/O
58	I/O	I/O
59	GND	GND
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	V_{CCI}
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	QCLKA
90	PRB, I/O	PRB, I/O
91	GND	GND
92	V_{CCI}	V_{CCI}
93	GND	GND
94	V_{CCA}	V_{CCA}
95	I/O	I/O
96	HCLK	HCLK
97	I/O	I/O
98	I/O	QCLKB
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O

256-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
105	I/O	I/O
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	GND	GND
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	I/O
120	I/O	V_{CCI}
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	TDO, I/O	TDO, I/O
127	I/O	I/O
128	GND	GND
129	I/O	I/O
130	I/O	I/O
131	I/O	I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	V_{CCA}	V_{CCA}
142	I/O	V_{CCI}
143	I/O	GND
144	I/O	V_{CCA}
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O

Pin Number	RT54SX32S Function	RT54SX72S Function
157	I/O	I/O
158	GND	GND
159	NC	NC
160	GND	GND
161	V_{CCI}	V_{CCI}
162	I/O	V_{CCA}
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CCA}	V_{CCA}
175	GND	GND
176	GND	GND
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	I/O
181	I/O	I/O
182	I/O	I/O
183	I/O	V_{CCI}
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	I/O	I/O
189	GND	GND
190	I/O	I/O
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	I/O	I/O
202	I/O	V_{CCI}
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	I/O	I/O

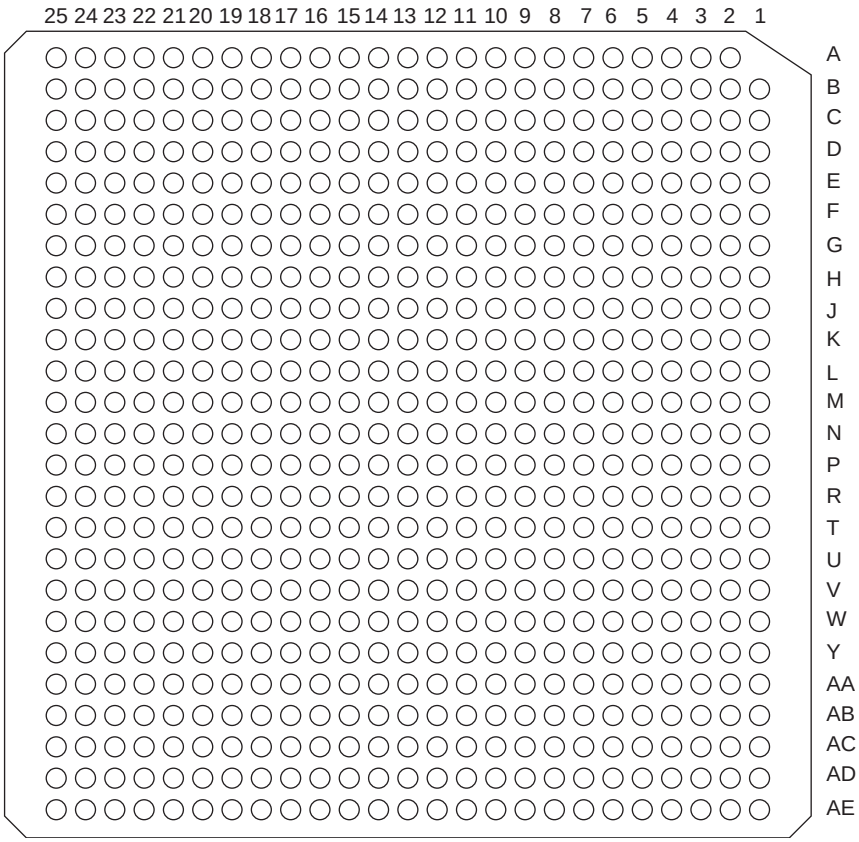
256-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
209	I/O	I/O
210	I/O	I/O
211	I/O	I/O
212	I/O	I/O
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O
216	I/O	I/O
217	I/O	I/O
218	I/O	QCLKD
219	CLKA	CLKA
220	CLKB	CLKB
221	V_{CCI}	V_{CCI}
222	GND	GND
223	NC	NC
224	GND	GND
225	PRA, I/O	PRA, I/O
226	I/O	I/O
227	I/O	I/O
228	I/O	V_{CCA}
229	I/O	I/O
230	I/O	I/O
231	I/O	QCLKC
232	I/O	I/O

Pin Number	RT54SX32S Function	RT54SX72S Function
233	I/O	I/O
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	GND
241	I/O	I/O
242	I/O	I/O
243	I/O	I/O
244	I/O	I/O
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	I/O
249	I/O	V_{CCI}
250	I/O	I/O
251	I/O	I/O
252	I/O	I/O
253	I/O	I/O
254	I/O	I/O
255	I/O	I/O
256	TCK, I/O	TCK, I/O

Package Pin Assignments

CG624 (Bottom View)



CG624-Pin

Pin Number	RT54SX72S Function
A2	NC
A3	NC
A4	NC
A5	I/O
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	NC
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	I/O
A22	NC
A23	NC
A24	NC
A25	NC
B1	NC
B2	GND
B3	GND
B4	V_{CCI}
B5	NC
B6	I/O
B7	I/O
B8	V_{CCI}
B9	NC
B10	I/O
B11	I/O
B12	I/O
B13	I/O
B14	CLKB
B15	I/O

CG624-Pin

Pin Number	RT54SX72S Function
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	NC
B23	V_{CCI}
B24	GND
B25	NC
C1	NC
C2	V_{CCI}
C3	GND
C4	PRB
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	QCLKC
C12	I/O
C13	PRA
C14	CLKA
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	I/O
C22	I/O
C23	GND
C24	V_{CCI}
C25	NC
D1	NC
D2	NC
D3	TDI
D4	GND

CG624-Pin

Pin Number	RT54SX72S Function
D5	PRA
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
D13	I/O
D14	QCLKD
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	V_{CCI}
D23	GND
D24	NC
D25	NC
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TCK
E6	I/O
E7	I/O
E8	I/O
E9	I/O
E10	I/O
E11	I/O
E12	V_{CCA}
E13	NC
E14	I/O
E15	I/O
E16	I/O
E17	I/O
E18	I/O

CG624-Pin

Pin Number	RT54SX72S Function
E19	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
E24	I/O
E25	I/O
F1	I/O
F2	V_{CCI}
F3	I/O
F4	I/O
F5	I/O
F6	NC
F7	NC
F8	I/O
F9	NC
F10	NC
F11	NC
F12	NC
F13	I/O
F14	I/O
F15	NC
F16	NC
F17	I/O
F18	I/O
F19	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
F24	I/O
F25	I/O
G1	I/O
G2	I/O
G3	TMS
G4	I/O
G5	I/O
G6	I/O
G7	V_{CCI}

CG624-Pin

Pin Number	RT54SX72S Function
G8	NC
G9	NC
G10	NC
G11	NC
G12	NC
G13	NC
G14	NC
G15	NC
G16	NC
G17	NC
G18	NC
G19	V_{CCI}
G20	I/O
G21	I/O
G22	I/O
G23	I/O
G24	I/O
G25	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	I/O
H6	I/O
H7	I/O
H8	V_{CCI}
H9	NC
H10	NC
H11	NC
H12	NC
H13	NC
H14	NC
H15	NC
H16	NC
H17	NC
H18	V_{CCI}
H19	I/O
H20	I/O
H21	I/O

CG624-Pin

Pin Number	RT54SX72S Function
H22	I/O
H23	I/O
H24	GND
H25	I/O
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	I/O
J7	NC
J8	NC
J9	V_{CCI}
J10	NC
J11	NC
J12	NC
J13	NC
J14	NC
J15	NC
J16	NC
J17	V_{CCI}
J18	NC
J19	NC
J20	I/O
J21	V_{CCA}
J22	I/O
J23	I/O
J24	I/O
J25	I/O
K1	I/O
K2	NC
K3	I/O
K4	I/O
K5	I/O
K6	NC
K7	NC
K8	NC
K9	NC
K10	GND

CG624-Pin

Pin Number	RT54SX72S Function
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	NC
K18	NC
K19	NC
K20	I/O
K21	I/O
K22	I/O
K23	I/O
K24	I/O
K25	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	NC
L8	NC
L9	NC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND
L17	NC
L18	NC
L19	NC
L20	I/O
L21	I/O
L22	I/O
L23	I/O
L24	I/O

CG624-Pin

Pin Number	RT54SX72S Function
L25	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	NC
M6	I/O
M7	NC
M8	NC
M9	NC
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	NC
M18	NC
M19	NC
M20	I/O
M21	NC
M22	I/O
M23	I/O
M24	NC
M25	I/O
N1	I/O
N2	I/O
N3	I/O
N4	I/O
N5	V_{CCA}
N6	I/O
N7	V_{CCA}
N8	NC
N9	NC
N10	GND
N11	GND
N12	GND
N13	GND

CG624-Pin

Pin Number	RT54SX72S Function
N14	GND
N15	GND
N16	GND
N17	NC
N18	NC
N19	V_{CCA}
N20	I/O
N21	V_{CCA}
N22	I/O
N23	I/O
N24	V_{CCI}
N25	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P5	I/O
P6	I/O
P7	NC
P8	NC
P9	NC
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	NC
P18	NC
P19	NC
P20	I/O
P21	NC
P22	I/O
P23	I/O
P24	I/O
P25	I/O
R1	I/O
R2	I/O

CG624-Pin

Pin Number	RT54SX72S Function
R3	I/O
R4	TRST
R5	I/O
R6	NC
R7	NC
R8	NC
R9	NC
R10	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	NC
R18	NC
R19	NC
R20	I/O
R21	I/O
R22	I/O
R23	I/O
R24	I/O
R25	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T5	I/O
T6	I/O
T7	I/O
T8	NC
T9	NC
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND

CG624-Pin

Pin Number	RT54SX72S Function
T17	NC
T18	NC
T19	NC
T20	NC
T21	I/O
T22	I/O
T23	I/O
T24	I/O
T25	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	I/O
U6	I/O
U7	I/O
U8	NC
U9	V_{CCI}
U10	NC
U11	NC
U12	NC
U13	NC
U14	NC
U15	NC
U16	NC
U17	V_{CCI}
U18	NC
U19	NC
U20	I/O
U21	I/O
U22	I/O
U23	I/O
U24	I/O
U25	I/O
V1	I/O
V2	I/O
V3	I/O
V4	V_{CCA}
V5	I/O

CG624-Pin

Pin Number	RT54SX72S Function
V6	I/O
V7	NC
V8	V_{CCI}
V9	NC
V10	NC
V11	NC
V12	NC
V13	NC
V14	NC
V15	NC
V16	NC
V17	NC
V18	V_{CCI}
V19	I/O
V20	I/O
V21	I/O
V22	V_{CCA}
V23	I/O
V24	I/O
V25	I/O
W1	I/O
W2	VCCI
W3	I/O
W4	I/O
W5	I/O
W6	I/O
W7	VCCI
W8	NC
W9	NC
W10	NC
W11	NC
W12	NC
W13	NC
W14	NC
W15	NC
W16	NC
W17	NC
W18	I/O
W19	VCCI

CG624-Pin

Pin Number	RT54SX72S Function
W20	I/O
W21	I/O
W22	I/O
W23	I/O
W24	I/O
W25	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	NC
Y12	NC
Y13	I/O
Y14	NC
Y15	NC
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	I/O
Y21	I/O
Y22	I/O
Y23	I/O
Y24	NC
Y25	I/O
AA1	NC
AA2	NC
AA3	I/O
AA4	I/O
AA5	GND
AA6	I/O
AA7	I/O
AA8	I/O

CG624-Pin

Pin Number	RT54SX72S Function
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O
AA13	V_{CCA}
AA14	NC
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	I/O
AA21	GND
AA22	I/O
AA23	I/O
AA24	I/O
AA25	NC
AB1	NC
AB2	V_{CCI}
AB3	I/O
AB4	GND
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	I/O
AB12	QCLKA
AB13	I/O
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	TDO
AB22	V_{CCI}

CG624-Pin

Pin Number	RT54SX72S Function
AB23	I/O
AB24	V_{CCI}
AB25	NC
AC1	NC
AC2	I/O
AC3	GND
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	I/O
AC10	I/O
AC11	I/O
AC12	PRB
AC13	I/O
AC14	HCLK
AC15	I/O
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	I/O
AC22	I/O
AC23	GND
AC24	I/O
AC25	NC
AD1	NC
AD2	GND
AD3	V_{CCI}
AD4	NC
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	I/O
AD10	V_{CCI}
AD11	I/O

CG624-Pin

Pin Number	RT54SX72S Function
AD12	I/O
AD13	I/O
AD14	I/O
AD15	I/O
AD16	NC
AD17	I/O
AD18	I/O
AD19	I/O
AD20	I/O
AD21	I/O
AD22	NC
AD23	V_{CCI}
AD24	GND
AD25	NC
AE1	NC
AE2	NC
AE3	NC
AE4	NC
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	I/O
AE11	I/O
AE12	I/O
AE13	I/O
AE14	QCLKB
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	NC
AE23	NC
AE24	NC
AE25	NC

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (Advanced v1.4)	Page
Advanced v1.3	On the PQ208 package for the RT54SX72S, pin 13, the function is I/O and not V_{CCI}.	page 37
Advanced v1.2.3	The "RT54SX-S Product Profile" table on page 1 table has been updated.	page 1
	The "Ceramic Device Resources" section on page 2	page 2
	The "Clock Resources" section on page 8 has been updated.	page 8
	Table 1 on page 8 is new.	page 8
	The "I/O Modules" section on page 9 and have been updated.	page 9
	Table 2 on page 10 has been updated.	page 10
	The "Hot Swapping" section on page 10 has been updated.	page 10
	Table 3 on page 10 is new.	page 10
	Table 4 on page 10 has been updated.	page 10
	The "Development Tool Support" section on page 12 has been updated.	page 12
	The "Design Considerations" section on page 12 has been updated.	page 12
	The "Pin Description" section on page 35 has been updated.	page 35
	The CG624 (Bottom View) on page 43 is new.	page 43
Advanced v1.1.2	The "DC Specifications (3.3V PCI Operation)" section on page 17 was updated.	page 17
Advanced v0.3	The "Programmable Interconnect Element" section on page 5 has been updated.	page 5
	The "I/O Modules" section on page 9 and Table 2	page 9
	The "Boundary Scan Testing (BST)" section on page 11 has been updated.	page 11
	The "Dedicated Mode" section on page 11 has been updated.	page 11
	The "Flexible Mode" section on page 11 has been updated.	page 11
	Table 7 on page 11 was changed.	page 11
	The "TRST Pin" section on page 11 has been updated.	page 11
	The "Probing Capabilities" section on page 11 has been updated.	page 11
	Table 8 on page 12 is new.	page 12
	The "Development Tool Support" section on page 12 was changed.	page 12
	The "Recommended Operating Conditions" section on page 13 has been updated.	page 13
	The "3.3V LVTTL and 5V TTL Electrical Specifications" table on page 14 was changed.	page 14
	The "5V CMOS Electrical Specifications" table on page 14 is new.	page 14
	The "5V PCI Compliance for the RT54SX-S Family" table on page 15	page 15
	The "Actel MIL-STD-883 Class B Product Flow" table on page 19 has been updated.	page 19
	The "Actel Extended Flow[1]" table on page 20 has been updated.	page 20
	The "RT54SX-S Timing Model" table on page 22 and the "Hard-Wired Clock" equation were updated.	page 22
	The "Pin Description" section on page 35 was updated.	page 35

Previous version	Changes in current version (Advanced v1.4)	Page
Advanced v0.2	The "Product Plan" table on page 2 has been updated.	2
	The "Clock Resources" table on page 8 has been updated.	8
	The "Performance" table on page 9, "I/O Modules" table on page 9, "Hot Swapping" table on page 10, "Boundary Scan Testing (BST)" table on page 11, "TRST Pin" table on page 11, "Development Tool Support" table on page 12, and "RT54SX-S Probe Circuit Control Pins" table on page 12 have changed.	9-11
	The "Absolute Maximum Ratings*" table on page 13 and "Recommended Operating Conditions" table on page 13 have been updated.	11
	The "3.3V and 5.0V Electrical Specifications" section on page 12 and "5V CMOS Electrical Specifications" table on page 14 are new.	12
	The "RT54SX-S Timing Model" on page 22 was updated.	22
	New slew rates were added to the "RT54SX32S Timing Characteristics" on page 28, page 29, and page 34.	29, 30, 35
Advanced v0.1.1	The TRSTB pin was incorrectly named and changed to TRST.	All
	In the "RT54SX-S Product Profile" table on page 1, the User I/Os have changed.	1
	In the "Ceramic Device Resources" table on page 2, the User I/Os have changed.	2
	The Clock Networks section has changed to "Clock Resources" table on page 8.	8
	The "TRST Pin" table on page 11 has changed.	10
	The"Design Considerations" table on page 12 Design Considerations section has changed.	11
	In the "2.5V/3.3V/5V Operating Conditions" table on page 13 section, the "Absolute Maximum Ratings*" table on page 13 changed. The I_{IO} row containing the I/O Source Sink Current was deleted.	12
	Equation 2 in the "Junction Temperature (T_J)" table on page 21 was corrected.	15
	Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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