Power-Up and Power-Down Behavior of 54SX and RT54SX Devices

Introduction

One of the key benefits of Actel's nonvolatile antifuse FPGA technology is the ability of the devices to be live at power-up. Since no configuration PROMs are required to download design information to the device, Actel FPGAs are ready to run as soon as the power-up sequence is complete. However, there are a few restrictions that need to be considered while designing with these devices. This Application Note explains all the requirements of Actel's 54SX and RT54SX devices during power-up and power-down. In addition, this Application Note also discusses the behavior of outputs during power-up, explains when the device is functional, and provides recommended ramp rates for power-up.

This report was measured in a laboratory environment. The values reported are typical values, and therefore, not guaranteed maximum or minimum values.

Background

In order to fully understand the power-up characteristics of Actel 54SX and RT54SX FPGAs, the user must first learn some background information about the power-up circuitry and understand the function of each power supply. The three power supplies available on 54SX and RT54SX devices are:

1. V_{CCI}: This is the power supply for all I/Os on the device
2. V_{CCR}: This is the reference voltage used for input tolerance
3. V_{CCA}: This is the power supply for the internal array

During power-up, the V_{CCA} voltage is used to initiate a sequence of events that puts the device into functional mode. Once V_{CCA} reaches approximately 2.0V (See "I/O Behavior" for minimum values and their dependency on ramp rate), a sensing circuit enables an internal charge pump. The charge pump provides a high voltage (5-8V) that is used to turn on isolation devices throughout the FPGA. These isolation devices reside on the input and output of every logic module in the chip and are used to isolate the logic modules from high voltages during programming. During normal operation, all isolation transistors are turned on, which allows the logic array and I/Os to function according to the design. The V_{CCA}-controlled sensing circuit also places the JTAG circuitry in TEST-LOGIC-RESET mode, so the device is in normal operation mode. The flip-flops in the design are not initialized to a known state during power-up. Thus, the user needs to provide an external signal to reset the flip-flops upon power-up.

Power Supply Requirements

Table 1 lists the specific power supply requirements for the 54SX and RT54SX FPGAs.

Table 1 • *Power Supply*

	V_{CCA}	V_{CCI}	V_{CCR}	Input Tolerance	Output Drive
All 54SX and RT54SX	3.3V	3.3V	5.0V	5.0V	3.3V
54SX16P	3.3V	3.3V	3.3V	3.3V	3.3V
	3.3V	3.3V	5.0V	5.0V	3.3V
	3.3V	5.0V	5.0V	5.0V	5.0V

Power-Up Behavior

I/O Behavior

During power-up, a pull-up transistor between each I/O and V_{CCI} will be turned on. Therefore, the I/Os will appear to drive LOW until the device is active. The amount of time the I/Os drive LOW depends on the ramp rates of the board's power supplies and the time delta between V_{CCR} and V_{CCA}. After the I/Os drive LOW, they will behave according to the design.

Table 2 on page 2 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for all 54SX and RT54SX devices at room temperature. Table 2 on page 2 assumes a linear ramp-up profile to 3.3V. The reset process that enables the outputs begins when V_{CCA} reaches the nominal value of about 2.0V (+/- 0.5V). Table 2 on page 2 characterizes the voltage at which the outputs become active against the V_{CCA} value for the listed power-up rate. For example, if the user powers-up an 54SX32 device at 0.66V/ms, the outputs become active when V_{CCA} reaches about 2.1V. The point at which the I/Os become enabled depends on the power-up rate and process variations between different devices. Note, results may vary from those presented here due to these dependencies.

Transient Current

When V_{CCA} reaches a voltage of about 2.0V, the V_{CCA} power supply will experience a transient current for approximately 500ns. This current is due to the sudden switching of all the internal logic modules when the device initialization is applied.

The value of the transient current is highly dependent on the V_{CCA} ramp-up rate and the size of the device. Table 3 summarizes typical values of the transient current for different ramp rates and device sizes at room temperature.

Table 2 • *V_{CCA} Voltage where I/Os Become Active (V)*

Ramp Rate	0.33V/µs	0.033V/µs	6.6V/ms	3.3V/ms	0.66V/ms	0.33V/ms	0.132V/ms	0.033V/ms
54SX08	3.3	3.3	2.6	2.2	2.0	2.0	1.9	1.9
54SX16	3.3	3.3	2.9	2.2	1.8	1.7	1.7	1.5
54SX16P	3.3	3.3	2.9	2.5	2.0	1.9	1.8	1.7
54SX32	3.3	3.3	3.2	2.8	2.1	2.0	1.9	1.9
RT54SX16	3.3	3.3	2.9	2.8	2.5	2.4	2.3	2.3
RT54SX32	3.3	3.3	3.2	3.0	2.6	2.5	2.4	2.2

Table 3 • *Typical Peak Transient Current (mA)*

Ramp Rate	0.33V/µs	0.033V/µs	6.6V/ms	3.3V/ms	0.66V/ms	0.33V/ms	0.132V/ms	0.033V/ms
54SX08	195	175	82	58	42	42	39	39
54SX16	415	413	274	172	90	70	53	45
54SX16P	369	368	250	145	55	45	30	30
54SX32	732	696	628	469	220	187	169	158
RT54SX16	389	348	276	222	183	159	126	126
RT54SX32	599	600	524	427	285	243	212	167

Power-Up/Power-Down Requirements

Sequence

The order in which the power supplies are ramped up and ramped down is critical for all 54SX and RT54SX devices. To avoid device damage, V_{CCR} must be greater than or equal to V_{CCI} at all times. This guideline applies to both power-up and power-down sequences. A p-n junction exists between the V_{CCI} and V_{CCR} power supplies in the circuitry of the JTAG TDI and TMS pins. When V_{CCI} is greater than V_{CCR} by 0.6V, the p-n junction will forward bias and cause excessive current flow. This condition cannot be violated for any period of time. The excessive current through the p-n junction may damage the TDI and TMS pin circuitry.

Complete Power-Down

On an Actel 54SX16, 54SX16P, RT54SX16, or RT54SX32 FPGA, it is important that V_{CCA} does not rise above 0.0V before initiating the power-up sequence. V_{CCA} must begin its power-up from 0.0V. This power-up consideration does not apply to 54SX08 or 54SX32 devices due to differences in the power-up circuitry. If any amount of residual voltage is present on V_{CCA} before power-up, the sensing circuit may not generate an appropriate reset signal, thus causing the FPGA to power-up in an unknown state. Should the JTAG state machine power-up in an unknown state, all I/Os will most likely be tristated. This does not cause any damage to the device, but the FPGA may not be functional after power-up.

For all RT54SX devices, this can be avoided by connecting the TRST pin to ground during power-up. Actel recommends this pin always be connected to ground for normal operation.

Driving I/Os before Power-Up

As stated earlier, the 54SX and RT54SX I/Os may drive low during power-up. Actel recommends that voltage only be applied to the inputs after the power-up sequence has been completed for all power supplies.

Applying a voltage greater than V_{CCI} to the TDI or TMS pins on 54SX and RT54SX devices may cause residual voltage to appear on V_{CCA}. This may cause the symptoms described in the previous section, "Complete Power-Down" for 54SX16, 54SX16P, RT54SX16, and RT54SX32 devices. This is due to a current path that exists from the TDI and TMS pins to V_{CCA} (if it uses the same power supply as V_{CCI}). If V_{CCA} and V_{CCI} are not directly connected together on the board, this

condition does not occur. External pull-up resistors from these pins to V_{CCI} are acceptable; however, pull-up resistors to V_{CCR} may cause this condition.

Conclusion

The power-up requirements for 54SX and RT54SX devices are defined in this Application Note. In order to keep the transient current during power-up to a minimum, a V_{CCA} ramp rate of 0.66V/ms or slower is recommended. If all the above power sequencing, prevention of residual V_{CCA} voltage, and I/O driving guidelines are met, the 54SX and RT54SX devices will function correctly after power-up. Specific board level power-up solutions are left to the designer.

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