Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

Introduction

All of Actel's FPGAs are nonvolatile, meaning they are live at power up and do not require a configuration device. This makes Actel's chips ideal candidates for hot-swap and cold-sparing applications. With new features like pull-up/pull-down resistors, PCI compliance, and slew rate control, Actel's SX-A and RT54SX-S devices have been specifically designed to accommodate a variety of power-up and power-down system requirements. These devices are also the first to support both hot swap and cold sparing. This document discusses in detail the characteristics of these devices during power up and recommends the proper configuration for hot-swap and cold-sparing compliance.

Power-Up Characteristics

Power-Up Sequence

Actel's SX-A and RT54SX-S devices can function with any power-up or power-down sequence of the power supplies. However, to comply with hot-swap and cold-sparing requirements using SX-A devices, V_{CCA} (array power supply) should come up no less than a diode drop below V_{CCI} (I/O power supply), so we recommend deriving both V_{CCA} and V_{CCI} from the same power supply. If V_{CCA} ramps up after V_{CCI} and more than a diode drop below it, outputs may drive to an unknown state for a short period of time during power up, regardless of power-up resistor settings (Figure 1). This is caused by the propagation delay of an input signal from an input buffer to the output buffer of your design. For RT54SX-S devices, any power-up sequence will allow hot swap and cold sparing[1] – as long as the critical path from input to output is less than 50ns. A 50ns on-chip delay has been added between both power supplies and the output enable signal for output buffers. This will provide time for input data to propagate to the output buffer before the output buffer is enabled, thus preventing any unwanted glitches (Figure 2).

On RT54SX-S devices, if V_{CCI} is powered on and V_{CCA} is off, there may be a high standby current on V_{CCI} in the order of 80mA. This has been closely studied, and we have determined that there are no reliability concerns with this condition. The device can safely remain in this state for 10 years.

1 For more information about hot-swap and cold-sparing compliance, please see the "Hot-Swap Compliance" section on page 4 and the "Cold Sparing" section on page 7.

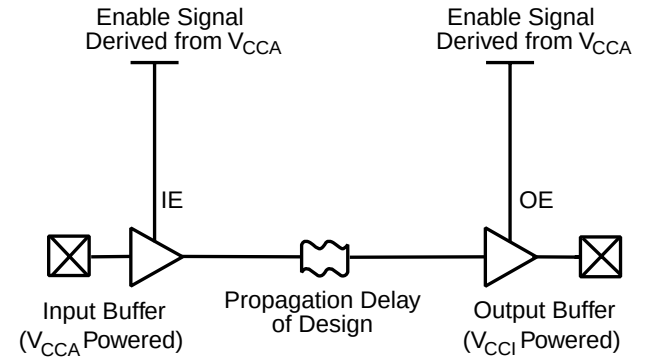

Figure 1 • SX-A Power-up Circuitry

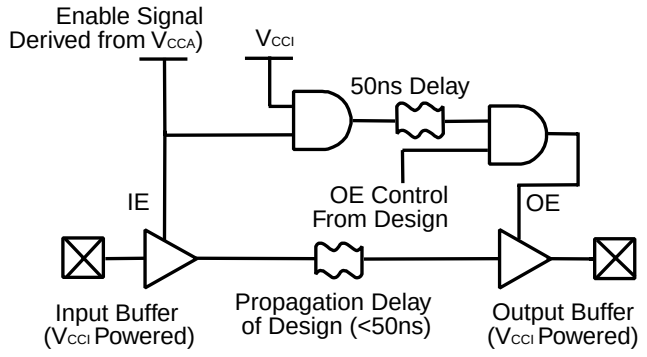

Figure 2 • RT54SX-S Power-up Circuitry

I/O State during Power Up

The I/Os of SX-A and RT54SX-S devices are tristated during power up until the I/Os become active. (For SX-A, this requires the recommended power-supply sequencing – V_{CCA} at the same time as or before V_{CCI}. See the "Power-Up Sequence" section for details).

After the I/Os become active, they will behave according to your design. Table 1 on page 2 summarizes the times at which the I/Os become active during power up for devices at room temperature with various ramp-up rates. The data assumes a linear voltage ramp up to 2.5V.

Power-up Resistors

All SX-A and RT54SX-S devices are equipped with optional pull-up or pull-down resistors of about 50kΩ that are enabled during power up. Just slightly before V_{CCA} reaches 2.5V, these resistors are disabled so the I/Os will behave normally (Figure 3 on page 2). When using these resistors,

consider the following: On SX-A devices, the risk of an I/O driving a temporary unknown state towards the end of the power-up sequence still remains when V_{CCI} is powered up before V_{CCA} (this glitch is discussed in the "Power-Up Sequence" section on page 1). The resistors cannot override this phenomenon (Figure 4 on page 3). When V_{CCA} is powered-up first, outputs will drive according to your design when the resistors are disabled. For RT54SX-S, outputs will drive according to your design when the resistors become disabled regardless of the power-up sequence.

The power-up resistors are available for all I/O standards. We recommend that you only use this feature for output signals. You are allowed to assign a power-up state to inputs that will be seen by inputs during, but not after, power up. Therefore, since the time at which the power-up state becomes disabled is variable, it is difficult to prevent a floating input condition, which can cause unknown values to be input through an I/O.

The pull-up and pull-down resistors can be enabled in the Designer software in the PinEdit tool on an individual basis (Figure 5 on page 3).

Table 1 • *Power-up Time at which I/Os Become Active*

Ramp Rate	0.25V/µs	0.025V/µs	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2
RT54SX32S	8	78	0.40	0.70	2.8	5.2	13.0	47.0
RTSX72S	10	100	0.42	0.68	2.6	4.8	11.0	40.0

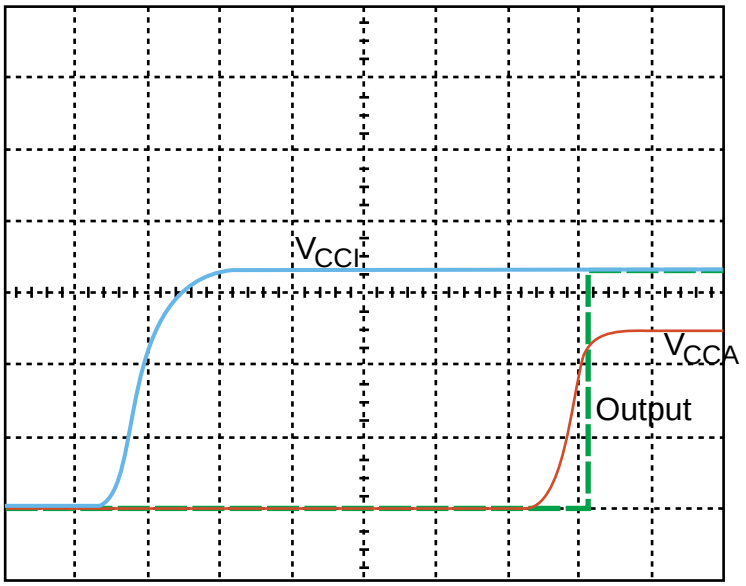

Figure 3 • *Scope Plot of Actual Output Behavior During Power up with Active Pull-down Resistor*

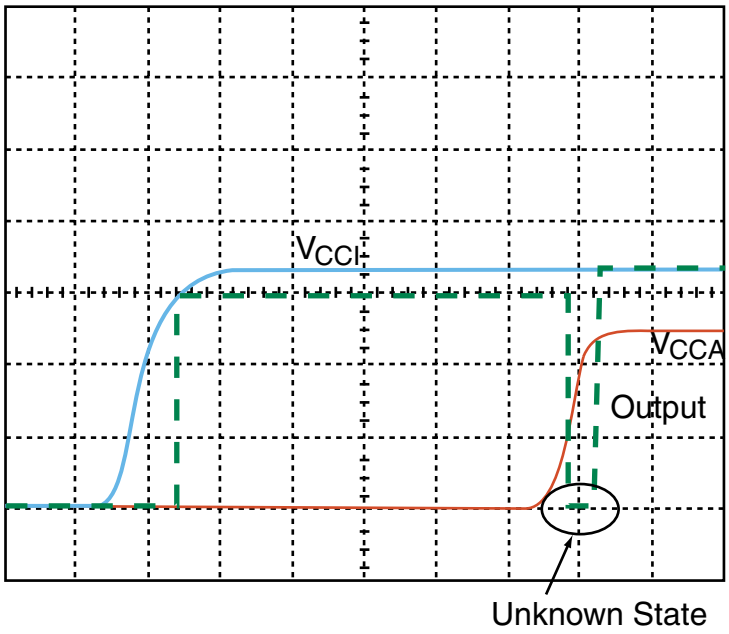

Figure 4 • *Output Driving to Unknown State with Pull-Up Resistor*

	Port Name	Macro Cell	Pin #	Fixed	I/O Standard	IO Threshold	Slew	Power Up State	Hot Swap	Loading (pf)
1	Address(7)	ADLIB:OUTBUF	23	☑	LVTTL	LVTTL	High	High	On	35
2	HoldMode	ADLIB:INBUF	99	☑	LVTTL	LVTTL	--	None	On	--
3	Fanout(1)	ADLIB:OUTBUF	153	☑	LVTTL	LVTTL	High	High	On	35
4	Fanout(2)	ADLIB:OUTBUF	151	☑	LVTTL	LVTTL	High	Low	On	35
5	TraceIn	ADLIB:INBUF	171	☑	LVTTL	LVTTL	--	None	On	--
6	WriteEnable	ADLIB:OUTBUF	33	☑	LVTTL	LVTTL	High	None	On	35

Figure 5 • *Setting Power-Up State in the Designer's Software PinEdit*

Transient Current

During power up of the SX-A and RT54SX-S devices, a built-in initialization sequence turns off isolation devices inside the FPGA. These isolation devices are only used during programming to protect the logic array and I/Os from high programming voltages. When the isolation devices are disabled, the array and I/O logic modules are enabled simultaneously, causing a large transient current to exist for approximately 500ns on the V_{CCA} plane. The device I/Os will remain tristated during this time. The duration and time of occurrence of this current pulse will vary depending on the ramp rates of the power supplies as will the maximum value of this current. Current values have been measured for several different power-up rates under typical operating conditions (room temperature, V_{CCA} at 2.5V). The results are summarized in Table 2.

The transient current will occur during the ramp up of V_{CCA} just slightly before the point at which the I/Os become active (Table 1 on page 2).

Table 2 • *Typical Peak Transient Current on V_{CCA} (mA)*

Ramp Rate	0.25V/µs	0.025V/µs	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
A54SX08A	162	125	61	51	41	50	46	45
A54SX16A	247	267	159	104	46	34	74	56
A54SX32A	440	430	340	236	116	97	73	72
A54SX72A	557	549	353	232	108	92	73	66
RT54SX32S	408	310	335	352	228	206	180	144
RT54SX72S	790	789	544	408	208	224	244	231

Hot-Swap Compliance

Hot swapping, to quote the PCI Industrial Computer Manufacturers Group[2] is the "orderly insertion and extraction of boards without adversely affecting system operation." This section summarizes the ability of Actel parts to operate in hot-swap environments. Originally the PCI SIG issued a Hot Plug Specification in 1997. This has been largely supplanted by the CompactPCI Hot-Swap Specification (dated August 3, 1998). Version 2.0, dated January 17, 2001 is the latest revision. PICMG's hot swap is a more comprehensive specification, and the remainder of the document will refer to that specification as the "Hot-Swap Specification." The PCI SIG makes a subtle distinction by saying that software support is standardized for hot swap but up to the user in hot plug. Silicon requirements are the same for both.

Actel's SX-A and RT54SX-S families provide support for hot swap according to the CompactPCI specification. These FPGAs do not have to be configured as PCI compliant to satisfy these hot-swap requirements.

Hot-Swap Silicon Requirements

The Hot-Swap Specification defines three levels of compatibility that silicon vendors may use to claim compliance:

- Silicon Requirements for hot-swap compliant boards
- Requirements for hot-swap silicon
- Recommended features for hot-swap silicon

Implementation in a Hot-Swap Compliant Board is by far the most important for a programmable-logic device. All of these requirements cannot be met with external circuitry alone. The required features are described in the following subsections. Hot-swap silicon includes all features needed for hot-swap compliant boards plus software registers in PCI configuration space (support for software connection control) and support for device hiding. Although the basic Actel silicon does not include such features, Actel's CorePCI macros do, as described in detail below. The final class, Recommended Features, encompasses all requirements for hot-swap silicon plus support circuitry for voltage precharge, early power, and the 64EN# signal. Version 2.0 of the Hot-Swap Specification has also added optional *Initially Not Responding* silicon support.

Silicon Requirements for Hot-Swap Compliant Boards

The silicon requirements are as follows:

- PCI Specification 2.1 (or later) Compliant
- Toleration of V_{CC} from Early Power
- Asynchronous Reset
- Precharge Voltage Toleration
- Modified I/O Buffer V/I Requirements
- Limited I/O Pin Leakage

PCI Specification 2.1 (or later) Compliant

The PCI device buffers must meet the AC specifications for 5.0V or 3.3V signaling. Input buffers require a clamping diode to ground. The clamp to V_{CCI} is optional in a 5.0V system, whereas in a 3.3V only system, the clamp is required (the power supply is the system power supply of 3.3V).

In addition, pull-up clamp diode to a power rail must be able to withstand short-circuit current until the drivers can be tristated (Figure 6).

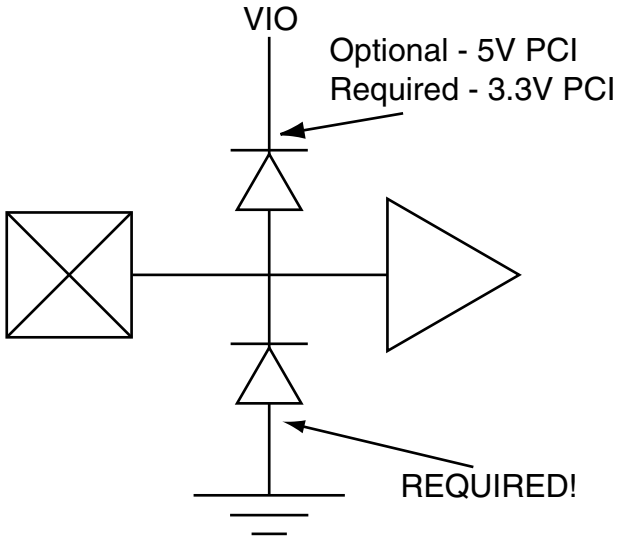

Figure 6 • *Hot-Swap PCI Input Buffer with Clamp Diodes*

In the Actel SX-A and RT54SX-S parts, selection of the clamping diode to V_{CCI} is fuse-programmable.

There are additional requirements associated with Revision 2.2 of the PCI Specification. The PCI buffers must be in a high-impedance state when the device reset is asserted. This is required in Revision 2.2 of the spec, but may not be the case in Revision 2.1. Actel's devices are compliant with this revision.

In addition, after RST# is released and before the device completely responds to a PCI cycle, Revision 2.2 specifies that the device is either *Initially Not Responding* or *Initially Retrying*. Actel's devices are in the former category, which is preferred for hot-swap compliance.

The output buffers use a slightly different V/I curve for hot swap as discussed in the "Modified I/O Buffer V/I Requirements" section on page 6. Actel SX-A and RT54SX-S devices fully comply with this requirement.

2 PICMG, CompactPCI Hot-Swap Specification, R2.0, January 17, 2001.

Toleration of V_{CC} from Early Power

The early power pins supply the power for the I/O circuit during physical insertion. These can be limited using a series register, so the maximum 5.0V and 3.3V supply currents during insertion may be somewhat lower than during normal operation of the card. Power up and power down are controlled in the CompactPCI environment using boards with unequal-length pins.

The insertion/power-up process consists of the following steps (unimportant steps from a silicon point of view have been eliminated):

- The board is in the "not-installed" state.
- Board installation begins.
- The board's logic ground is discharged to chassis ground through a bleed resistor.
- The bleed resistor breaks contact with chassis ground. Logic ground is again isolated.
- The board contacts long pins on the backplane first. These are for ground, +5.0V, +3.3V, and V_{CCI}. The board is in an unstable state when pins are first mated. Note: This condition typically lasts less than 4ns, but could be much longer.
- Enough pins are connected to achieve stable early power. CompactPCI bus interface logic is powered up and decoupling capacitors attached to early power are charged. The device's PCI reset signal is driven active and is asserted throughout the connection process. The device asynchronously tristates all PCI signals. Early power stabilizes all of the CompactPCI bus signals to the signal precharge potential.
- The board contacts the medium-length pins on the backplane, which will make contact in a random manner. The board's CompactPCI pins begin to track the levels on the PCI bus. The board now receives the PCI clock. The medium-length power pins contact and short out the current-limiting resistors.
- The board contacts the short BD_SEL# pin. The board is now fully inserted in the backplane. The precharge potential is now (optionally) removed from each signal, and the board enters the "installed" state.

The SX-A devices use a core voltage of 2.5V and an I/O voltage of either 3.3V or 5.0V. CompactPCI provides 3.3V and 5.0V power, but not 2.5V, which must be derived from one of the other two supplies. Therefore, at power up there are four possibilities:

V_{CCI} = 3.3V

- 2.5V derived from 3.3V supply (V_{CCI})
- 2.5V derived from 5.0V supply

V_{CCI} = 5.0V

- 2.5V derived from 3.3V supply
- 2.5V derived from 5.0V supply (V_{CCI})

If different power supplies are used to derive the I/O and array voltages, the device may not be hot-swap compliant. Also, even if the Actel core and I/O voltages are derived from the same supply, the order of supply power up is less critical, but it is still possible for the I/O voltage to be applied before the core voltage. Powering the SX-A or RT54SX-S core before or at the same time as, the I/O ring is required for hot-swap compliance. Additional power-up information is discussed in the "Power-Up Characteristics" section on page 1. Actel SX-A and RT54SX-S devices fully comply with this requirement as long as the I/O voltage is not supplied before the core voltage.

Asynchronous Reset

The device must maintain a high-impedance output until reset is released (this is not the master PCI reset). The bus pins will be live when reset is released, and therefore a requirement exists in which state machines must be able to recover from unknown states. Of course, this should not affect the I/O circuits. Note, since the local PCI_RESET# signal is stable before the medium pins are contacted, this signal can be used to tristate the PCI bus signals. In other words, the I/O buffers need not power on in a tristated condition. Actel SX-A and RT54SX-S devices fully comply with this requirement.

Precharge Voltage Toleration

The device must tolerate holding I/O pins at the precharge voltage for an unspecified period. This is not a problem for the I/O buffer itself. However, there is an issue associated with power up and power down. The combination of precharge and a power rail at 0V could cause excessive current draw from two sources. One could be the hot-swap monitoring circuitry; the other is the clamp diode required for 3.3V PCI.

To avoid a potential problem, the power rail for either 5.0V or 3.3V devices MUST be no more than a diode drop below the precharge voltage at all times. The orderly power-up/power-down procedure (with early power pins) specified by the CompactPCI Hot-Swap Specification is highly recommended. If the system complies with this, then SX-A and RT54SX-S devices meet the Precharge Voltage Toleration requirement.

Modified I/O Buffer V/I Requirements

The device's output buffer must have the same characteristics as the standard 5V PCI output buffer with two exceptions. For pull down, standard PCI allows low-voltage drive to begin at 0.55V, while hot-swap PCI requires that drive begin at 0V. On the pull-up side, standard PCI allows voltage drive to begin at 2.4V, while hot-swap PCI requires that driving begin at 3.3V. Actel SX-A and RT54SX-S devices fully comply with this requirement.

Limited I/O Pin Leakage

V_P at the device must be adjusted so that I/O pin leakage over all operating conditions is limited to 10µA. It is a recommendation, not required, that the I/O pin leakage is controlled within even tighter limits. I/O pin leakage in the SX-A and RT54SX-S devices be currently specified at a maximum of 10µA. Actel SX-A and RT54SX-S devices fully comply with this requirement.

Summary of Silicon Requirements for Hot-Swap Capable Boards

Actel SX-A and RT54SX-S parts meet the CompactPCI requirements (Revision 1.0 or 2.0) for hot-swap capable boards. Actel recommends that all designs follow the Compact PCI Hot-Swap Specification.

If a board does not completely conform to the Hot-Swap Specification, it is recommended that at least the power up and power down be controlled as specified in the Hot-Swap Specification. Even if power up and power down are not controlled, there is never a problem with 3.3V PCI operation.

Hot-Swap Silicon

Software/Register Requirements

As a minimum, hot-swap silicon requires a hot-swap control and status register mechanism. The Actel PCI Target, Target+DMA, and Target/Master macros implement this feature in accordance with the Hot-Swap Specification. A brief description follows.

The Hot Plug System Driver uses a uniform bit assignment ("Not Used" means reads are undefined and writes should always be 0):

Bit 7 – ENUM# Insertion Status

1 – ENUM# Asserted

0 – Not Asserted

Bit 6 – ENUM# Insertion Status

1 – ENUM# Asserted

0 – Not Asserted

Bit 5 – Not Used

Bit 4 – Not Used

Bit 3 – LED ON/OFF (the "Blue LED" that indicates it is safe to extract the card)

1 – LED ON

0 – LED OFF

Bit 2 – Not Used

Bit 1 – ENUM# Signal Mask

1 – Mask Signal

0 – Enable Signal

Bit 0 – Not Used

The accessing of the hot-swap control and status register is through two levels of indirection. First, Bit 4 of the regular PCI status register (address 04h) is set to indicate the presence of a capabilities list. If that bit is set, then register 37h in the configuration header indicates the location of the first item in the linked list. The two least significant bits must be zero (the offset is DWORD aligned). This address would point to the hot-swap register block.

In the case of an Actel PCI macro, register 37h contains 80h. The macro implements the following register block in configuration space:

80h – Reserved

81h – Hot-Swap Control and Status Register

82h – Next Item in Capabilities List (a dummy location in our case)

83h – 06h (indicates hot-swap capability)

Revision 2.0 of the Hot-Swap Specification includes a provision for device hiding support. This has not yet been incorporated in Actel's PCI macro.

Summary of Hot-Swap Silicon Features

Although an unprogrammed Actel FPGA does not contain hot-swap silicon features, these PCI-specific features ARE part of the Actel PCI macros, so an FPGA that includes the macro will satisfy Revision 1.0 of the Hot-Swap Specification's requirements for hot-swap silicon features. Support for device hiding will be incorporated in a future release of Actel's PCI macro.

Recommended Hot-Swap Silicon Features

Actel devices do NOT currently support any of the optional hot-swap silicon features. Such circuitry should be implemented outside of Actel's devices, although a portion of the control circuitry can be done using programmable logic.

Cold Sparing

As discussed in the "Power-Up Sequence" section on page 1, the I/Os of SX-A and RT54SX-S devices can be tristated during power up. Cold-sparing applications rely on this silicon feature. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, both V_{CCA} and V_{CCI} must be clamped to ground. Also, any I/Os being driven must not be in 3.3V PCI mode, since clamp diodes will forward bias (this includes disabling the clamp diode on unused I/Os and JTAG pins – see the "Driving Unused I/Os" section for more information). This will prevent the power supplies from experiencing residual voltage when a voltage is applied to the inputs in a cold-sparing condition. When these conditions are met, you can safely drive any I/O of an unpowered device, with less than 100µA of leakage current. The "Driving an Unpowered Device" section, for recommended software settings to enable cold sparing.

As in hot-swap applications, there will be a delay from the time at which the I/Os become active during power up to the time at which data will be valid at the output pins (Figure 2 on page 1). This delay can be determined through timing analysis of the critical path from the input pin to the output pin.

Driving an Unpowered Device

In hot-swap and cold-sparing applications, the array can inadvertently consume power even if neither V_{CCA} nor V_{CCI} is powered. This results from external driving of a tristated output, which can forward-bias the clamp diode and power up a portion of the array. To avoid this, the clamp diode should always be disabled in Actel's Designer software. This means avoiding the choice of PCI for the I/O standard. If high slew is still required, choose the LVTTL I/O standard option and select HIGH for slew. Please note that the hot-swap box will indicate on, meaning that the clamp diode is not used.

Driving Unused I/Os

If unused I/O pins are connected on the board (for future use) that are driven by another device while the device is in an unpowered state, select Disable Clamping Diode for Unused I/O Pins in the "Generate Programming Files" dialog box as shown below in Figure 7. This feature will also disable the clamp diodes on the JTAG input pins.

With this option turned on, you will avoid powering up the device through the clamping diode of an unused I/O pin.

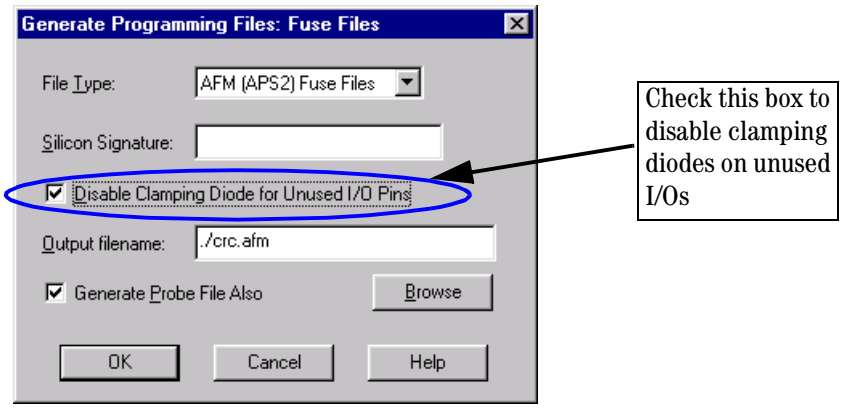

Figure 7 • Generate Programming Files: Fuse Files (Disable Clamping Diodes on Unused I/Os)

Conclusion

Actel's antifuse FPGAs provide an excellent solution for commercial and aerospace applications that require high performance, low power consumption, low cost, and exceptional reliability. With the introduction of the SX-A and RT54SX-S families, Actel now adds the benefits of power-up friendly silicon that supports both cold sparing and hot swap.

No power-up or power-down sequence is required for the devices to operate correctly. To take advantage of cold-sparing and hot-swap features, please follow the recommendations described in this document.

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