
Macro Library Guide

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Definitions

Hard Macros

The Hard Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. Please refer to the ACT Family Field Programmable Gate Array Databook for definitions of ACT family modules. The relative placement of two module-macros is pre-defined. The timing characteristics are a function of the fanout on the output of the macro.

ACTgen Macro

ACTgen macros are described in Actel's publication, "A Guide to ACTgen Macros."

Combinability

For information on combinability, refer to the *Designer Series Development Tool User's Guide*.

How to Use this Guide

Family Inclusion Indicator

On the side of each data page are tabs indicating whether the cell is a member of the ACT 1, ACT 2/1200XL, 3200DX, ACT 3, 40MX, 42MX, or 54SX library.

Guidelines

These Guidelines are applicable to Hard macros only.

1. All input pin loading is assumed to be a single load except macros that are built using two combinational modules or one sequential and one combinatorial module. These macros are assumed to have a load of two on some of their input pins.
2. All macros have output pin loading of zero except for the sequential macros that are built using two combinational modules only. These macros have an output pin loading of one.
3. All hard macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the Hard Macro section of this manual.

Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

↑	denotes rising edge clock
↓	denotes falling edge clock
X	in an input column denotes a 'don't care' or logic simulation state 'unknown'
!Q	denotes Q not

Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

Restrictions

Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as "normal" data input/output buffers or they may be used as "special" pins. The following constraints apply to I/O pins used as "special" pins.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3 and 54SX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may *only* be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

Advanced Application Notes

For Advanced Application notes, please refer to Actel's *Databook*.

HDL Instantiation of Macros

Individual macros can be instantiated in your Verilog or VHDL Code.

In Verilog, an instantiation is performed within a module with the following syntax:

```
macro_name instance_name
(.macro_pin_name(net_name), ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
AND3 U12 (.A(SIG1), .B(SIG2), .C(SIG3),
.Y(SIG4));
```

In VHDL, an instantiation is performed within an architecture with the following syntax:

```
instance_name: macro_name PORT MAP
(macro_pin_name=>signal_name, ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
U12: AND3 PORT MAP (A=>SIG1, B=>SIG2,
C=>SIG3, Y=>SIG4);
```

In either language, connection by name rather than by position is shown and is the recommended practice.

Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE interface guides.

	Target Family			
Original Family	ACT 1/40MX	ACT 2/1200XL/ 3200DX/42MX	ACT 3	54SX
ACT 1 or 40MX	X	YES	YES	NO
ACT 2, 1200XL, 3200DX, 42MX	NO	X	YES**	YES**
ACT 3	NO	NO	X	YES*
54SX	NO	NO	NO	X

* Except registered I/O, IOCLK, and IOPCL

** Except QCLK and RAM

List of Combinational Macros

AND2	3	A03B	22
AND2A	3	A03C	22
AND2B	4	A04A	23
AND3	4	A05A	23
AND3A	5	A06	24
AND3B	5	A06A	24
AND3C	6	A07	25
AND4	6	A08	25
AND4A	7	A09	26
AND4B	7	A0I1	26
AND4C	8	A0I1A	27
AND4D	8	A0I1B	27
AND5A	9	A0I1C	28
AND5B	9	A0I1D	28
AND5C	10	A0I2A	29
A01	10	A0I2B	29
A010	11	A0I3A	30
A011	11	A0I4	30
A012	12	A0I4A	31
A013	12	A0I5	31
A014	13	AX1	32
A015	13	AX1A	32
A016	14	AX1B	33
A017	14	AX1C	33
A018	15	AX1D	34
A01A	15	AX1E	34
A01B	16	AXO1	35
A01C	16	AXO2	35
A01D	17	AXO3	36
A01E	17	AXO5	36
A02	18	AXO6	37
A02A	18	AXO7	37
A02B	19	AXOI1	38
A02C	19	AXOI2	38
A02D	20	AXOI3	39
A02E	20	AXOI4	39
A03	21	AXOI5	40
A03A	21	AXOI7	40

BUFA	41	DLM8A	116
BUFF	41	DLM8B	117
CLKINT	42	DLMA	118
CM7	43	DLME1A	118
CM8	44	DLP1	119
CM8A	45	DLP1A	119
CM8F	46	DLP1B	120
CM8INV	47	DLP1C	120
CMA9	47	JKF	121
CMAF	48	DLP1D	121
CMB3	48	DLP1E	122
CMB7	49	DXAND7	122
CMBB	49	DXAX7	123
CMBF	50	DXNAND7	123
CMEA	50	FA1	124
CMEB	51	FA1A	124
CMEE	51	FA1B	125
CMEF	52	FA2A	125
CMF1	52	GAND2	126
CMF2	53	GMX4	126
CMF3	53	GNAND2	127
CMF4	54	GND	127
CMF5	54	GNOR2	128
CMF6	55	GOR2	128
CMF7	55	GXOR2	129
CMF8	56	HA1	129
CMF9	56	HA1A	130
CMFA	57	HA1B	130
CMFB	57	HA1C	131
CMFC	58	INV	131
CMFD	58	INVA	132
CMFE	59	JKF1B	132
CS1	59	JKF2A	133
CS2	60	JKF2B	133
CY2A	60	JKF2C	134
CY2B	61	JKF2D	134
DLEB	111	JKF3A	135
DLEC	111	JKF3B	135
DLM	112	JKF3C	136
DLM2	112	JKF3D	136
DLM2A	113	JKF4B	137
DLM2B	113	JKFPC	137
DLM3	114	MAJ3	138
DLM3A	114	MAJ3X	138
DLM4	115	MAJ3XI	139
DLM4A	115	MIN3	139

MIN3X	140	OA3	161
MIN3XI	140	OA3A	162
MX2	141	OA3B	162
MX2A	141	OA4	163
MX2B	142	OA4A	163
MX2C	142	OA5	164
MX4	143	OAI1	164
MXC1	143	OAI2A	165
MXT	144	OAI3	165
NAND2	144	OAI3A	166
NAND2A	145	OR2	167
NAND2B	145	OR2A	167
NAND3	146	OR2B	168
NAND3A	146	OR3	168
NAND3B	147	OR3A	169
NAND3C	147	OR3B	169
NAND4	148	OR3C	170
NAND4A	148	OR4	170
NAND4B	149	OR4A	171
NAND4C	149	OR4B	171
NAND4D	150	OR4C	172
NAND5B	150	OR4D	172
NAND5C	151	OR5A	173
NOR2	151	OR5B	173
NOR2A	152	OR5C	174
NOR2B	152	QCLKINT	174
NOR3	153	TF1A	175
NOR3A	153	TF1B	175
NOR3B	154	VCC	176
NOR3C	154	XA1	176
NOR4	155	XA1A	177
NOR4A	155	XA1B	177
NOR4B	156	XA1C	178
NOR4C	156	XAI1	178
NOR4D	157	XAI1A	179
NOR5B	157	XNOR2	179
NOR5C	158	XNOR3	180
OA1	158	XO1	180
OA1A	159	XO1A	181
OA1B	159	XOR2	181
OA1C	160	XOR3	182
OA2	160	ZOR3	182
OA2A	161	ZOR3I	183

List of Sequential Macros

DF1	61	DFM3	80
DF1A	62	DFM3B	81
DF1B	62	DFM3E	81
DF1C	63	DFM3F	82
DFC1	63	DFM3G	82
DFC1A	64	DFM4	83
DFC1B	64	DFM4A	83
DFC1C	65	DFM4B	84
DFC1D	65	DFM4C	84
DFC1E	66	DFM4D	85
DFC1F	66	DFM4E	85
DFC1G	67	DFM5A	86
DFE	67	DFM5B	86
DFE1B	68	DFM6A	87
DFE1C	68	DFM6B	87
DFE2D	69	DFM7A	88
DFE3A	69	DFM7B	89
DFE3B	70	DFM8A	90
DFE3C	70	DFM8B	91
DFE3D	71	DFMA	92
DFE4	71	DFMB	92
DFE4A	72	DFME1A	93
DFE4B	72	DFP1	93
DFE4C	73	DFP1A	94
DFE4F	73	DFP1B	94
DFE4G	74	DFP1C	95
DFEA	74	DFP1D	95
DFEB	75	DFP1E	96
DFEC	75	DFP1F	96
DFED	76	DFP1G	97
DFEG	76	DFPC	97
DFEH	77	DFPCA	98
IODFE	77	DFPCB	98
IODFEC	78	DFPCC	99
IODFEP	78	DL1	99
DFM	79	DL1A	100
DFM1B	79	DL1B	100
DFM1C	80	DL1C	101

DL2A	101
DL2B	102
DL2C	102
DL2D	103
DLC	103
DLC1	104
DLC1A	104
DLC1F	105
DLC1G	105
DLCA	106
DLE	106
DLE1D	107
DLE2A	107
DLE2B	108
DLE2C	108
DLE3A	109
DLE3B	109
DLE3C	110
DLEA	110

List of CC Macros

DF1_CC	186
DF1A_CC	186
DF1B_CC	187
DF1C_CC	187
DFC1_CC	188
DFC1A_CC	188
DFC1B_CC	189
DFC1D_CC	189
DFE_CC	190
DFE1B_CC	190
DFE1C_CC	191
DFA_CC	191
DFM_CC	192
DFMA_CC	192
DFM1B_CC	193
DFM1C_CC	193
DFP1_CC*	194
DFP1A_CC*	194
DFP1B_CC*	195
DFP1D_CC*	195
DFPC_CC*	196
DFPCA_CC*	196

List of RAM Macros

RAM4FA	198
RAM4FF	199
RAM4FR	200
RAM4RA	201
RAM4RF	202
RAM4RR	203
RAM8FA	204
RAM8FF	205
RAM8FR	206
RAM8RA	207
RAM8RF	208
RAM8RR	209

List of Input/Output Macros

BIBUF	212	DEPETL	231
CLKBIBUF	212	FECTH	232
CLKBUF	213	FECTL	232
CLKBUFI	213	FEPTH	233
CLKINTI	214	FEPTL	233
HCLKBUF	214	FECTMH	234
INBUF	215	FECTML	234
OUTBUF	215	FEPTMH	235
TRIBUFF	216	FEPTML	235
BBDLHS	217	IBUF	236
BBHS	217	IOCLKBUF	236
IBDL	218	IOPCLBUF	237
IR	218	IREC	237
IRI	219	IREP	238
OBDLHS	219	OBUFTH	238
OBHS	220	OBUFTL	239
ORH	220	ORECTH	239
ORIH	221	ORECTL	240
ORITH	221	OREPTH	240
ORTH	222	OREPTL	241
QCLKBUF	222		
TBDLHS	223		
TBHS	223		
BBHSA	224		
BBLSA	224		
BBUFTH	225		
BBUFTL	225		
BIECTH	226		
BIECTL	226		
BIEPH	227		
BIEPTL	227		
BRECTH	228		
BRECTL	228		
BREPTH	229		
BREPTL	229		
DECETH	230		
DECETL	230		
DEPETH	231		

Alphabetical List of Macros

A01.....	10	AND2A.....	3
A010.....	11	AND2B.....	4
A011.....	11	AND3.....	4
A012.....	12	AND3A.....	5
A013.....	12	AND3B.....	5
A014.....	13	AND3C.....	6
A015.....	13	AND4.....	6
A016.....	14	AND4A.....	7
A017.....	14	AND4B.....	7
A018.....	15	AND4C.....	8
A01A.....	15	AND4D.....	8
A01B.....	16	AND5A.....	9
A01C.....	16	AND5B.....	9
A01D.....	17	AND5C.....	10
A01E.....	17	AOI2A.....	29
A02.....	18	AOI2B.....	29
A02A.....	18	AOI3A.....	30
A02B.....	19	AOI4.....	30
A02C.....	19	AOI4A.....	31
A02D.....	20	AOI5.....	31
A02E.....	20	AX1.....	32
A03.....	21	AX1A.....	32
A03A.....	21	AX1B.....	33
A03B.....	22	AX1C.....	33
A03C.....	22	AX1D.....	34
A04A.....	23	AX1E.....	34
A05A.....	23	AXO1.....	35
A06.....	24	AXO2.....	35
A06A.....	24	AXO3.....	36
A07.....	25	AXO5.....	36
A08.....	25	AXO6.....	37
A09.....	26	AXO7.....	37
A0I1.....	26	AXOI1.....	38
A0I1A.....	27	AXOI2.....	38
A0I1B.....	27	AXOI3.....	39
A0I1C.....	28	AXOI4.....	39
A0I1D.....	28	AXOI5.....	40
AND2.....	3	AXOI7.....	40

BBDLHS	217	CMFA	57
BBHS	217	CMFB	57
BBHSA	224	CMFC	58
BBLSA	224	CMFD	58
BBUFTH	225	CMFE	59
BBUFTL	225	CS1	59
BIBUF	212	CS2	60
BIECTH	226	CY2A	60
BIECTL	226	CY2B	61
BIEPH	227	DECETH	230
BIEPTL	227	DECETL	230
BRECTH	228	DEPETH	231
BRECTL	228	DEPETL	231
BREPTH	229	DF1	61
BREPTL	229	DF1_CC	186
BUFA	41	DF1A	62
BUFF	41	DF1A_CC	186
CLKBIBUF	212	DF1B	62
CLKBUF	213	DF1B_CC	187
CLKBUFI	213	DF1C	63
CLKINT	42	DF1C_CC	187
CLKINTI	214	DFC1	63
CM7	43	DFC1_CC	188
CM8	44	DFC1A	64
CM8A	45	DFC1A_CC	188
CM8F	46	DFC1B	64
CM8INV	47	DFC1B_CC	189
CMA9	47	DFC1C	65
CMAF	48	DFC1D	65
CMB3	48	DFC1D_CC	189
CMB7	49	DFC1E	66
CMBB	49	DFC1F	66
CMBF	50	DFC1G	67
CMEA	50	DFE	67
CMEB	51	DFE_CC	190
CMEE	51	DFE1B	68
CMEF	52	DFE1B_CC	190
CMF1	52	DFE1C	68
CMF2	53	DFE1C_CC	191
CMF3	53	DFE2D	69
CMF4	54	DFE3A	69
CMF5	54	DFE3B	70
CMF6	55	DFE3C	70
CMF7	55	DFE3D	71
CMF8	56	DFE4	71
CMF9	56	DFE4A	72

DFE4B	72	DFP1C	95
DFE4C	73	DFP1D	95
DFE4F	73	DFP1D_CC*	195
DFE4G	74	DFP1E	96
DFEA	74	DFP1F	96
DFEA_CC	191	DFP1G	97
DFEB	75	DFPC	97
DFEC	75	DFPC_CC*	196
DFED	76	DFPCA	98
DFEG	76	DFPCA_CC*	196
DFEH	77	DFPCB	98
DFM	79	DFPCC	99
DFM_CC	192	DL1	99
DFM1B	79	DL1A	100
DFM1B_CC	193	DL1B	100
DFM1C	80	DL1C	101
DFM1C_CC	193	DL2A	101
DFM3	80	DL2B	102
DFM3B	81	DL2C	102
DFM3E	81	DL2D	103
DFM3F	82	DLC	103
DFM3G	82	DLC1	104
DFM4	83	DLC1A	104
DFM4A	83	DLC1F	105
DFM4B	84	DLC1G	105
DFM4C	84	DLCA	106
DFM4D	85	DLE	106
DFM4E	85	DLE1D	107
DFM5A	86	DLE2A	107
DFM5B	86	DLE2B	108
DFM6A	87	DLE2C	108
DFM6B	87	DLE3A	109
DFM7A	88	DLE3B	109
DFM7B	89	DLE3C	110
DFM8A	90	DLEA	110
DFM8B	91	DLEB	111
DFMA	92	DLEC	111
DFMA_CC	192	DLM	112
DFMB	92	DLM2	112
DFME1A	93	DLM2A	113
DFP1	93	DLM2B	113
DFP1_CC*	194	DLM3	114
DFP1A	94	DLM3A	114
DFP1A_CC*	194	DLM4	115
DFP1B	94	DLM4A	115
DFP1B_CC*	195	DLM8A	116

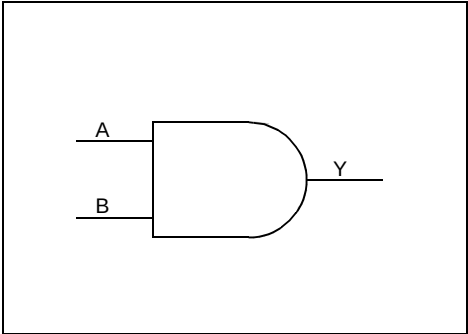
DLM8B	117	IR	218
DLMA	118	IREC	237
DLME1A.....	118	IREP	238
DLP1.....	119	IRI	219
DLP1A	119	JKF	121
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DLP1C	120	JKF2A.....	133
DLP1D	121	JKF2B.....	133
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DXAX7	123	JKF3A.....	135
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FA1.....	124	JKF3C.....	136
FA1A.....	124	JKF3D.....	136
FA1B.....	125	JKF4B.....	137
FA2A.....	125	JKFPC	137
FECTH	232	MAJ3.....	138
FECTL	232	MAJ3X	138
FECTMH	234	MAJ3XI	139
FECTML	234	MIN3	139
FEPTH	233	MIN3X.....	140
FEPTL	233	MIN3XI	140
FEPTMH	235	MX2	141
FEPTML	235	MX2A	141
GAND2.....	126	MX2B	142
GMX4	126	MX2C	142
GNAND2.....	127	MX4	143
GND	127	MXC1	143
GNOR2.....	128	MXT	144
GOR2.....	128	NAND2	144
GXOR2.....	129	NAND2A.....	145
HA1.....	129	NAND2B.....	145
HA1A	130	NAND3	146
HA1B	130	NAND3A.....	146
HA1C	131	NAND3B.....	147
HCLKBUF	214	NAND3C.....	147
IBDL	218	NAND4	148
IBUF	236	NAND4A.....	148
INBUF	215	NAND4B.....	149
INV	131	NAND4C.....	149
INVA	132	NAND4D.....	150
IOCLKBUF	236	NAND5B.....	150
IODFE	77	NAND5C.....	151
IODFEC	78	NOR2	151
IODFEP	78	NOR2A	152
IOPCLBUF	237	NOR2B	152

NOR3	153	OR5C	174
NOR3A	153	ORECTH	239
NOR3B	154	ORECTL	240
NOR3C	154	OREPTH	240
NOR4	155	OREPTL	241
NOR4A	155	ORH	220
NOR4B	156	ORIH	221
NOR4C	156	ORITH	221
NOR4D	157	ORTH	222
NOR5B	157	OUTBUF	215
NOR5C	158	QCLKBUF	222
OA1	158	QCLKINT	174
OA1A	159	RAM4FA	198
OA1B	159	RAM4FF	199
OA1C	160	RAM4FR	200
OA2	160	RAM4RA	201
OA2A	161	RAM4RF	202
OA3	161	RAM4RR	203
OA3A	162	RAM8FA	204
OA3B	162	RAM8FF	205
OA4	163	RAM8FR	206
OA4A	163	RAM8RA	207
OA5	164	RAM8RF	208
OAI1	164	RAM8RR	209
OAI2A	165	TBDLHS	223
OAI3	165	TBHS	223
OAI3A	166	TF1A	175
OBDLHS	219	TF1B	175
OBHS	220	TRIBUFF	216
OBUFFTH	238	VCC	176
OBUFTL	239	XA1	176
OR2	167	XA1A	177
OR2A	167	XA1B	177
OR2B	168	XA1C	178
OR3	168	XAI1	178
OR3A	169	XAI1A	179
OR3B	169	XNOR2	179
OR3C	170	XNOR3	180
OR4	170	XO1	180
OR4A	171	XO1A	181
OR4B	171	XOR2	181
OR4C	172	XOR3	182
OR4D	172	ZOR3	182
OR5A	173	ZOR3I	183
OR5B	173		

Combinational/Sequential Macros

AND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input AND

Truth Table

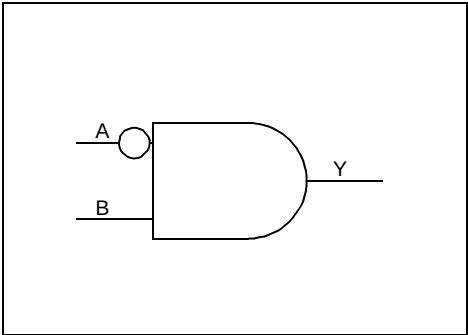
A	B	Y
X	0	0
0	X	0
1	1	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AND2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input AND with active low A Input

Truth Table

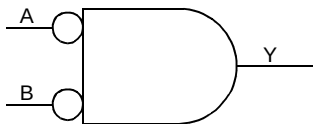
A	B	Y
X	0	0
0	1	1
1	X	0

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AND2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2-Input AND with active low Inputs

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

Input

A, B

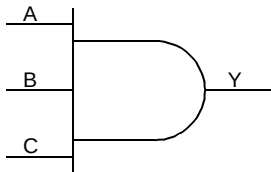
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input AND

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input

A, B,C

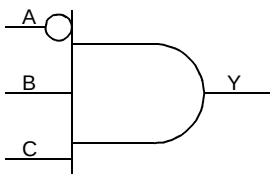
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

3-Input AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

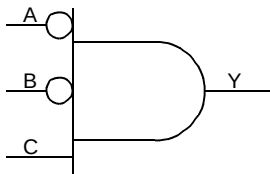
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

AND3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input AND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

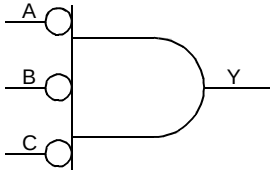
Input
A, B,C

Output
Y

Family	Modules	
	Seq	Comb
All		1

AND3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input AND with active low Inputs

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input

A, B, C

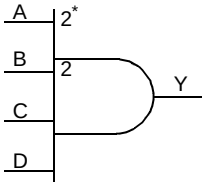
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND4

ACT 1,ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Input

A, B, C, D

Output

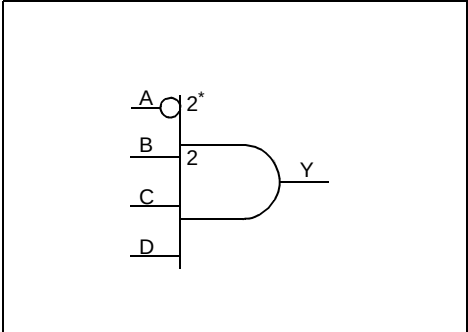
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and 40MX.

AND4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

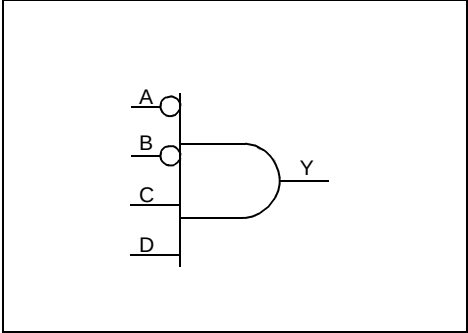
Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX		2
Others		1

* A 2 on the symbol implies 2 logic module delays, only for ACT 1 and 40MX.

AND4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input AND with active low A- and B-Inputs

Truth Table

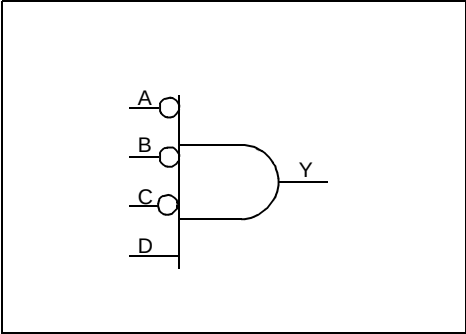
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AND4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input A, B, C, D	Output Y
----------------------------	--------------------

Function
4-Input AND with active low A-, B-, and C-Inputs

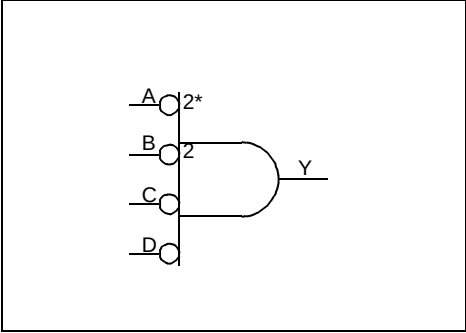
Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

AND4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input A, B, C, D	Output Y
----------------------------	--------------------

Function
4-Input AND with active low Inputs

Truth Table

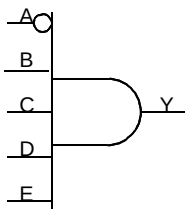
A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays, except 54SX.

AND5A

54SX



Function

5-Input AND with active low A input

Truth Table

A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Input

A, B, C, D, E

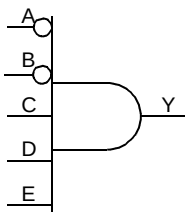
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND5B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function

5-Input AND with active low A-, and B-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

Input

A, B, C, D, E

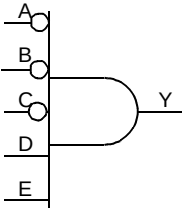
Output

Y

Family	Modules	
	Seq	Comb
All		1

AND5C

54SX



Function

5-Input AND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Input

A, B, C, D, E

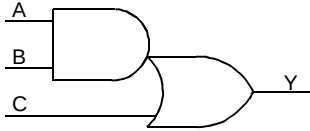
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

A01

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function

3-Input AND-OR

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Input

A, B, C

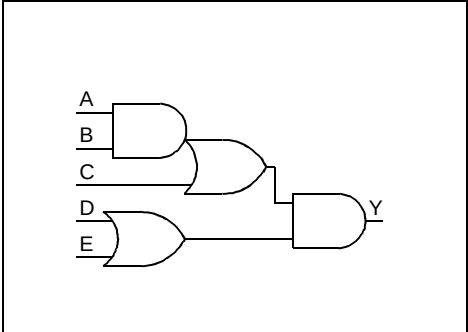
Output

Y

Family	Modules	
	Seq	Comb
All		1

A010

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Input A, B, C, D, E	Output Y
------------------------	-------------

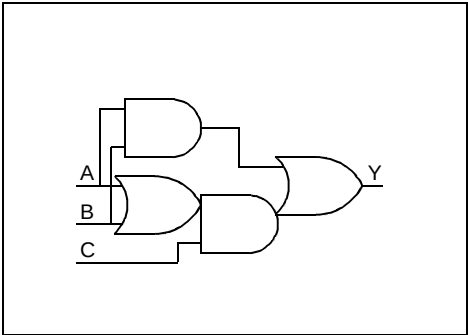
Function
5-Input AND-OR-AND

Truth Table					
A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

Family	Modules	
	Seq	Comb
All		1

A011

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Input A, B, C	Output Y
------------------	-------------

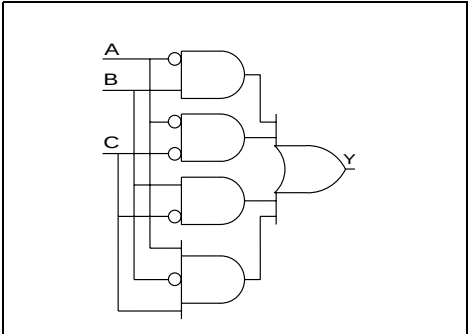
Function
3-Input AND-OR

Truth Table			
A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Family	Modules	
	Seq	Comb
All		1

A012

54SX



Input A, B, C	Output Y
-------------------------	--------------------

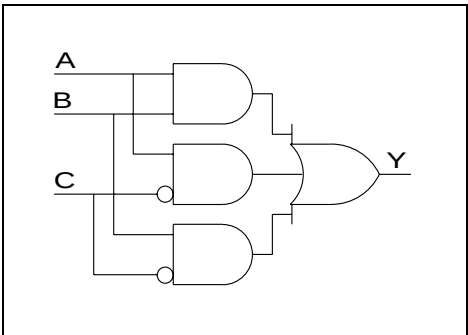
Function
3-Input AND-OR

Truth Table			
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

A013

54SX



Input A, B, C	Output Y
-------------------------	--------------------

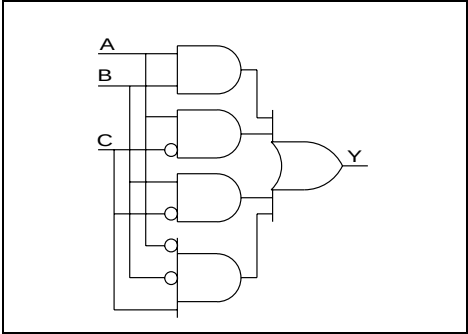
Function
3-Input AND-OR

Truth Table			
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

A014

54SX



Input A, B, C	Output Y
------------------	-------------

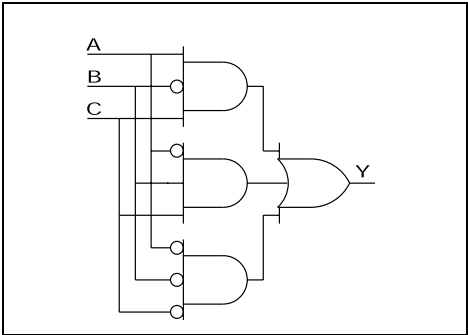
Function
3-Input AND-OR

Truth Table			
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

A015

54SX



Input A, B, C	Output Y
------------------	-------------

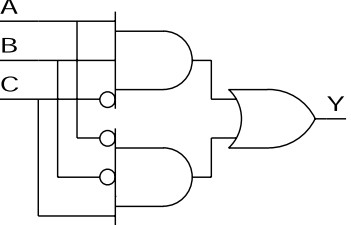
Function
3-Input AND-OR

Truth Table			
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

A016

54SX



Input
A, B, C

Output
Y

Function
3-Input AND-OR

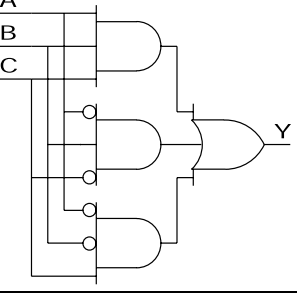
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

A017

54SX



Input
A, B, C

Output
Y

Function
3-Input AND-OR

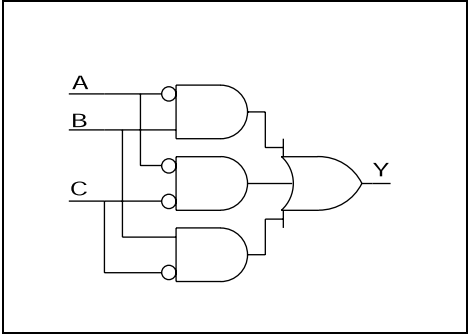
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

A018

54SX



Function
3-Input AND-OR

Truth Table

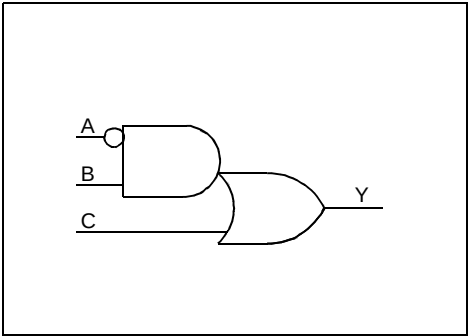
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Input A, B, C	Output Y
------------------	-------------

Family	Modules	
	Seq	Comb
54SX		1

A01A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
3-Input AND-OR with active low A-Input

Truth Table

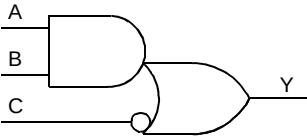
A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

Input A, B, C	Output Y
------------------	-------------

Family	Modules	
	Seq	Comb
All		1

A01B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Logic diagram for A01B: A 3-input AND-OR gate. Inputs A and B are connected to an AND gate. Input C is connected to an OR gate. The output of the AND gate and input C are connected to the OR gate. The output of the OR gate is Y.

Function
3-Input AND-OR with active low C-Input

Truth Table

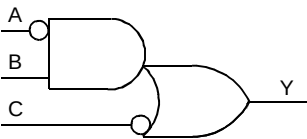
A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

A01C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Logic diagram for A01C: A 3-input AND-OR gate. Input A is connected to an AND gate with an active low bubble. Input B is connected to the AND gate. Input C is connected to an OR gate with an active low bubble. The output of the AND gate and the output of the OR gate are connected to the OR gate. The output of the OR gate is Y.

Function
3-Input AND-OR with active low A- and C-Inputs

Truth Table

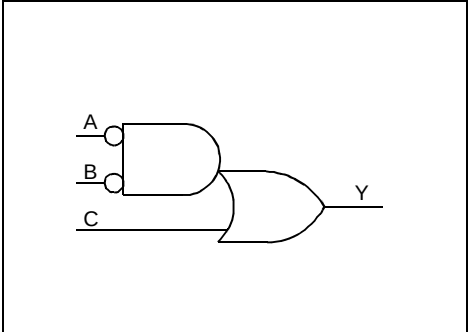
A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

A01D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
3-Input AND-OR with active low A- and B-Inputs

Truth Table

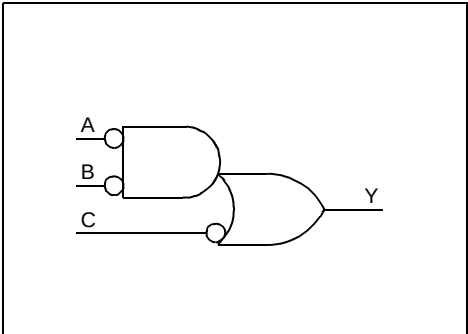
A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A01E

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
3-Input AND-OR with active low Inputs

Truth Table

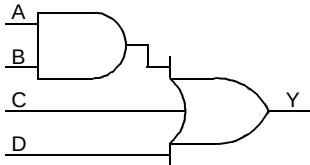
A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A02

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

Input

A, B, C, D

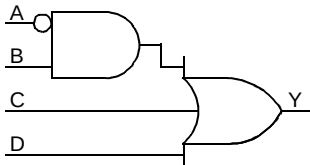
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A02A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input AND-OR with active low A-Input

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

Input

A, B, C, D

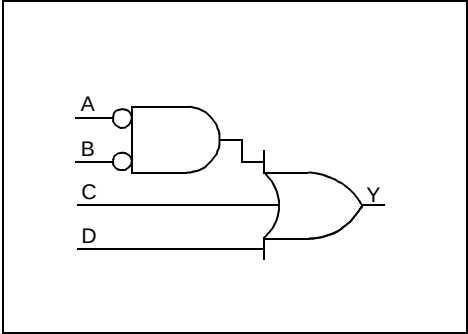
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A02B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR with active low A-Input

Truth Table

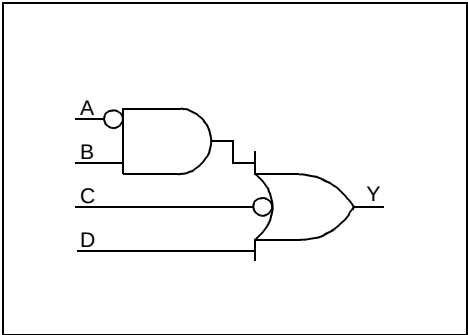
A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A02C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR with active low A- and C-Inputs

Truth Table

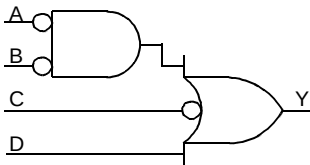
A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A02D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

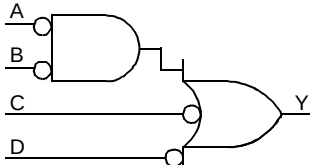
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
ALL		1

A02E

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

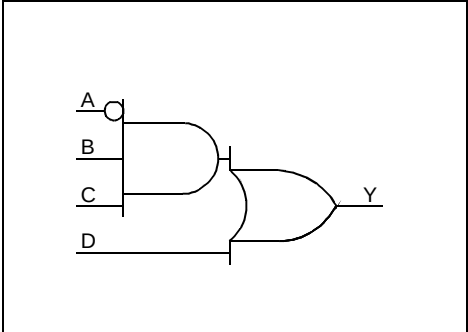
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
ALL		1

A03

Act 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input AND-OR with active low A Input

Truth Table

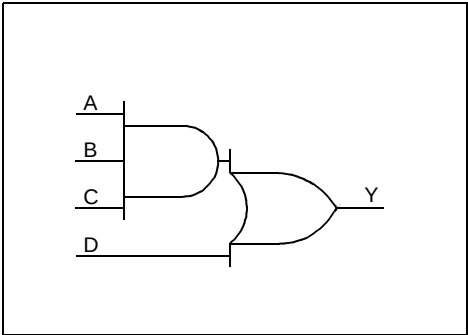
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A03A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR

Truth Table

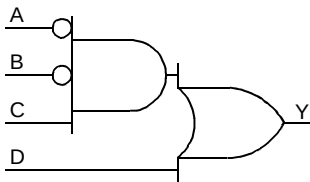
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A03B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4 Input AND-OR with active low A-, B- Inputs

Truth Table

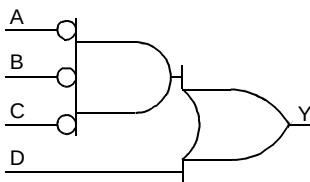
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A03C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
4-Input AND-OR with active low A-, B-, C- Inputs

Truth Table

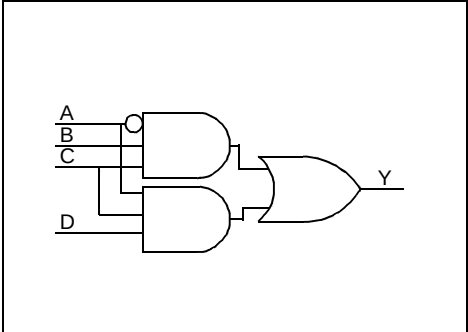
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A04A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input AND-OR

Truth Table

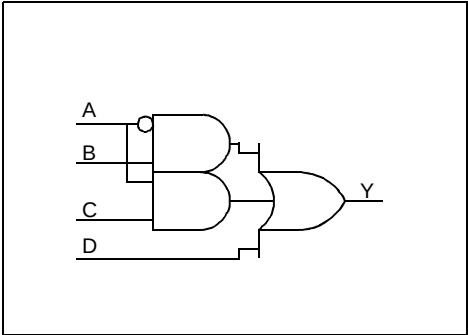
A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

Input A, B, C, D	Output Y
---------------------	-------------

Family	Modules	
	Seq	Comb
ALL		1

A05A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input AND-OR

Truth Table

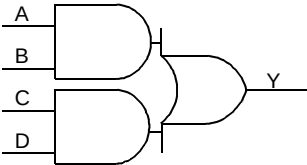
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

Input A, B, C, D	Output Y
---------------------	-------------

Family	Modules	
	Seq	Comb
ALL		1

A06

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
2-wide 4-Inputs AND-OR

Truth Table

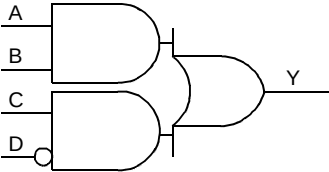
A	B	C	D	Y
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A06A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
2-wide 4-Inputs AND-OR with active low D-Input

Truth Table

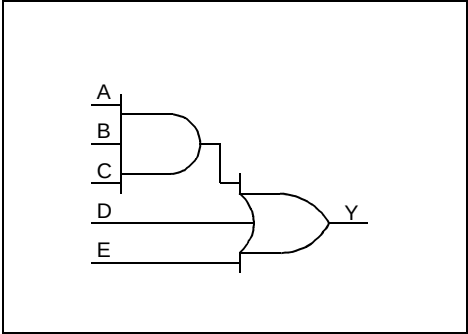
A	B	C	D	Y
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

Input A, B, C, D	Output Y
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A07

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
5-Input AND-OR

Truth Table

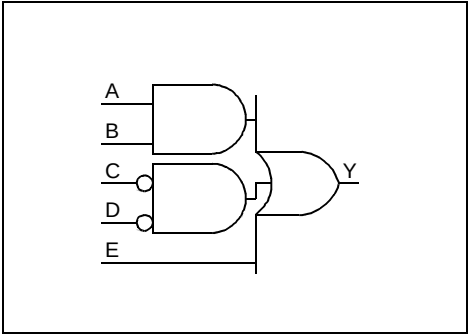
A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

Input A, B, C, D, E	Output Y
------------------------	-------------

Family	Modules	
	Seq	Comb
ALL		1

A08

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
5-Input AND-OR with active low C- and D-Inputs

Truth Table

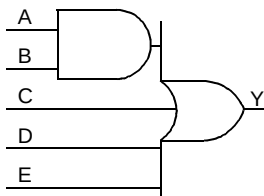
A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

Input A, B, C, D, E	Output Y
------------------------	-------------

Family	Modules	
	Seq	Comb
ALL		1

A09

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function

5-Input AND-OR

Truth Table

A	B	C	D	E	Y
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

Input

A, B, C, D, E

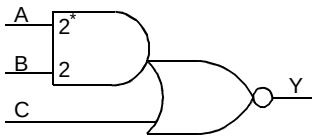
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

A011

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input AND-OR-INVERT

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

Input

A, B, C

Output

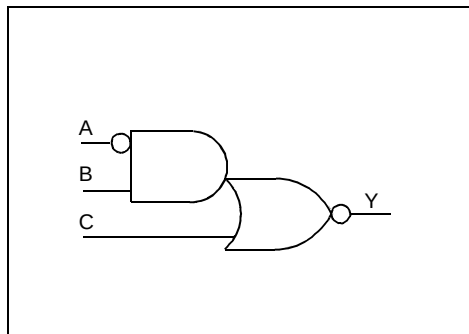
Y

Family	Modules	
	Seq	Comb
ACT 1, 40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX

A0I1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input AND-OR-INVERT with active low A-Input

Truth Table

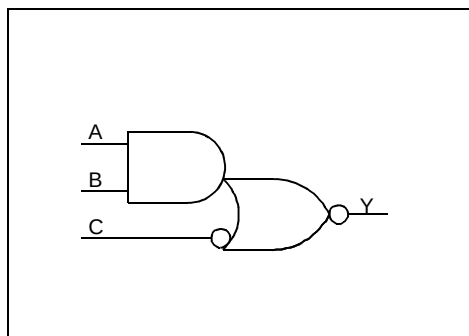
A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ALL		1

A0I1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input AND-OR-INVERT with active low C-Input

Truth Table

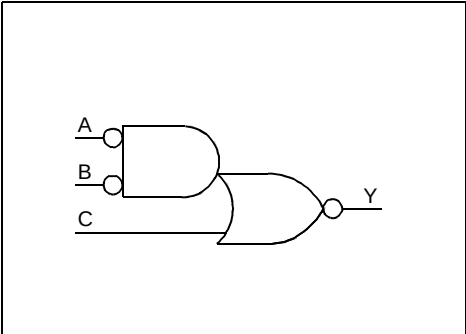
A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
ALL		1

A0I1C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
3 Input AND-OR-INVERT with active low A- and B-Inputs

Truth Table

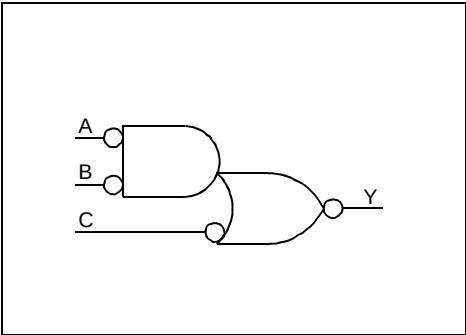
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

A0I1D

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
3-Input AND-OR-INVERT with active low Inputs

Truth Table

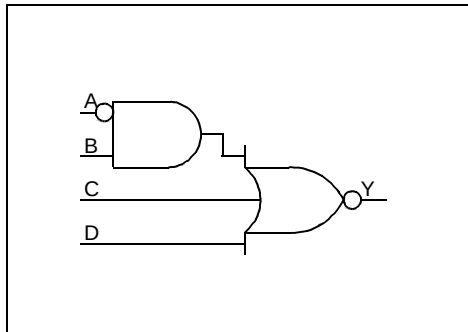
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ALL		1

AOI2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input AND-OR-INVERT with active low A-Input

Truth Table

A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

Input

A, B, C, D

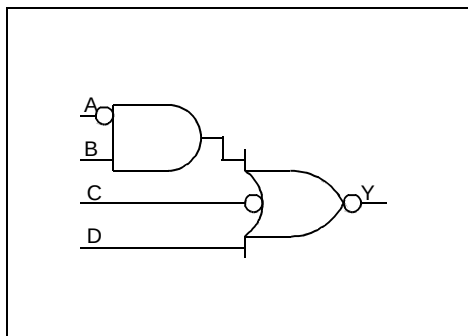
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

AOI2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input AND-OR-INVERT with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

Input

A, B, C, D

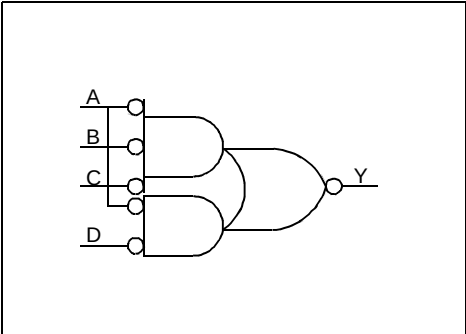
Output

Y

Family	Modules	
	Seq	Comb
ALL		1

AOI3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input A, B, C, D	Output Y
----------------------------	--------------------

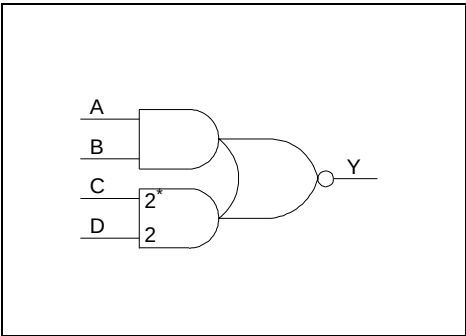
Function
4-Input AND-OR-INVERT with active low Inputs

Truth Table				
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
ALL		1

AOI4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input A, B, C, D	Output Y
----------------------------	--------------------

Function
2-wide 4-Inputs AND-OR-INVERT

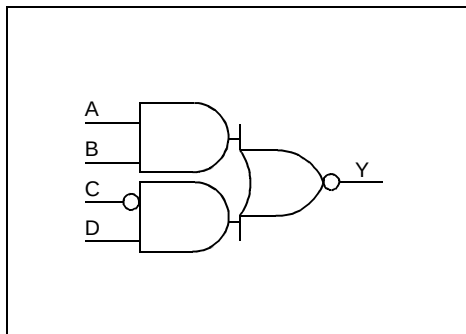
Truth Table				
A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except 54SX.

AOI4A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function

2-wide 4-Inputs AND-OR-INVERT with active low C-Input

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

Input

A, B, C, D

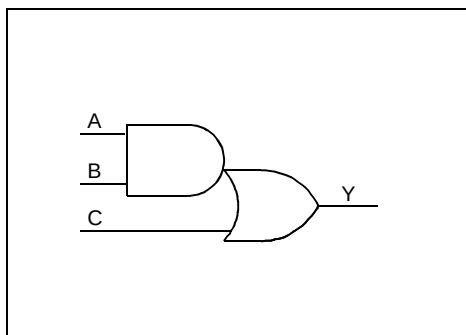
Output

Y

Family	Modules	
	Seq	Comb
All		1

AOI5

54SX



Function

3-Input AND-OR-INVERT

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

Input

A, B, C

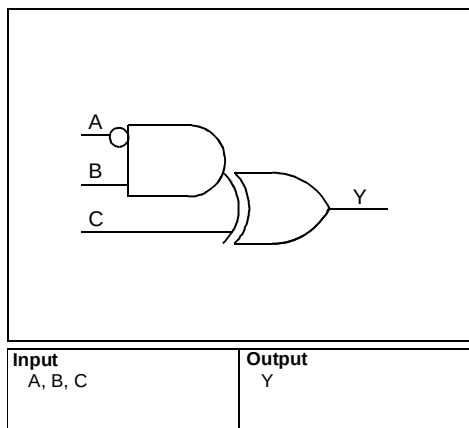
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

AX1

ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input AND-XOR with active low A-Input

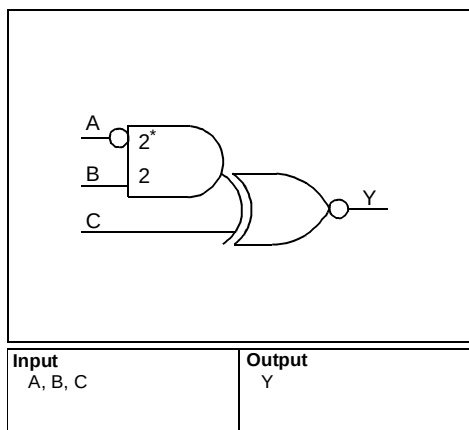
Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Family	Modules	
	Seq	Comb
ΔII		1

AX1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input AND-XOR-INVERT with active low A-Input

Truth Table

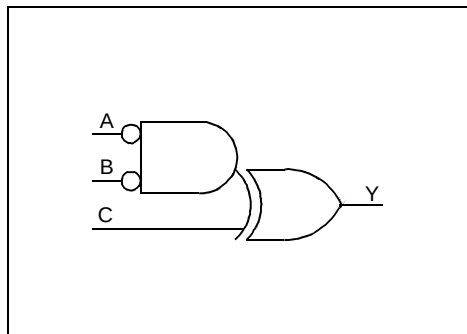
A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

Family	Modules	
	Seq	Comb
ACT 1/40MX/ 54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, 40MX, and 54SX.

AX1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input AND-XOR with active low A- and B-Inputs

Truth Table

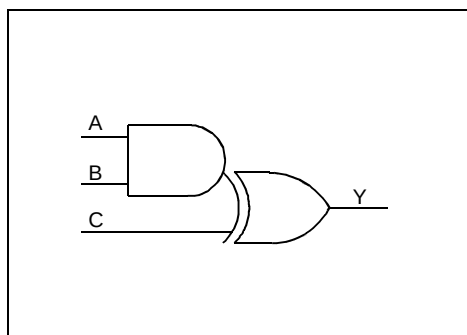
A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AX1C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX

**Function**

3-Input AND-XOR

Truth Table

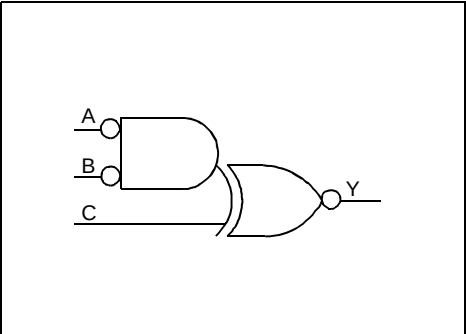
A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

AX1D

54SX



Input A, B, C	Output Y
------------------	-------------

Function
3-Input AND-XOR

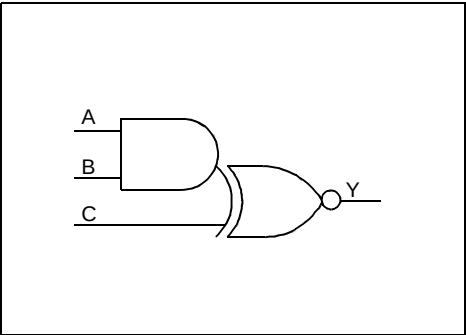
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

AX1E

54SX



Input A, B, C	Output Y
------------------	-------------

Function
3-Input AND-XNOR

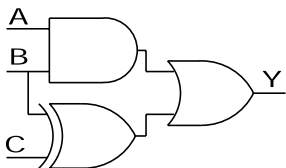
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

AXO1

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

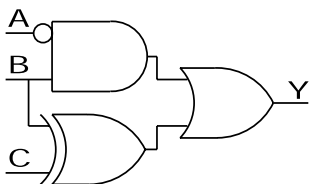
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO2

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO354SX

Logic diagram for AXO3: A 3-input OR gate. Inputs A and C are connected directly to the OR gate. Input B is connected to the OR gate through an inverter. The output of the OR gate is Y.

Input
A, B, C

Output
Y

Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

AXO554SX

Logic diagram for AXO5: A 3-input OR gate. Inputs A and C are connected to the OR gate through inverters. Input B is connected directly to the OR gate. The output of the OR gate is Y.

Input
A, B, C

Output
Y

Function
3-Input Gate

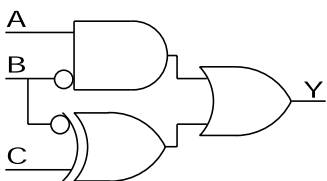
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

AXO6

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

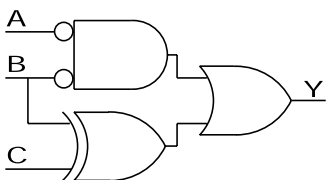
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO7

54SX



Function
3-Input Gate

Truth Table

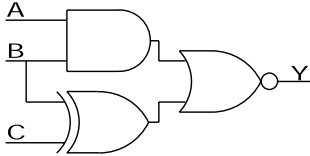
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI154SX



Function
3-Input Gate

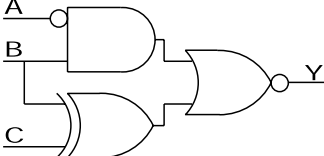
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI254SX



Function
3-Input Gate

Truth Table

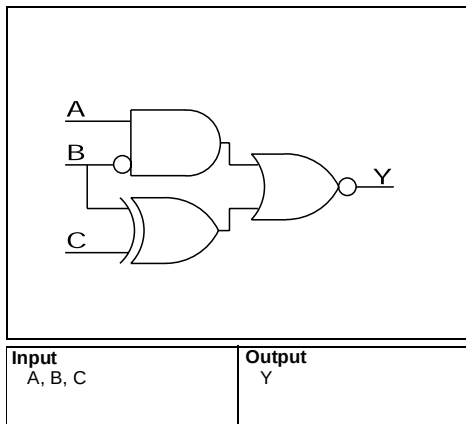
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Input	Output
A, B, C	Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI3

54SX



Function
3-Input Gate

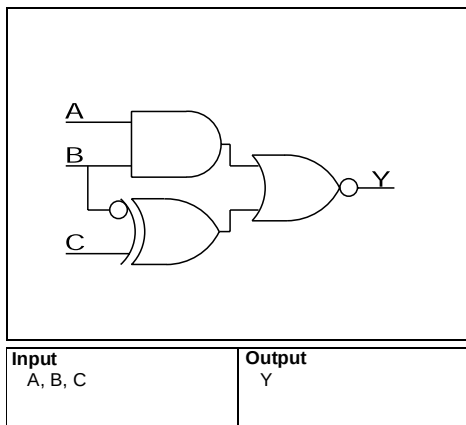
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

AXOI4

54SX



Function
3-Input Gate

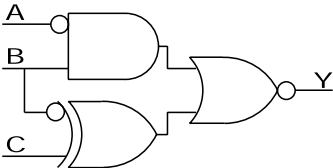
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

AXOI5

54SX



Function

3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Input

A, B, C

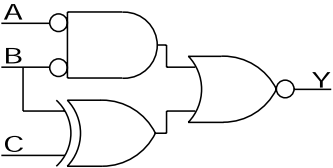
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI7

54SX



Function

3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Input

A, B, C

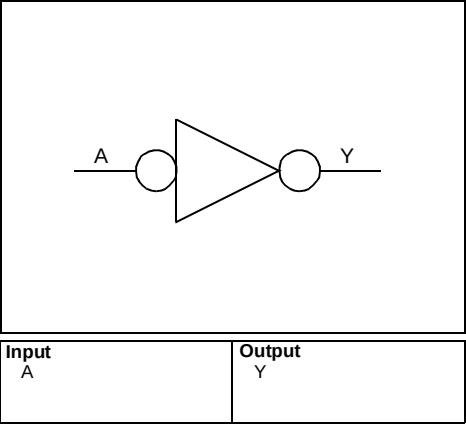
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

BUFA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Buffer, with active low Input and Output

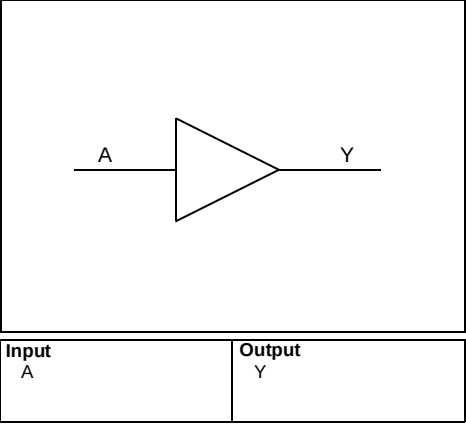
Truth Table

A	Y
0	0
1	1

Family	Modules	
	Seq	Comb
All		1

BUFF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Buffer

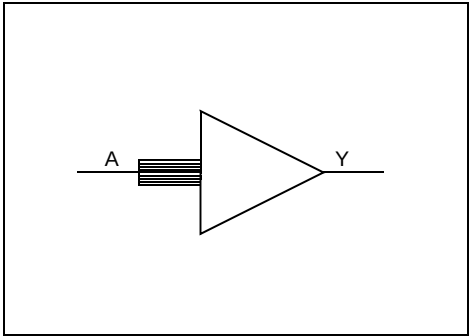
Truth Table

A	Y
0	0
1	1

Family	Modules	
	Seq	Comb
All		1

CLKINT

ACT 2/1200XL, 3200DX, 42MX, 54SX54SX



Function
Internal Clock Interface

Truth Table

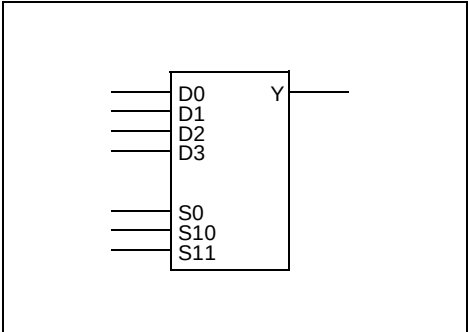
A	Y
0	0
1	1

Input A	Output Y
-------------------	--------------------

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

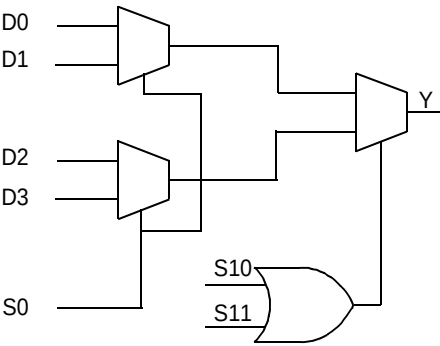
CM7

ACT2/1200XL, ACT 3, 3200DX, 42MXX, 54SX



Input D0, D1, D2, D3, S0, S10, S11	Output y
--	--------------------

Function
Full Combinational Module



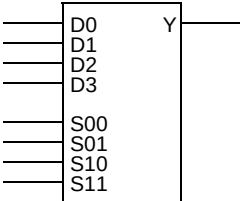
Truth Table

S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

Family	Modules	
	Seq	Comb
All		1

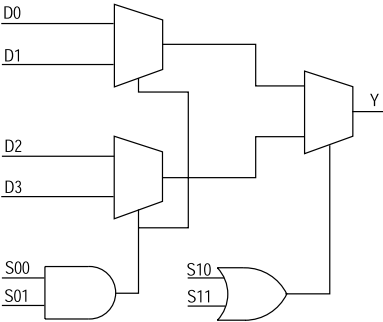
CM8

ACT2/1200XL, ACT 3, 3200DX, 42MXX, 54SX



Function
Full Combinational Module

Input	Output
D0, D1, D2, D3, S00, S01, S10, S11	y



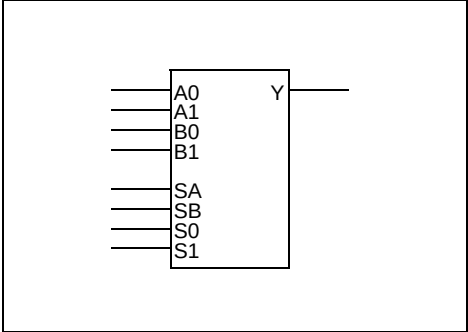
Truth Table

S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All		1

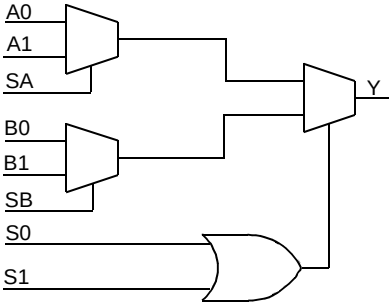
CM8A

Act 1, 40MX



Input	Output
A0, A1, B0, B1, SA, SB, S0, S1	Y

Function
Full Combinational Module



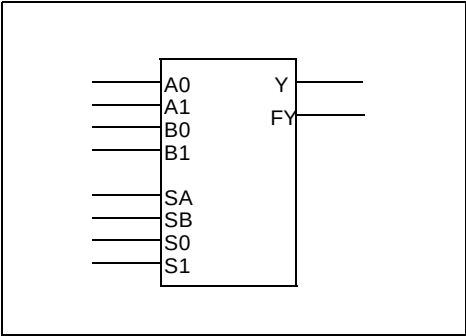
Truth Table

S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

CM8F

54SX

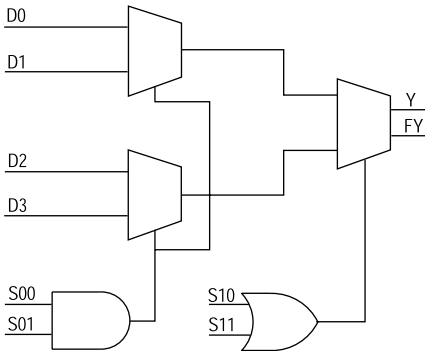


Input
D0, D1, D2, D3, S00,
S01, S10, S11

Output
Y, FY

Function

Full Combinational Module with fast output



Truth Table

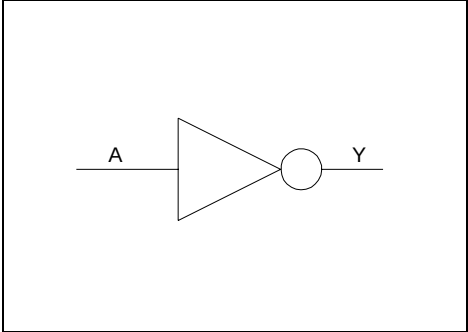
S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
54SX		1

NOTE: FY is a fast output that has a maximum fanout of 1.

CM8INV

54SX



Function
Inverter with active low output

Truth Table

A	Y
0	1
1	0

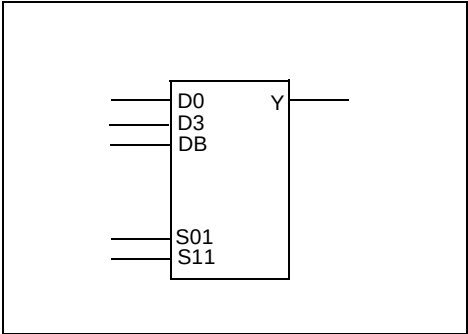
Input	Output
A	Y

Family	Modules	
	Seq	Comb
54SX		0

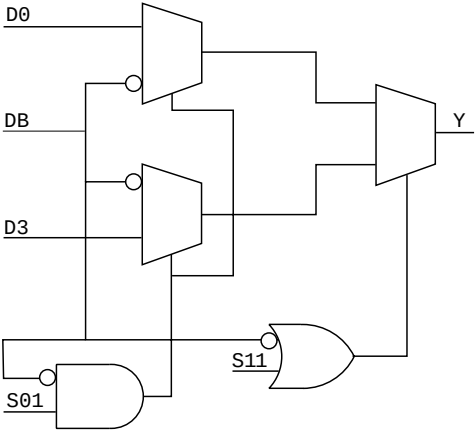
NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module.

CMA9

54SX



Function
Full Combinational Module

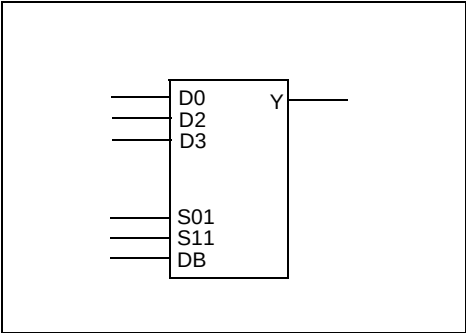


Input	Output
D0, D3, DB, S01, S11	Y

Family	Modules	
	Seq	Comb
54SX		1

CMAF

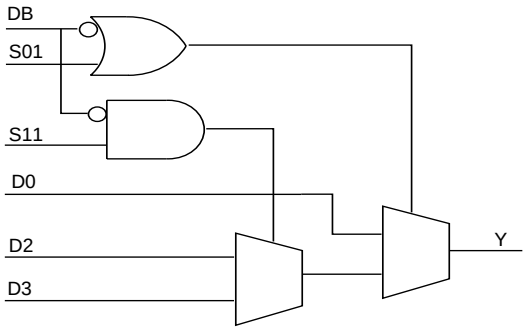
54SX



Input	Output
D0, D3, DB, S01, S11	Y

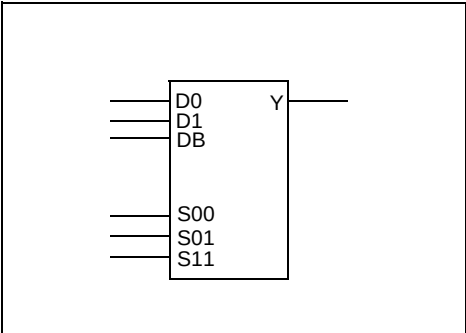
Family	Modules	
	Seq	Comb
54SX		1

Function
Full Combinational Module



CMB3

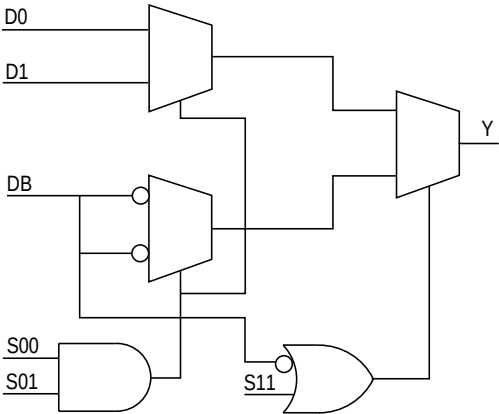
54SX



Input	Output
D0, D1, DB, S00, S01, S11	Y

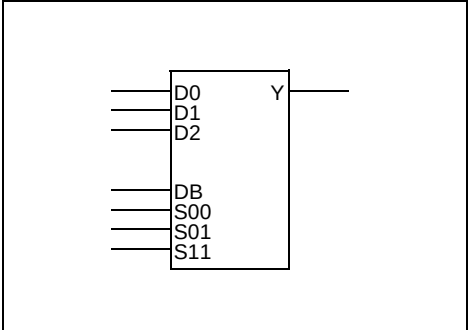
Family	Modules	
	Seq	Comb
54SX		1

Function
Full Combinational Module



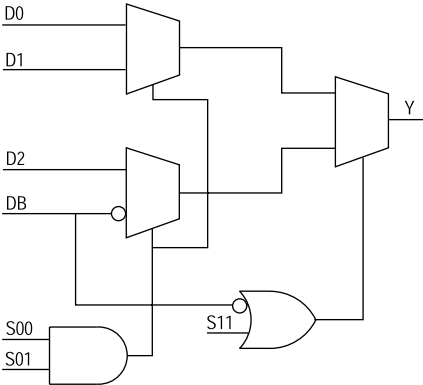
CMB7

54SX



Input	Output
D0, D1, D2, DB, S00, S01, S11	Y

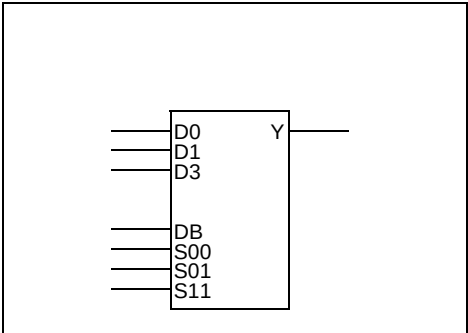
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

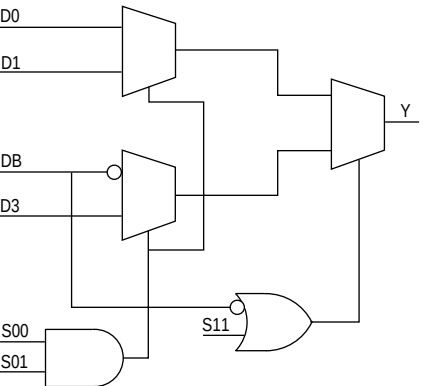
CMBB

54SX



Input	Output
D0, D1, D3, DB, S00, S01, S11	Y

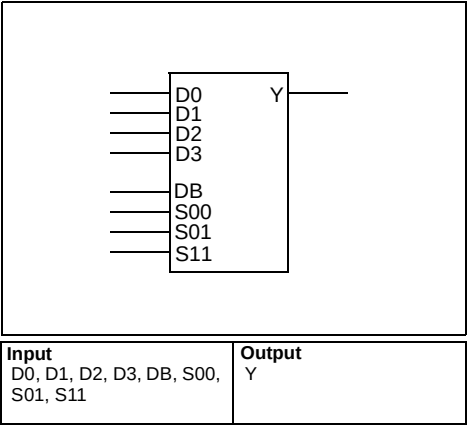
Function
Full Combinational Module



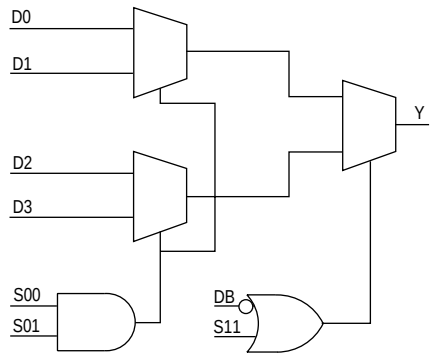
Family	Modules	
	Seq	Comb
54SX		1

CMBF

54SX



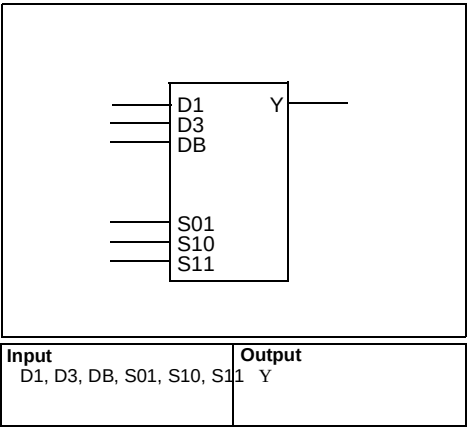
Function
Full Combinational Module



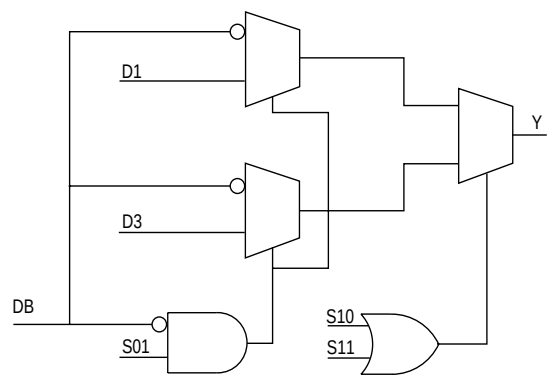
Family	Modules	
	Seq	Comb
54SX		1

CMEA

54SX



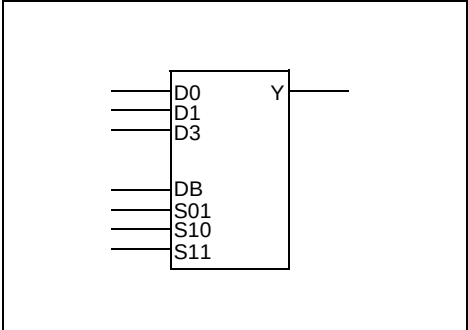
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

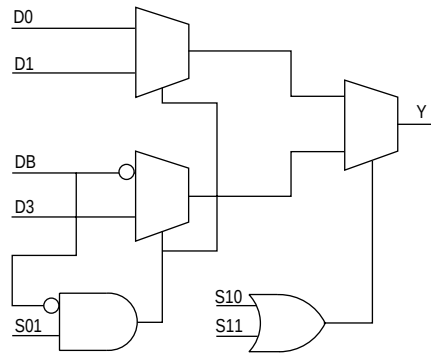
CMEB

54SX



Input	Output
D0, D1, D3, DB, S01, S10, S11	Y

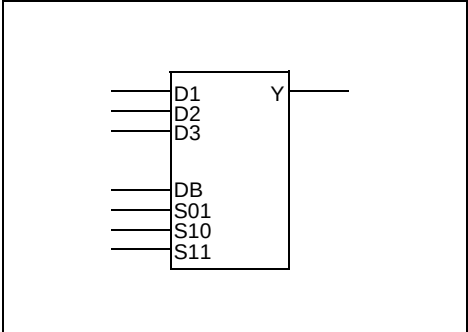
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

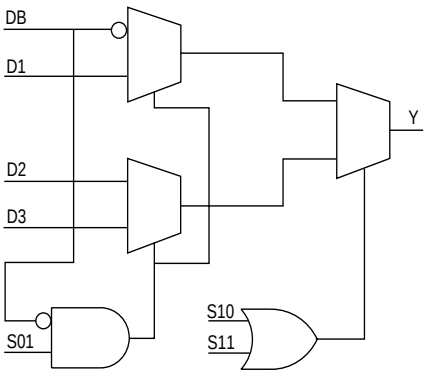
CMEE

54SX



Input	Output
D1, D2, D3, DB, S01, S10, S11	Y

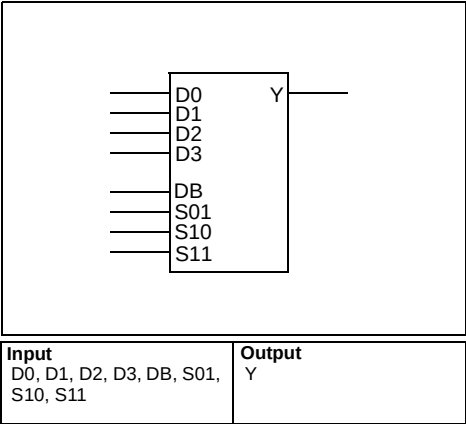
Function
Full Combinational Module



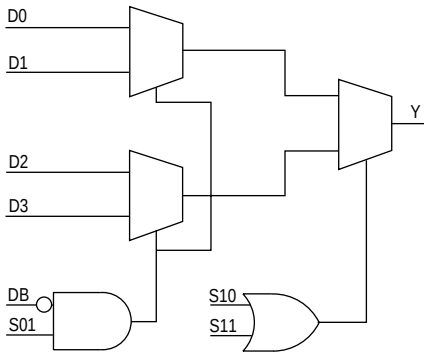
Family	Modules	
	Seq	Comb
54SX		1

CMEF

54SX



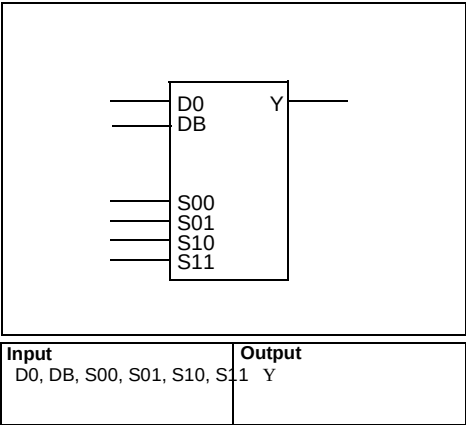
Function
Full Combinational Module



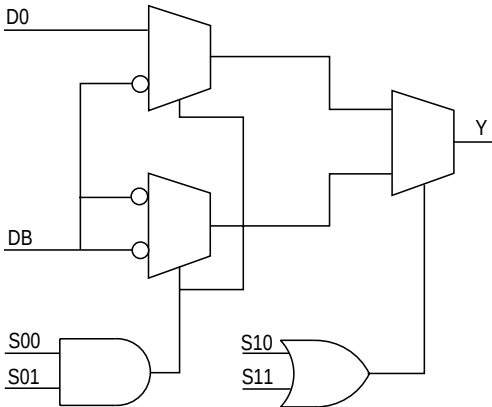
Family	Modules	
	Seq	Comb
54SX		1

CMF1

54SX



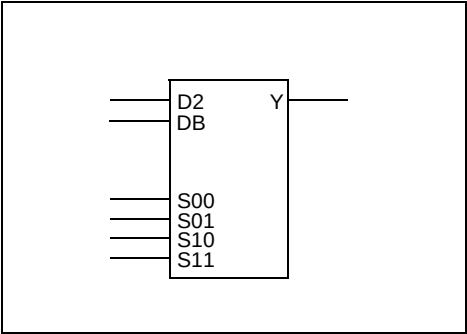
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

CMF4

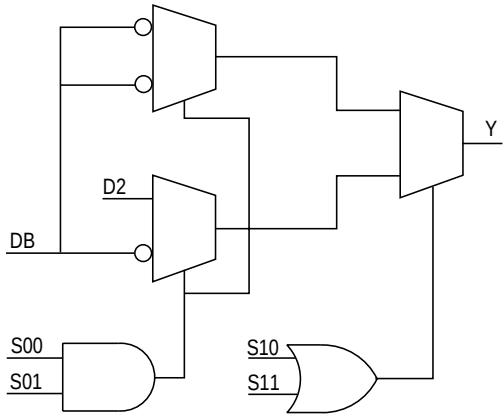
54SX



Input	Output
D2, DB, S00, S01, S10, S11	Y

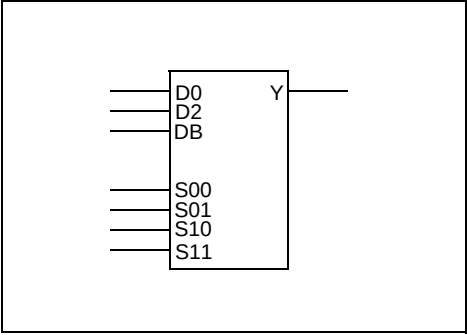
Family	Modules	
	Seq	Comb
54SX		1

Function
Full Combinational Module



CMF5

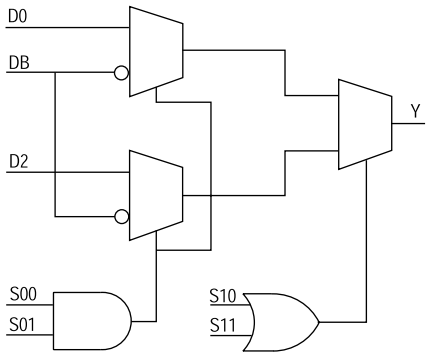
54SX



Input	Output
D0, D2, DB, S00, S01, S10, S11	Y

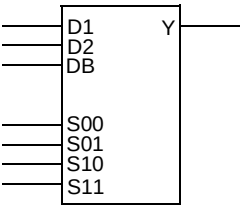
Family	Modules	
	Seq	Comb
54SX		1

Function
Full Combinational Module



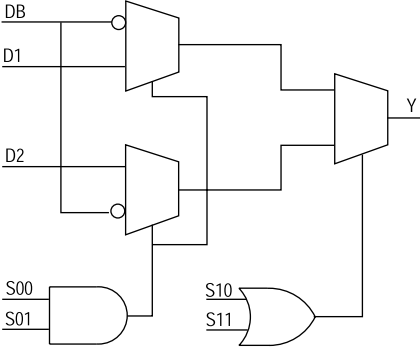
CMF6

54SX



CMF6 module symbol showing inputs D1, D2, DB, S00, S01, S10, S11 and output Y.

Function
Full Combinational Module



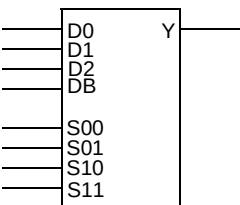
Logic diagram for CMF6 showing internal gates and connections for inputs D1, D2, DB, S00, S01, S10, S11 and output Y.

Input D1, D2, DB, S00, S01, S10, S11	Output Y
--	--------------------

Family	Modules	
	Seq	Comb
54SX		1

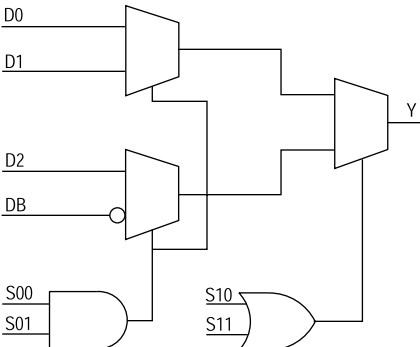
CMF7

54SX



CMF7 module symbol showing inputs D0, D1, D2, DB, S00, S01, S10, S11 and output Y.

Function
Full Combinational Module



Logic diagram for CMF7 showing internal gates and connections for inputs D0, D1, D2, DB, S00, S01, S10, S11 and output Y.

Input D0, D1, D2, DB, S00, S01, S10, S11	Output Y
--	--------------------

Family	Modules	
	Seq	Comb
54SX		1

CMF8

54SX

D3

DB

Y

S00

S01

S10

S11

Input

D3, DB, S00, S01, S10, S11

Output

Y

Family	Modules	
	Seq	Comb
54SX		1

Function

Full Combinational Module

CMF9

54SX

D0

D3

DB

Y

S00

S01

S10

S11

Input

D0, D3, DB, S00, S01, S10, S11

Output

Y

Family	Modules	
	Seq	Comb
54SX		1

Function

Full Combinational Module

CMFA

54SX

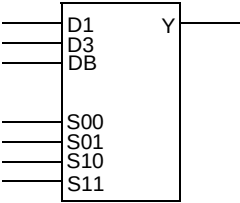
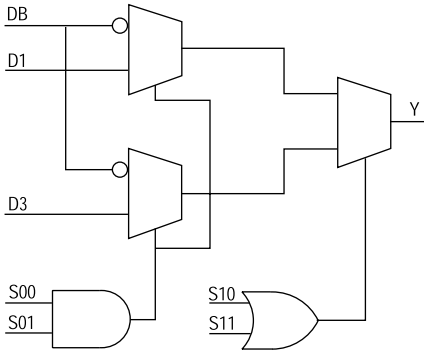


Diagram of the CMFA module symbol. It has four inputs on the left: D1, D3, DB, and DB. It has four inputs on the bottom: S00, S01, S10, and S11. It has one output on the right: Y.

Function
Full Combinational Module



Logic diagram for the CMFA module. It consists of four 2-input AND gates and one 2-input OR gate. The first AND gate has inputs D1 and DB. The second AND gate has inputs D3 and DB. The third AND gate has inputs S00 and S01. The fourth AND gate has inputs S10 and S11. The outputs of the first and second AND gates are connected to the inputs of the OR gate. The output of the OR gate is connected to the output Y.

Input
D1, D3, DB, S00, S01, S10, S11

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

CMFB

54SX

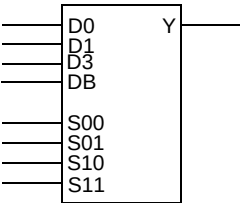
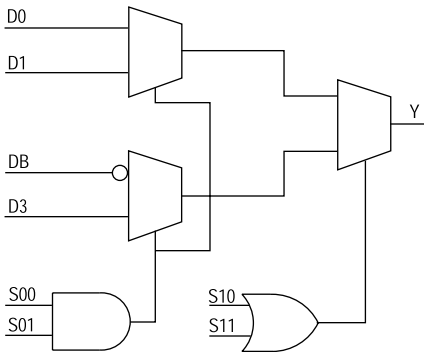


Diagram of the CMFB module symbol. It has four inputs on the left: D0, D1, D3, and DB. It has four inputs on the bottom: S00, S01, S10, and S11. It has one output on the right: Y.

Function
Full Combinational Module



Logic diagram for the CMFB module. It consists of four 2-input AND gates and one 2-input OR gate. The first AND gate has inputs D0 and D1. The second AND gate has inputs D3 and DB. The third AND gate has inputs S00 and S01. The fourth AND gate has inputs S10 and S11. The outputs of the first and second AND gates are connected to the inputs of the OR gate. The output of the OR gate is connected to the output Y.

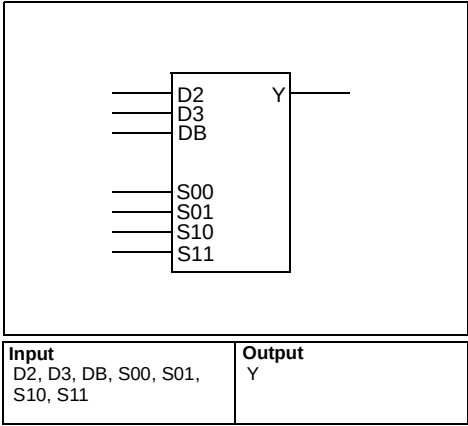
Input
D0, D1, D3, DB, S00, S01, S10, S11

Output
Y

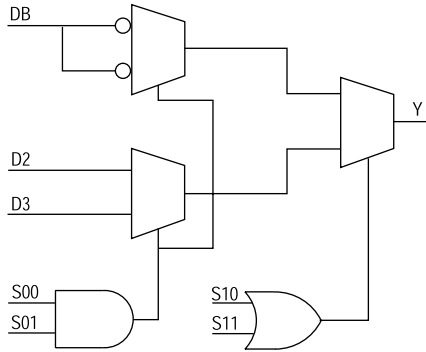
Family	Modules	
	Seq	Comb
54SX		1

CMFC

54SX



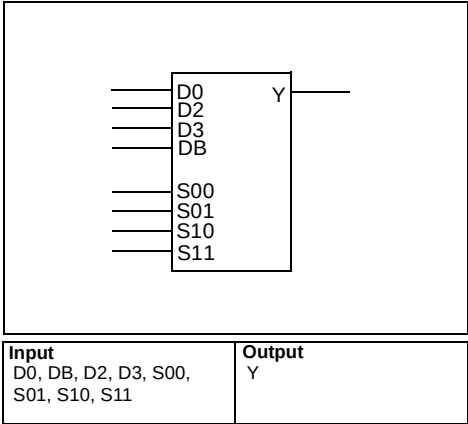
Function
Full Combinational Module



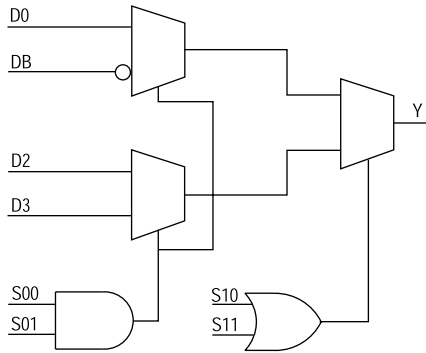
Family	Modules	
	Seq	Comb
54SX		1

CMFD

54SX



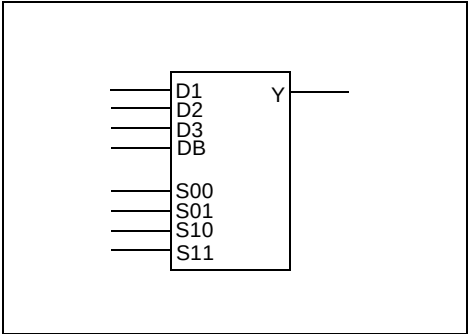
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

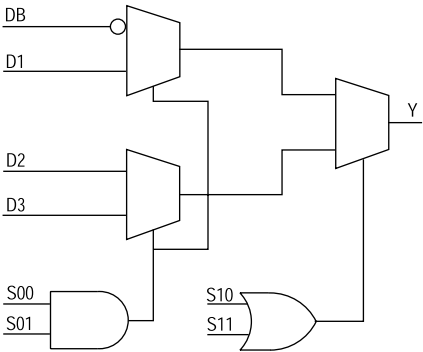
CMFE

54SX



Input	Output
D1, D2, D3, DB, S00, S01, S10, S11	Y

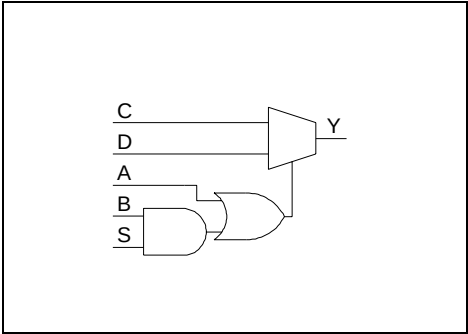
Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

CS1

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Input	Output
A, S, B, C, D	Y

Function
Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

CS2

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX

```
graph LR
    C --- OR1
    D --- OR1
    B --- OR1
    A --- OR1
    OR1 --- AND1
    S --- AND1
    C --- AND1
    AND1 --- Y
```

Function

Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1

Input

A, S, B, C, D

Output

Y

Family	Modules	
	Seq	Comb
All		1

CY2A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX

```
graph LR
    B1 --- OR1
    A1 --- OR1
    B0 --- OR1
    A0 --- OR1
    OR1 --- Y
```

Function

Carry Generator

Truth Table

A1	B1	A0	B0	Y
X	0	X	0	0
X	0	0	X	0
0	0	X	X	0
0	X	X	0	0
0	X	0	X	0
X	1	1	1	1
1	X	1	1	1
1	1	X	X	1

Input

A1, B1, A0, B0

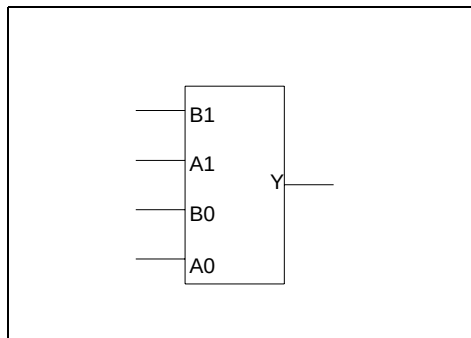
Output

Y

Family	Modules	
	Seq	Comb
All		1

CY2B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
Carry Generator

Truth Table

A1	B1	A0	B0	Y
X	0	0	0	0
0	0	X	X	0
0	X	0	0	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1
1	1	X	X	1

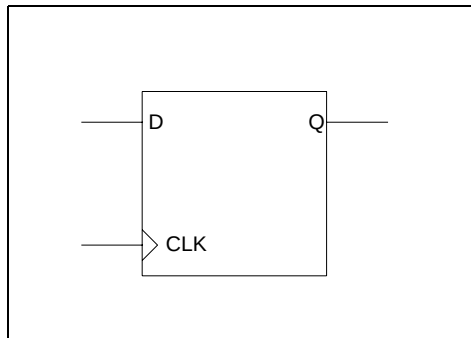
Input
A1, B1, A0, B0

Output
Y

Family	Modules	
	Seq	Comb
All		1

DF1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
D-Type Flip-Flop

Truth Table

CLK	Q_{n+1}
↑	D

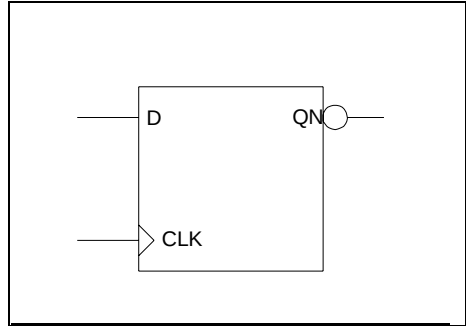
Input
D, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active low Output

Truth Table

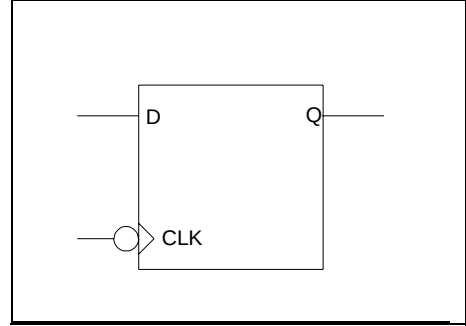
CLK	QN _{n+1}
↑	!D

Input D, CLK	Output QN
-----------------	--------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop with active low Clock

Truth Table

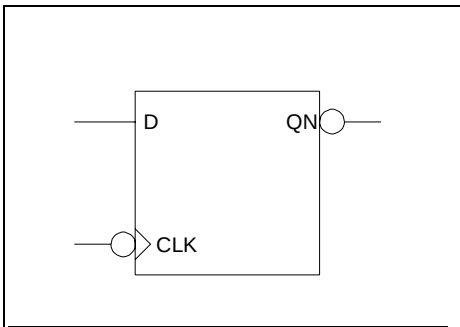
CLK	Q _{n+1}
↓	D

Input D, CLK	Output Q
-----------------	-------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1C

ACT 1, 40MX,



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

CLK	Q_{n+1}
↓	!D

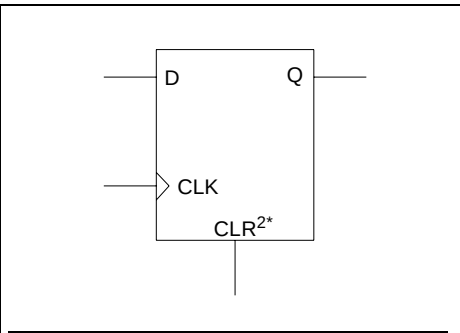
Input
D, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with active high Clear

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↑	D

Input
CLR, D, CLK

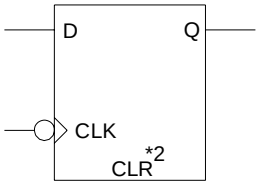
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

DFC1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

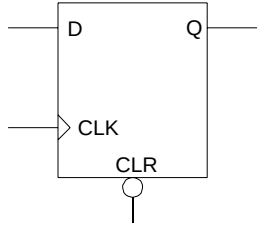
Input CLR, D, CLK	Output Q
----------------------	-------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

DFC1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop, with active low Clear

Truth Table

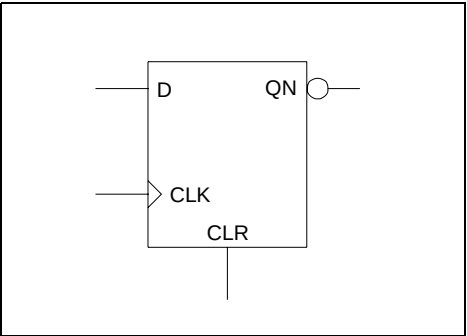
CLR	CLK	Q _{n+1}
0	X	0
1	↑	D

Input CLR, D, CLK	Output Q
----------------------	-------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1C

ACT 1, 40MX



Function
D-Type Flip-Flop, with active high Clear and Clock

Truth Table

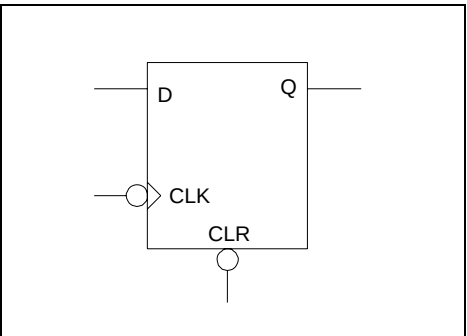
CLR	CLK	Q_{n+1}
1	X	1
0	$\uparrow$	!D

Input CLR, D, CLK	Output QN
-----------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFC1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
D-Type Flip-Flop, with active low Clear and Clock

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	$\downarrow$	D

Input CLR, D, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic symbol for DFC1E D-Type Flip-Flop. Inputs: D, CLK (active low), CLR (active low). Output: QN (active low, with a *2 delay indicator).

Function

D-Type Flip-Flop, with active low Clear and Output

Truth Table

CLR	CLK	Q _N _{n+1}
0	X	1
1	↑	!D

Input

CLR, D, CLK

Output

Q_N

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFC1F

ACT 1, 40MX

Logic symbol for DFC1F D-Type Flip-Flop. Inputs: D, CLK (active low), CLR (active low). Output: QN (active low).

Function

D-Type Flip-Flop, with active high Clear, active low Clock and Output

Truth Table

CLR	CLK	Q _N _{n+1}
1	X	1
0	↓	!D

Input

CLR, D, CLK

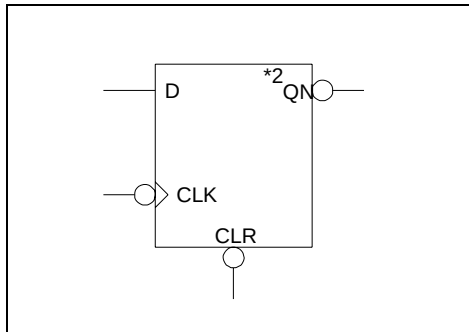
Output

Q_N

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFC1G

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with active low Clear, Clock and Output

Truth Table

CLR	CLK	Q_{n+1}
0	X	1
1	↓	!D

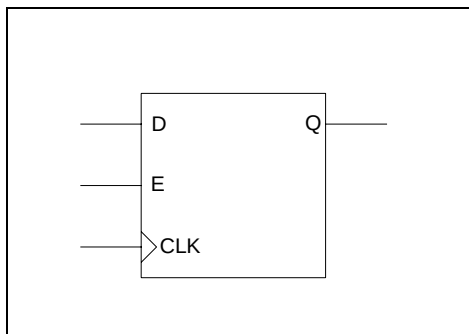
Input	Output
CLR, D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFF

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with active high Enable

Truth Table

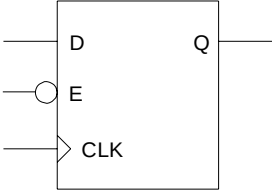
E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Input	Output
D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↑	D

Input

D, E, CLK

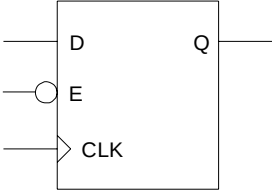
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↓	D

Input

D, E, CLK

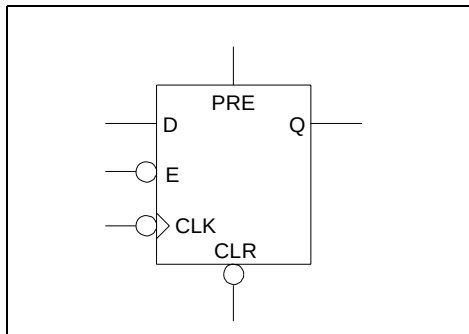
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE2D

ACT 1, 40MX



Function

D-Type Flip-Flop, with active high Preset, active low Enable, Clear, and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Input

CLR, D, E, PRE, CLK

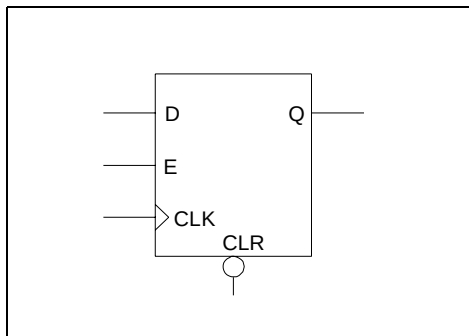
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with Enable and active low Clear

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	0	X	Q
1	1	↑	D

Input

CLR, D, E, CLK

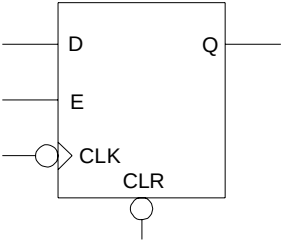
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop, with Enable and active low Clear and Clock

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	0	X	Q
1	1	↓	D

Input

CLR, D, E, CLK

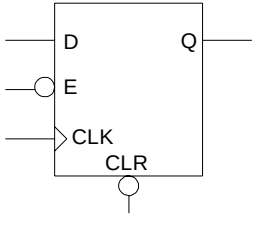
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop, with Enable and active low Clear

Truth Table

CLR	E	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input

CLR, D, E, CLK

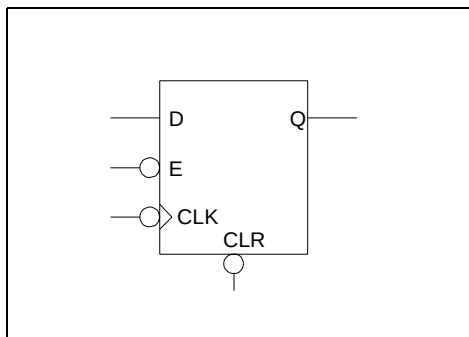
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop, with active low Enable, Clear and Clock

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↓	D

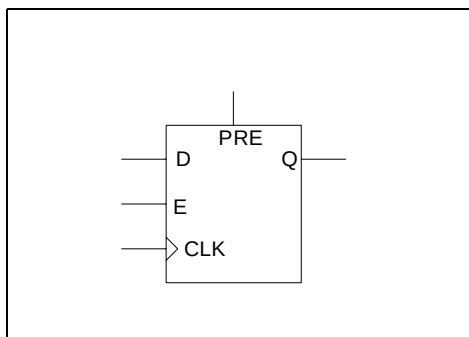
Input
CLR, D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE4

ACT 1, 40MX



Function

D-Type Flip-Flop, with active high Enable and Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↑	D

Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4A

ACT 1, 40MX

Logic diagram of DFE4A D-Type Flip-Flop. Inputs: D, E, PRE, CLK. Output: Q. PRE is active high, CLK is active low.

Function
D-Type Flip-Flop, with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↓	D

Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4B

ACT 1, 40MX

Logic diagram of DFE4B D-Type Flip-Flop. Inputs: D, E, PRE, CLK. Output: Q. PRE is active high, CLK is active low, E is active high.

Function
D-Type Flip-Flop, with active low Enable, and active high Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↑	D

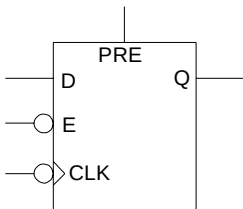
Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4C

ACT 1, 40MX



Function

D-Type Flip-Flop, with active low Enable and Clock, and active high Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↓	D

Input

D, E, PRE, CLK

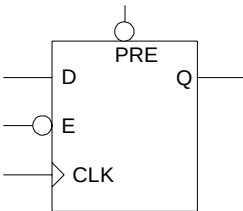
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4F

54SX



Function

D-Type Flip-Flop, with active low Enable, and active low Preset

Truth Table

PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Input

D, E, PRE, CLK

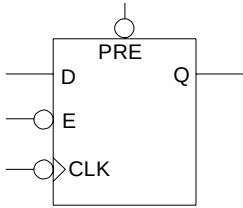
Output

Q

Family	Modules	
	Seq	Comb
54SX	1	

DFE4G

54SX



Function
D-Type Flip-Flop, with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↓	D

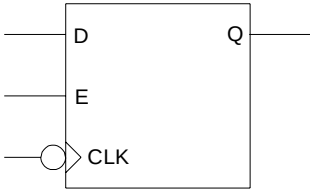
Input
D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
54SX	1	

DFEA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

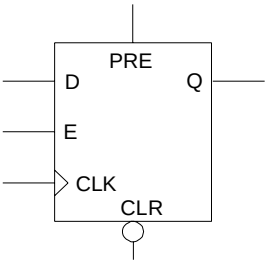
Input
D, E, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFEB

ACT 1, 40MX



Function

D-Type Flip-Flop, with Enable, Preset, and active low Clear

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

Input

CLR, D, E, PRE, CLK

Output

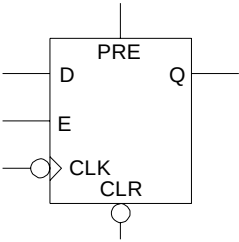
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

*Your design should not allow both PRE and CLR to be asserted at the same time.

DFEC

ACT 1, 40MX



Function

D-Type Flip-Flop, with Enable, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

Input

CLR, D, E, PRE, CLK

Output

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFED

ACT 1, 40MX

Logic symbol for DFED D-Type Flip-Flop. Inputs: D, E (active low), CLK, CLR (active low). Output: Q. PRE is also shown as an input.

Function
D-Type Flip-Flop, with active low Enable and Clear, and active high Preset

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↑	D
0	1	X	X	*

Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFEG

54SX

Logic symbol for DFEG D-Type Flip-Flop. Inputs: D, E (active low), CLK, CLR (active low). Output: Q. PRE is also shown as an input.

Function
D-Type Flip-Flop with Enable and active low Preset Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	1	Q
1	1	0	↑	D

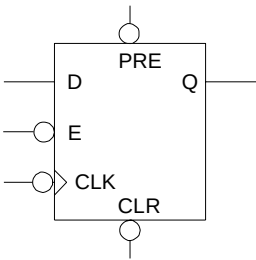
Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
54SX	1	

DFEH

54SX



Function

D-Type Flip-Flop with active low Enable and Clear and Pre-set

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

Input

CLR, D, E, PRE, CLK

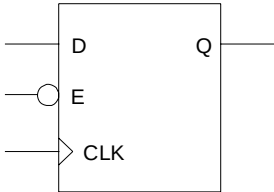
Output

Q

Family	Modules	
	Seq	Comb
54SX	1	

IODFE

ACT 3



Function

D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↑	D

Input

D, E, CLK

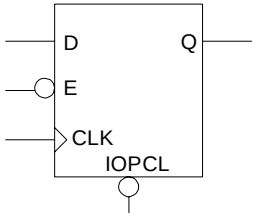
Output

Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.
NOTE 2: Uses an I/O module.

IODFEC

ACT 3



The diagram shows a D-Type Flip-Flop with inputs D, E (active low), and CLK. The output is Q. The IOPCL pin is shown as an active low input (bubble) connected to the bottom of the flip-flop block.

Function

D-Type Flip-Flop, with active low Enable and Clear

Truth Table

IOPCL	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Input

IOPCL, D, E, CLK

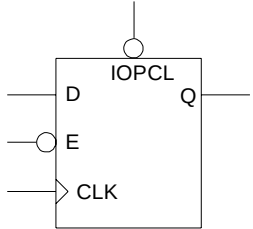
Output

Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.
NOTE 2: Uses an I/O module.

IODFEP

ACT 3



The diagram shows a D-Type Flip-Flop with inputs D, E (active low), and CLK. The output is Q. The IOPCL pin is shown as an active low input (bubble) connected to the top of the flip-flop block.

Function

D-Type Flip-Flop, with active low Enable and Preset

Truth Table

IOPCL	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Input

IOPCL, D, E, CLK

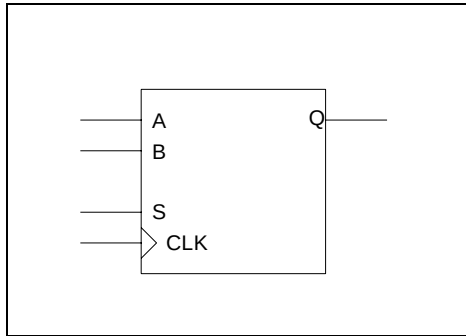
Output

Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

DFM

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Input

A, B, S, CLK

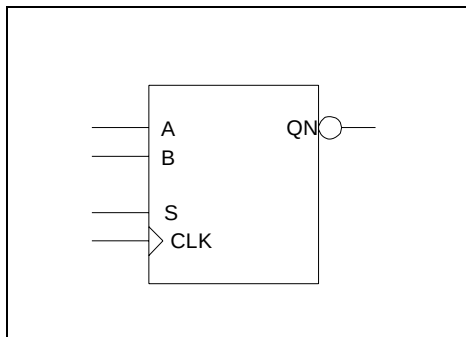
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM1B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

Input

A, B, S, CLK

Output

QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM1C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic diagram of DFM1C: A D-Type Flip-Flop with 2-input Multiplexed Data (A, B), Set (S), and Clock (CLK) inputs. The output is QN.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

S	CLK	QN _{n+1}
0	↓	!A
1	↓	!B

Input
A, B, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM3

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX

Logic diagram of DFM3: A D-Type Flip-Flop with 2-input Multiplexed Data (A, B), Set (S), Clock (CLK), and Clear (CLR) inputs. The output is Q. CLR is active high.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear

Truth Table

CLR	S	CLK	Q _{n+1}
0	0	↑	A
0	1	↑	B

Input
A, B, CLR, S, CLK

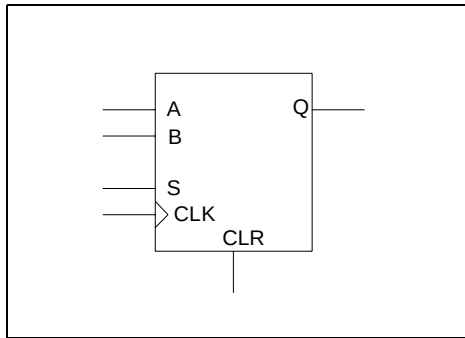
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX

DFM3B

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↓	A
1	1	↓	B

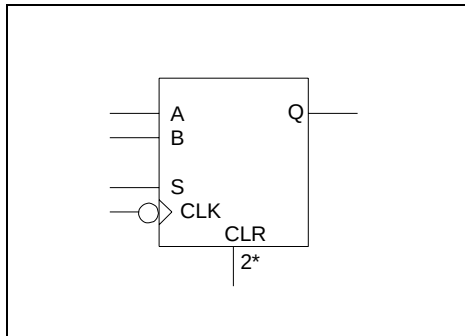
Input
A, B, CLR, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM3E

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

Truth Table

CLR	S	CLK	Q_{n+1}
1	X	X	0
0	0	↓	A
0	1	↓	B

Input
A, B, CLR, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX

DFM3F

ACT 1, 40MX

Logic diagram of DFM3F: A D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output. Inputs: A, B, S, CLK, CLR. Output: QN.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output

Truth Table

CLR	S	CLK	Q _{N+1}
1	X	X	1
0	0	↑	!A
0	1	↑	!B

Input
A, B, CLR, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

DFM3G

ACT 1, 40MX

Logic diagram of DFM3G: A D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output. Inputs: A, B, S, CLK, CLR. Output: QN.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output

Truth Table

CLR	S	CLK	Q _{N+1}
1	X	X	1
0	0	↓	!A
0	1	↓	!B

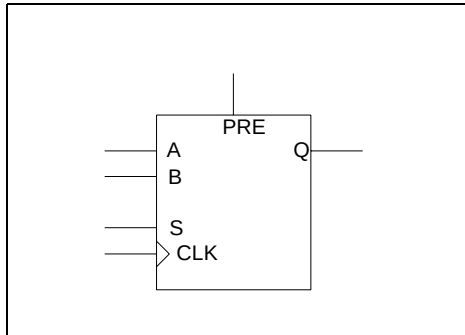
Input
A, B, CLR, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

DFM4

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

Truth Table

PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↑	A
0	1	↑	B

Input

A, B, PRE, S, CLK

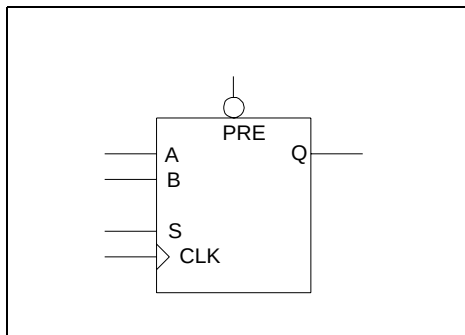
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

DFM4A

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↑	A
1	1	↑	B

Input

A, B, PRE, S, CLK

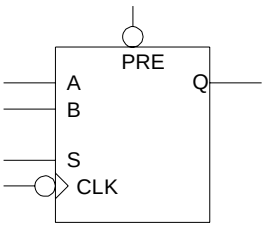
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

DFM4B

ACT 1, 40MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	$\uparrow$	A
1	1	$\uparrow$	B

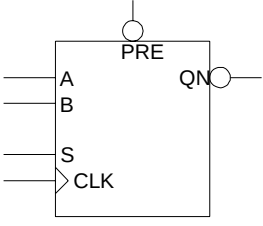
Input
A, B, PRE, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

DFM4C

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

Truth Table

PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	$\uparrow$	!A
1	1	$\uparrow$	!B

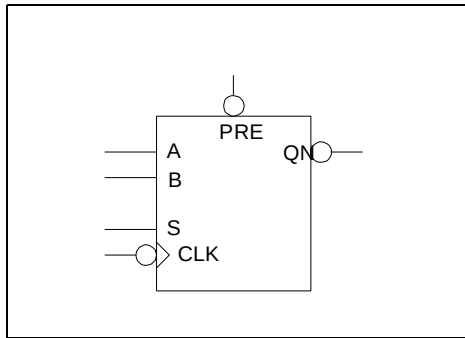
Input
A, B, PRE, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM4D

ACT 1, ACT2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	0
1	0	↓	!A
1	1	↓	!B

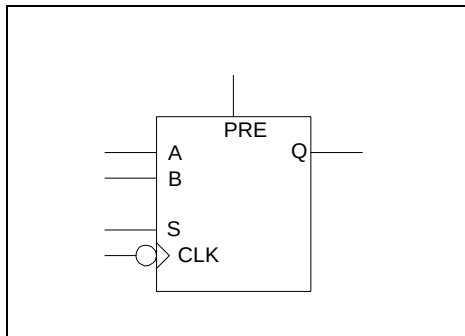
Input
A, B, PRE, S, CLK

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFM4E

ACT 1, 40MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

Truth Table

PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↓	A
0	1	↓	B

Input
A, B, PRE, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM5A

ACT 1, 40MX

Logic diagram of DFM5A D-Type Flip-Flop. Inputs: A, B, S, CLK, CLR, PRE. Output: Q. CLR is active low.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

Truth Table

CLR	PRE	S	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↑	A
1	0	1	↑	B
0	1	X	X	*

Input
A, B, CLR, PRE, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM5B

ACT 1, 40MX

Logic diagram of DFM5B D-Type Flip-Flop. Inputs: A, B, S, CLK, CLR, PRE. Output: Q. CLR is active low.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	S	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↓	A
1	0	1	↓	B
0	1	X	X	*

Input
A, B, CLR, PRE, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM6A

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Logic diagram of DFM6A: A D-Type Flip-Flop with 4-input Multiplexed Data. Inputs: D0, D1, D2, D3 (multiplexed data), S0, S1 (set inputs), CLK (clock), CLR (active low clear). Output: Q.

Input

D0, D1, D2, D3, S0, S1, CLK, CLR

Output

Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

CLR	S1	S0	CLK	Q _{n+1}
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

Family	Modules	
	Seq	Comb
All	1	

DFM6B

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Logic diagram of DFM6B: A D-Type Flip-Flop with 4-input Multiplexed Data. Inputs: D0, D1, D2, D3 (multiplexed data), S0, S1 (set inputs), CLK (clock), CLR (active low clear). Output: Q.

Input

D0, D1, D2, D3, S0, S1, CLK, CLR

Output

Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

Truth Table

CL R	S1	S0	CL K	Q _{n+1}
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Family	Modules	
	Seq	Comb
All	1	

DFM7A

ACT 2/1200XL, ACT 3, 3200DX, 42MX

Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

CL R	S1 1	S1 0	S 0	CL K	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

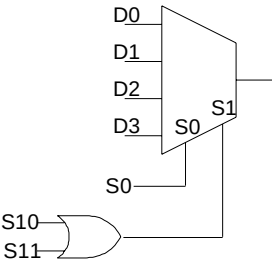
Input
D0, D1, D2, D3, S0, S10, S11, CLK, CLR

Output
Q

Family	Modules	
	Seq	Comb
All	1	

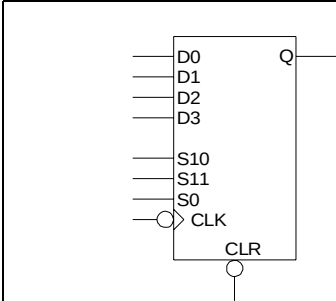
NOTE 1: The DFM7A macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM7B

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

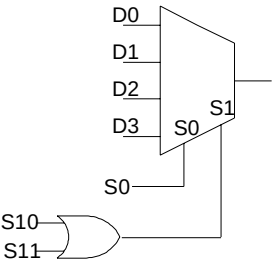
Truth Table

CL R	S1 1	S1 0	S 0	CL K	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Input D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Output Q
---	--------------------

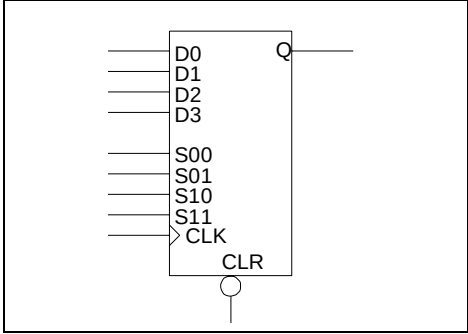
Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM7B macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8A

ACT 3



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

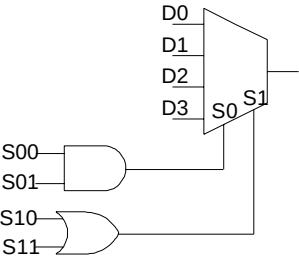
CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2

Input D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Output Q
--	--------------------

Family	Modules	
	Seq	Comb
All	1	

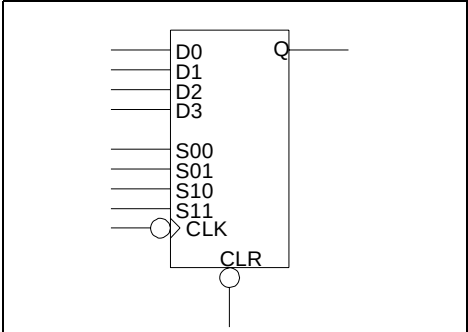
NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8B

ACT 3



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

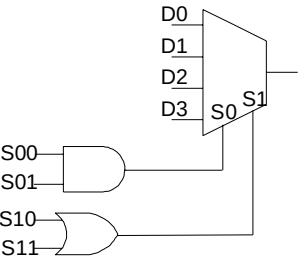
Truth Table

CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2

Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Q

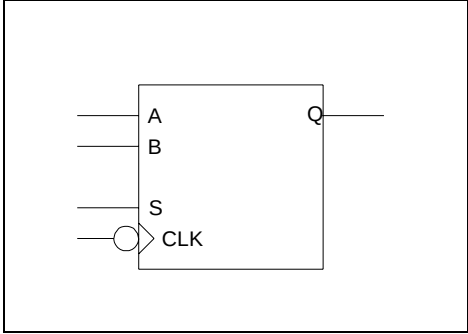
Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM8B macro represents the full ACT 3 S-Module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFMA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



The logic diagram shows a square block representing the flip-flop. On the left side, there are four input lines: two for data inputs A and B, one for the set input S, and one for the clock input CLK. The CLK input is connected to a circle with a triangle pointing into the block, indicating an active-low clock. On the right side, there is one output line labeled Q.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q_{n+1}
0	↓	A
1	↓	B

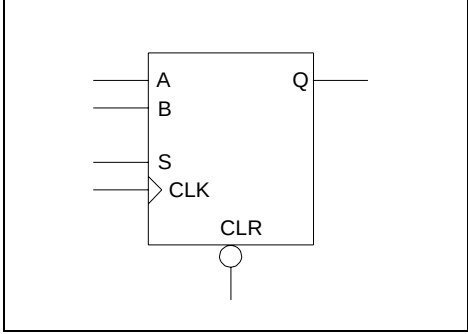
Input
A, B, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFMB

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



The logic diagram shows a square block representing the flip-flop. On the left side, there are four input lines: two for data inputs A and B, one for the set input S, and one for the clock input CLK. The CLK input is connected to a circle with a triangle pointing into the block, indicating an active-low clock. On the bottom side, there is one input line labeled CLR, connected to a circle with a triangle pointing into the block, indicating an active-low clear. On the right side, there is one output line labeled Q.

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear

Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

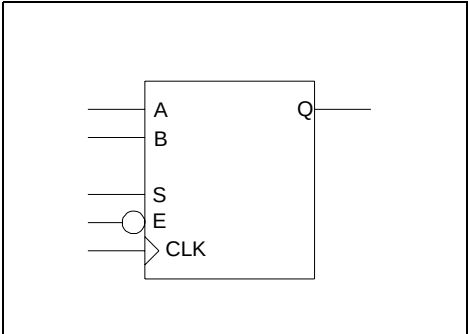
Input
A, B, CLR, S, CLK

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFME1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

Truth Table

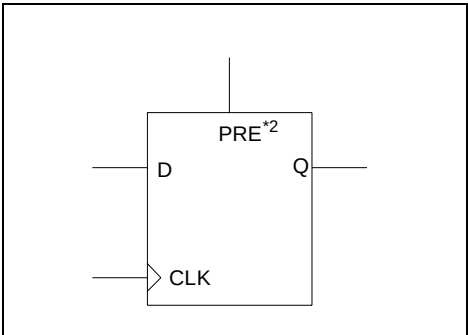
E	S	CLK	Q_{n+1}
1	X	X	Q
0	0	$\uparrow$	A
0	1	$\uparrow$	B

Input A, B, S, E, CLK	Output Q
---------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFP1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	$\uparrow$	D

Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

DFP1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↓	D

Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

DFP1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

Function
D-Type Flip-Flop with active low Preset

Truth Table

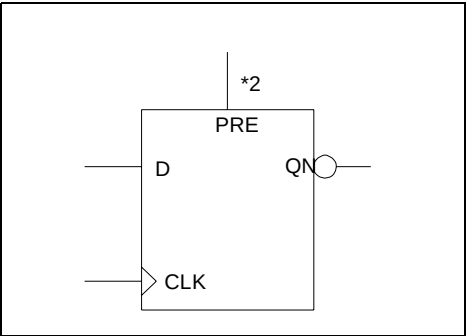
PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

Input	Output
D, PRE, CLK	Q

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

DFP1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active high Preset, and active low Output

Truth Table

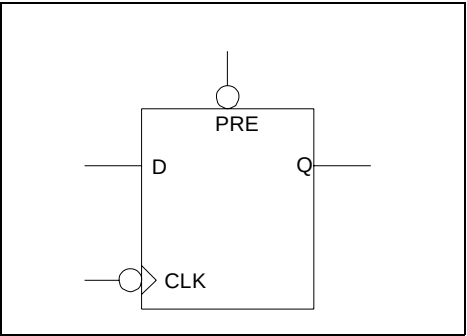
PRE	CLK	QN _{n+1}
1	X	0
0	↑	!D

Input D, PRE, CLK	Output QN
-----------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

DFP1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

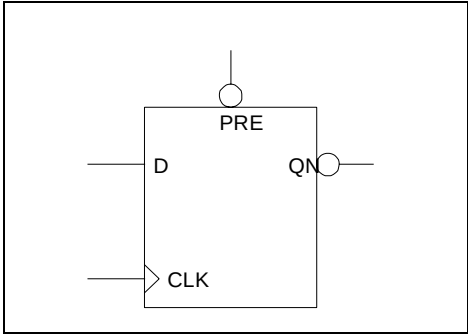
PRE	CLK	Q _{n+1}
0	X	1
1	↓	D

Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

DFP1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active low Preset and Output

Truth Table

PRE	CLK	Q _N _{n+1}
0	X	0
1	↑	!D

Input

D, PRE, CLK

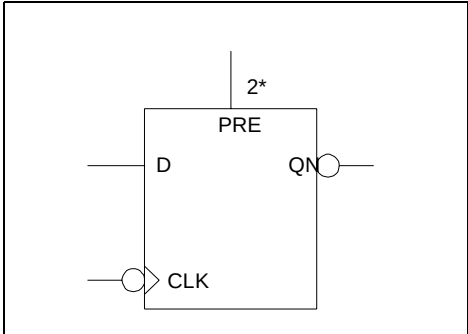
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFP1F

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active high Preset, and active low Clock and Output

Truth Table

PRE	CLK	Q _N _{n+1}
1	X	0
0	↓	!D

Input

D, PRE, CLK

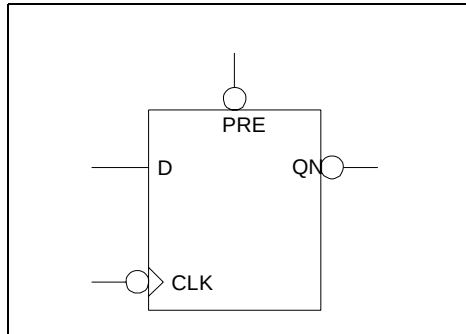
Output

QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	1

DFP1G

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

D-Type Flip-Flop with active high Preset, and active low Clock and Output

Truth Table

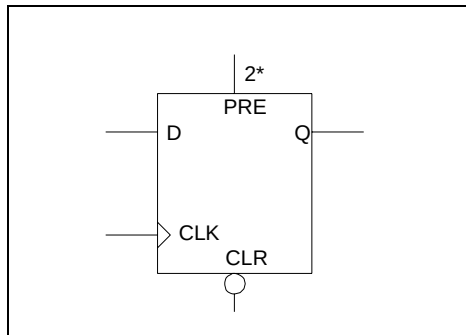
PRE	CLK	QN _{n+1}
1	X	0
0	↓	!D

Input
D, PRE, CLK**Output**
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others	1	

DFPC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

Input
CLR, D, PRE, CLK**Output**
Q

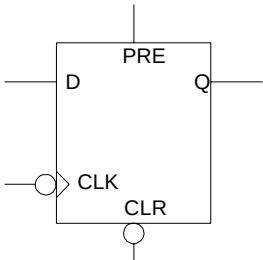
Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.

** In ACT 1/40MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DFPCA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Input

CLR, D, PRE, CLK

Output

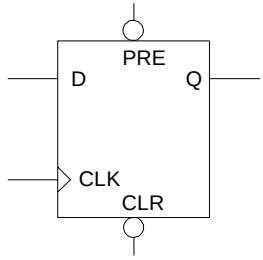
Q

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFPCB

54SX



Function

D-Type Flip-Flop, with active low Clear, and Preset

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	X	X	0
1	0	X	1
1	1	↑	D

Input

CLR, D, E, PRE, CLK

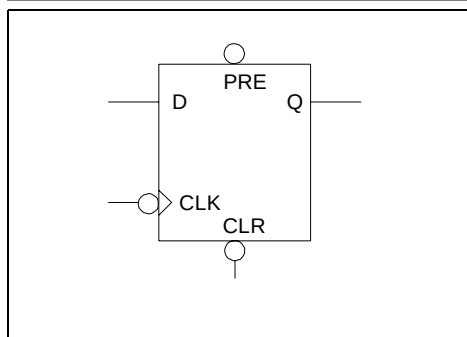
Output

Q

Family	Modules	
	Seq	Comb
54SX	1	

DFPCC

54SX



Function

D-Type Flip-Flop, with active low Preset, Clear and Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↓	D

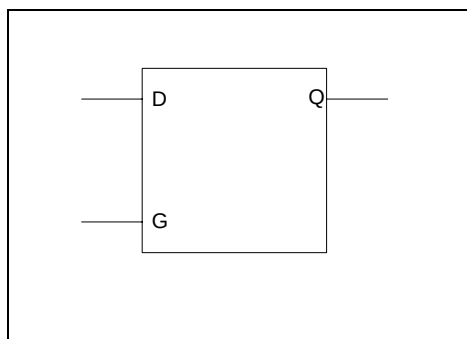
Input
CLR, D, E, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
54SX	1	

DL1

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch

Truth Table

G	Q_{n+1}
0	Q
1	D

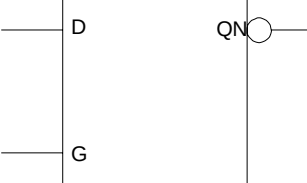
Input
D, G

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
54SX		1
Others	1	

DL1A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX



Function

Data Latch, with active low Output

Truth Table

G	QN _{n+1}
0	QN
1	!D

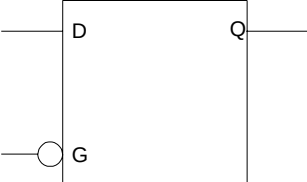
Input
D, G

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DL1B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch, with active low Clock

Truth Table

G	Q _{n+1}
1	Q
0	D

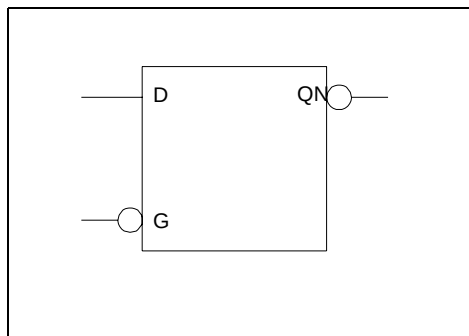
Input
D, G

Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
54SX		1
Others	1	

DL1C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

**Function**

Data Latch, with active low Clock and Output

Truth Table

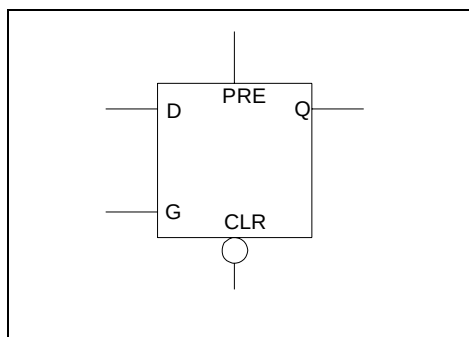
G	QN_{n+1}
1	QN
0	!D

Input
D, G**Output**
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DL2A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX

**Function**

Data Latch with active low Clear, and active high Preset

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

Input
CLR, D, G, PRE**Output**
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has

DL2B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

Function
Data Latch with active high Clear, and active low Preset, Clock and Output

Truth Table

CLR	PRE	G	QN _{n+1}
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

Input
CLR, D, G, PRE

Output
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time.

DL2C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX

Function
Data Latch with active low Clear, active high Preset, and active low Clock

Truth Table

CLR	PRE	G	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

Input
CLR, D, G, PRE

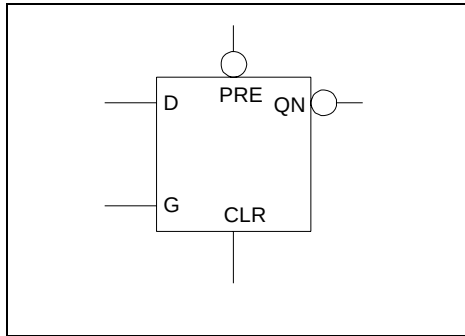
Output
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has

DL2D

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

**Function**

Data Latch with active high Clear, and active low Preset, and Output

Truth Table

CLR	PRE	G	Q_{n+1}
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	!D
1	0	X	*

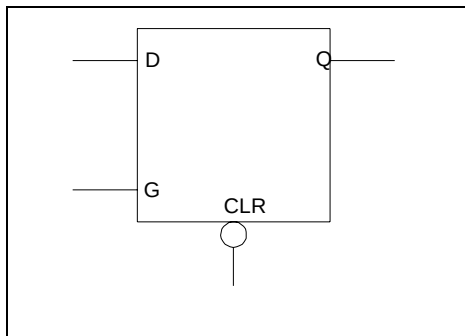
Input
CLR, D, G, PRE**Output**
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has

DLC

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX

**Function**

Data Latch with active low Clear

Truth Table

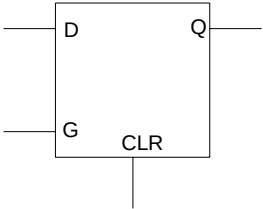
CLR	G	Q_{n+1}
0	X	0
1	0	Q
1	1	D

Input
CLR, D, G**Output**
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
54SX		1
Others	1	

DLC1

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch with active high Clear

Truth Table

CLR	G	Q _{n+1}
1	X	0
0	0	Q
0	1	D

Input

CLR, D, G

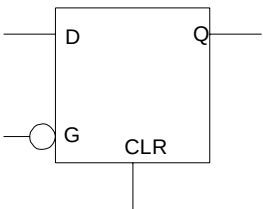
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLC1A

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch with active high Clear, and active low Clock

Truth Table

CLR	G	Q _{n+1}
1	X	0
0	1	Q
0	0	D

Input

CLR, D, G

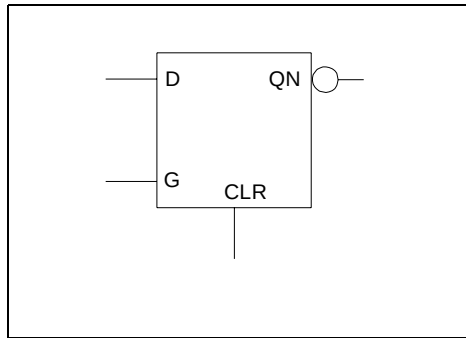
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLC1F

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

**Function**

Data Latch with active high Clear, and active low Output

Truth Table

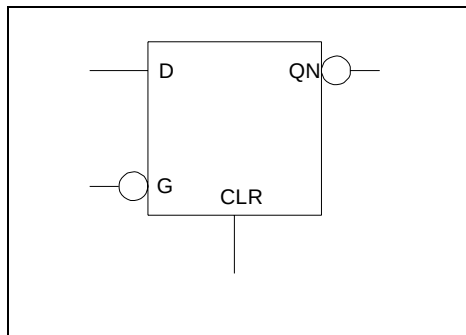
CLR	G	QN_{n+1}
1	X	1
0	0	QN
0	1	!D

Input CLR, D, G	Output QN
---------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

DLC1G

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

**Function**

Data Latch with active high Clear, and active low Clock and Output

Truth Table

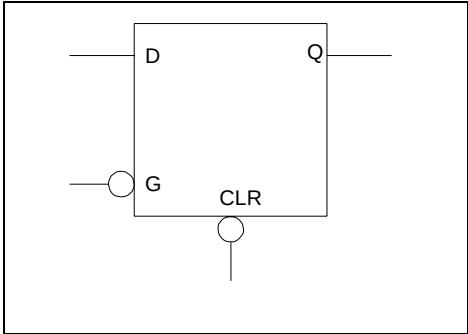
CLR	G	QN_{n+1}
1	X	1
0	1	QN
0	0	!D

Input CLR, D, G	Output QN
---------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

DLCA

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function
Data Latch with active low Clear and Clock

Truth Table

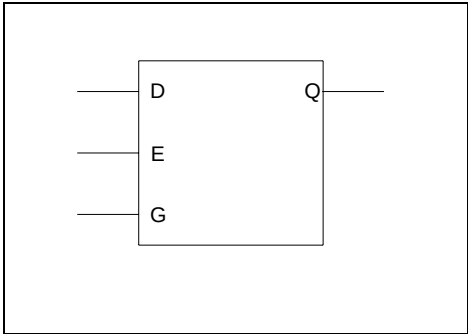
CLR	G	Q _{n+1}
0	X	0
1	1	Q
1	0	D

Input CLR, D, G	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
54SX		1
Others	1	

DLE

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX



Function
Data Latch with active high Enable

Truth Table

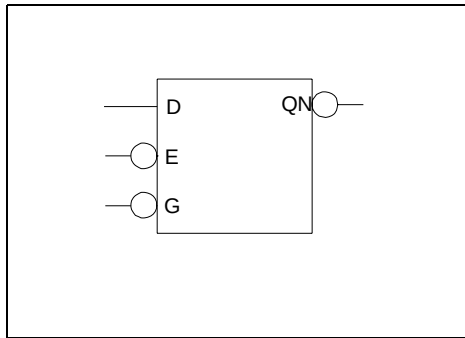
E	G	Q _{n+1}
0	X	Q
X	0	Q
1	1	D

Input D, E, G	Output Q
-------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLE1D

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX

**Function**

Data Latch with active low Enable and Clock, and active low Output

Truth Table

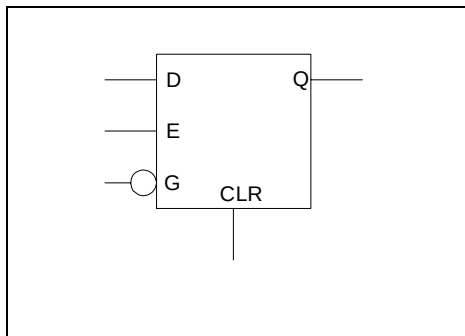
E	G	Q_{n+1}
1	X	Q_n
X	1	Q_n
0	0	$\neg D$

Input	Output
D, E, G	Q_n

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLE2A

ACT 1, 40MX

**Function**

Data Latch with active high Enable and Clear, and active low Clock

Truth Table

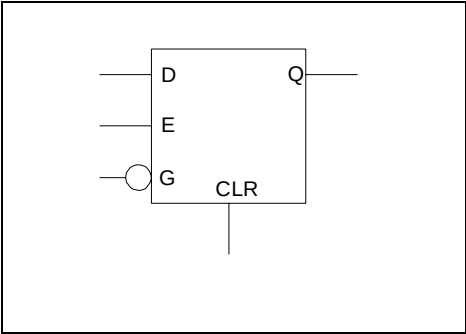
CLR	E	G	Q_{n+1}
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	$\neg D$

Input	Output
CLR, D, E, G	Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1

DLE2B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX



Function
Data Latch with active low Enable, Clear and Clock

Truth Table

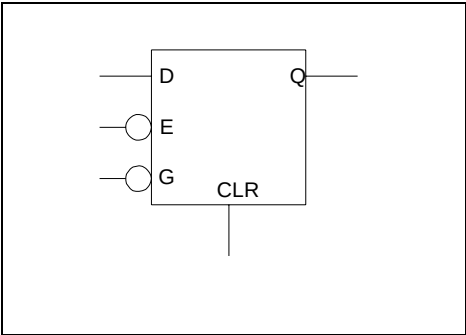
CLR	E	G	Q_{n+1}
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

Input CLR, D, E, G	Output Q
------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLE2C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function
Data Latch with active low Enable and Clock, and active high Clear

Truth Table

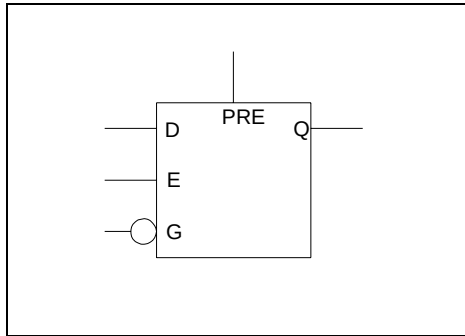
CLR	E	G	Q_{n+1}
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Input CLR, D, E, G	Output Q
------------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

DLE3A

ACT 1, 40MX

**Function**

Data Latch with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	G	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Input

D, E, G, PRE

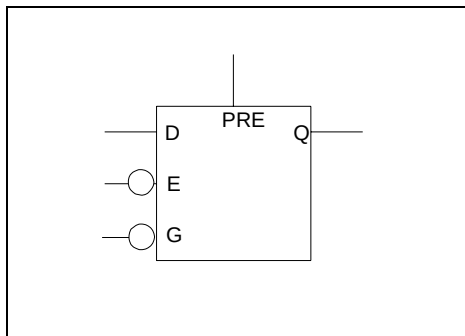
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1

DLE3B

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX

**Function**

Data Latch with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	G	Q_{n+1}
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

Input

D, E, G, PRE

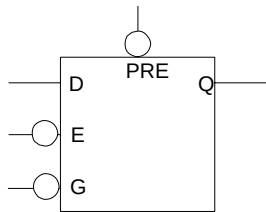
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLE3C

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch with active low Enable, Preset and Clock

Truth Table

PRE	E	G	Q_{n+1}
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

Input

D, E, G, PRE

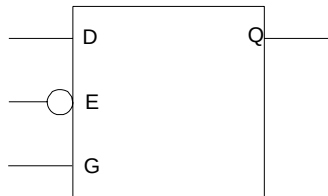
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLEA

ACT 1, ACT 2/1200XL, ACT3, 3200DX, 40MX, 42MX



Function

Data Latch with active low Enable and active high Clock

Truth Table

E	G	Q_{n+1}
1	X	Q
X	0	Q
0	1	D

Input

D, E, G

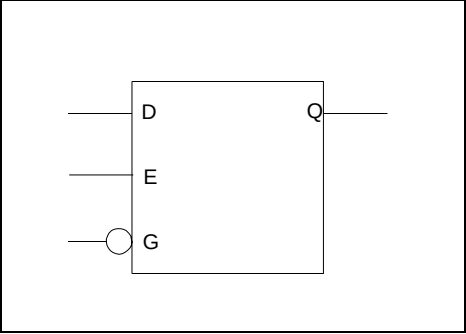
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLEB

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

Data Latch with active low Enable, and active high Clock

Truth Table

E	G	Q _{n+1}
0	X	Q
X	1	Q
1	0	D

Input

D, E, G

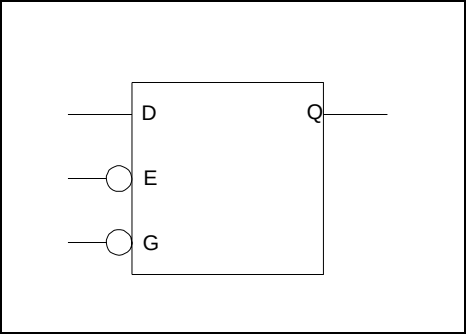
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLEC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

Data Latch with active low Enable, and Clock

Truth Table

E	G	Q _{n+1}
1	X	Q
X	1	Q
0	0	D

Input

D, E, G

Output

Q

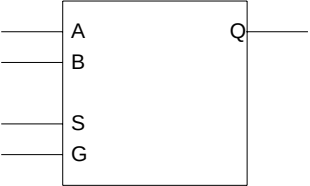
Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

Macro Library Guide

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DLM

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
Data Latch with 2-input Multiplexed Data

Truth Table

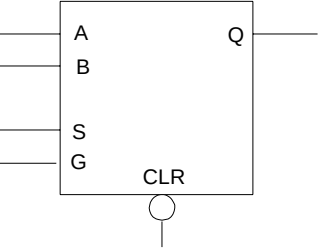
S	G	Q_{n+1}
X	0	Q
0	1	A
1	1	B

Input A, B, S, G	Output Q
----------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLM2

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
Data Latch with 2-input Multiplexed Data and Active-Low Clear

Truth Table

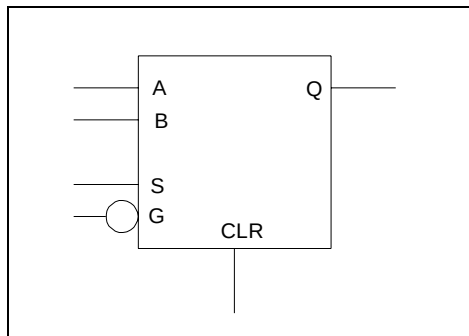
CLR	S	G	Q_{n+1}
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Input A, B, S, G, CLR	Output Q
---------------------------------	--------------------

Family	Modules	
	Seq	Comb
All	1	

DLM2A

ACT 1, 40MX

**Function**

Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

Truth Table

CLR	S	G	Q_{n+1}
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Input

A, B, CLR, S, G

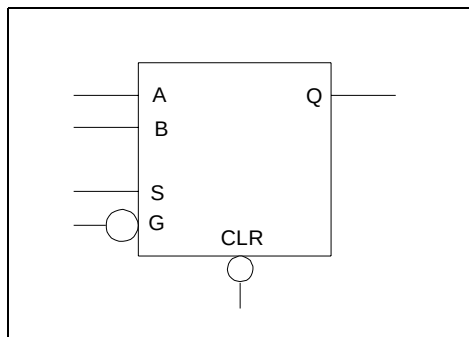
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1

DLM2B

ACT 2/1200XL, ACT 3, 3200DX, 42MX

**Function**

Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

Truth Table

CLR	S	G	Q_{n+1}
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

Input

A, B, CLR, S, G

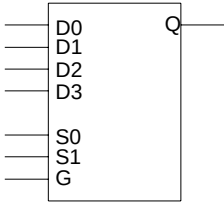
Output

Q

Family	Modules	
	Seq	Comb
All	1	

DLM3

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Data Latch with 4-input Multiplexed Data

Truth Table

S1	S0	G	Q _{n+1}
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

Input

D0, D1, D2, D3, S0, S1, G

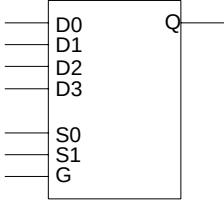
Output

Q

Family	Modules	
	Seq	Comb
All	1	

DLM3A

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Data Latch with 4-input Multiplexed Data, and active low Clock

Truth Table

S1	S0	G	Q _{n+1}
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

Input

D0, D1, D2, D3, S0, S1, G

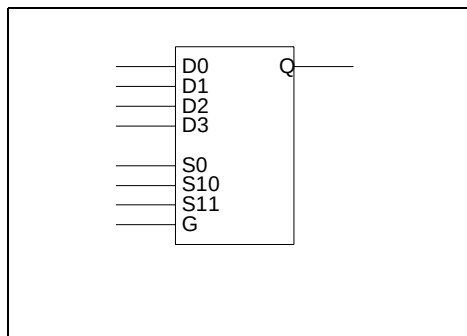
Output

Q

Family	Modules	
	Seq	Comb
All	1	

DLM4

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Input
D0, D1, D2, D3, S0, S10,
S11, G

Output
Q

Function

Data Latch with 4-input Multiplexed Data

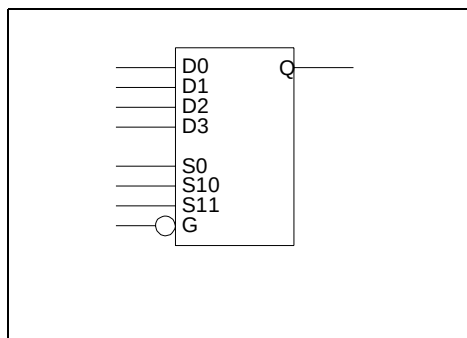
Truth Table

S1 0	S1 1	S0	G	Q _{n+1}
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All	1	

DLM4A

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Input
D0, D1, D2, D3, S0, S10,
S11, G

Output
Q

Function

Data Latch with 4-input Multiplexed Data

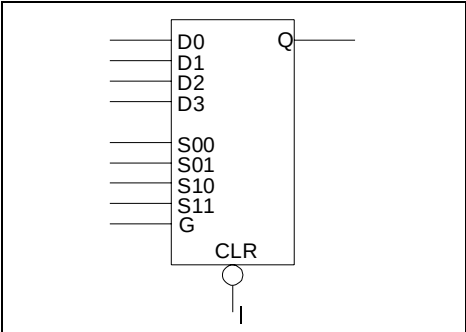
Truth Table

S10	S11	S0	G	Q _{n+1}
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

Family	Modules	
	Seq	Comb
All	1	

DLM8A

ACT 3



Input	Output
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR	Q

Function
D-Type Latch with 4-input Multiplexed Data and active low Clear

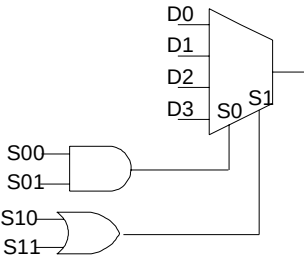
Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3

Family	Modules	
	Seq	Comb
ACT 3	1	

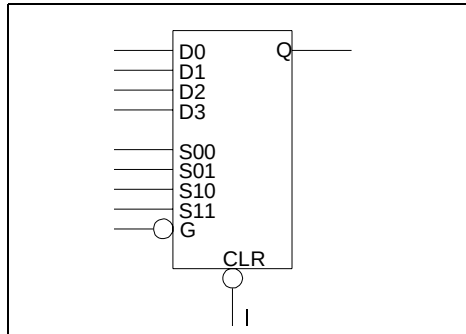
NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DLM8B

ACT 3



Input
D0, D1, D2, D3, S00,
S01, S10, S11, CLK, CLR

Output
Q

Function

D-Type Latch with 4-input Multiplexed Data and active low Clear

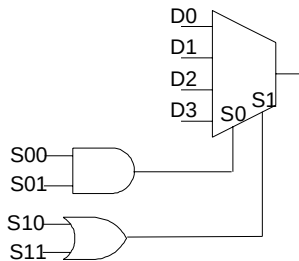
Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	1	Q
1	0	0	0	X	0	D0
1	0	0	X	0	0	D0
1	0	0	1	1	0	D1
1	1	X	0	X	0	D2
1	X	1	0	X	0	D2
1	1	X	X	0	0	D2

Family	Modules	
	Seq	Comb
ACT 3	1	

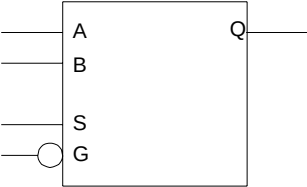
NOTE 1: The DLM8B macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DLMA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

Data Latch with 2-input Multiplexed Data, and active low Clock

Truth Table

S	G	Q _{n+1}
X	1	Q
0	0	A
1	0	B

Input

A, B, G, S

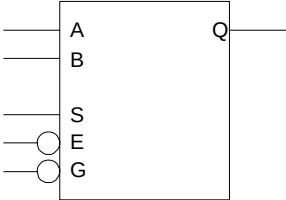
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLME1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function

2-bit Data Latch with Multiplexed Data and Enable, and active low Clock

Truth Table

E	S	G	Q _{n+1}
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

Input

A, B, E, G, S

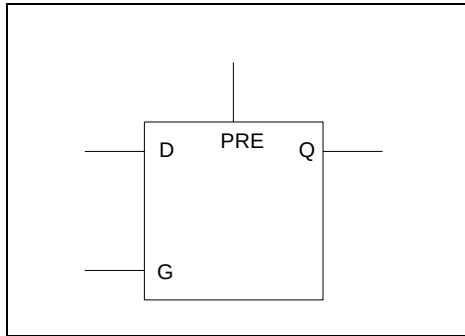
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLP1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

Data Latch with active high Preset, and Clock

Truth Table

PRE	G	Q_{n+1}
1	X	1
0	0	Q
0	1	D

Input

D, G, PRE

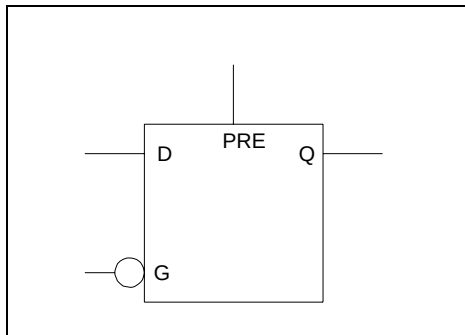
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

Data Latch with active high Preset, and active low Clock

Truth Table

PRE	G	Q_{n+1}
1	X	1
0	1	Q
0	0	D

Input

D, G, PRE

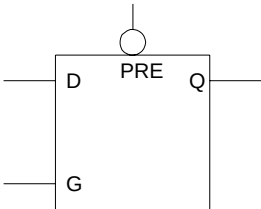
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch with active low Preset, and active high Clock

Truth Table

PRE	G	Q _{n+1}
0	X	1
1	0	Q
1	1	D

Input

D, G, PRE

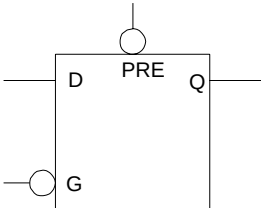
Output

Q

Family	Modules	
	Seq	Comb
All		1

DLP1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

Data Latch with active low Preset and Clock

Truth Table

PRE	G	Q _{n+1}
0	X	1
1	1	Q
1	0	D

Input

D, G, PRE

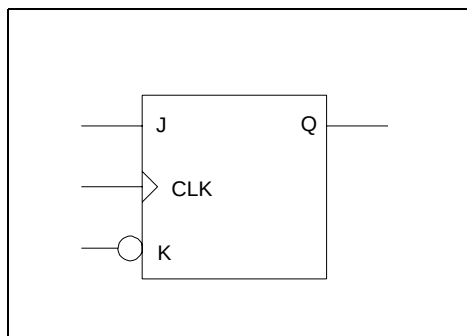
Output

Q

Family	Modules	
	Seq	Comb
All		1

JKF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

JK Flip-Flop with active low K-Input

Truth Table

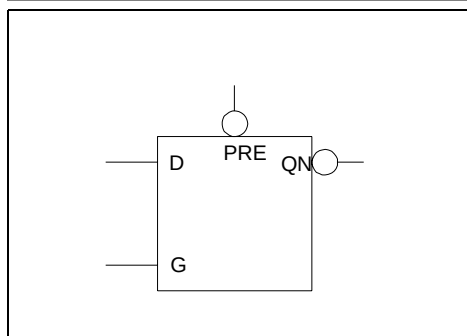
J	K	CLK	Q_{n+1}
0	0	$\uparrow$	0
0	1	$\uparrow$	Q
1	0	$\uparrow$	$\bar{Q}$
1	1	$\uparrow$	1

Input
J, K, CLK**Output**
Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1
Others	1	

DLP1D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX

**Function**

Data Latch with active low Preset and Output, and active high Clock

Truth Table

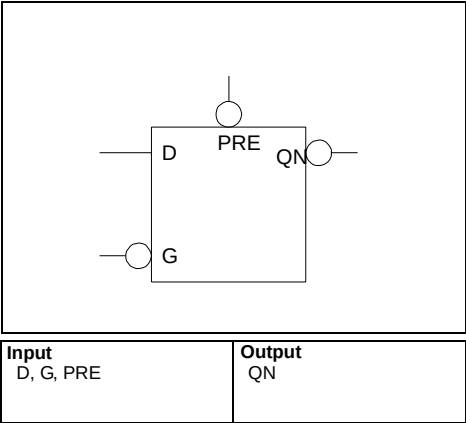
PRE	G	QN_{n+1}
0	X	0
1	0	QN
1	1	$\bar{D}$

Input
D, G, PRE**Output**
QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DLP1E

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
Data Latch with active low Preset, Clock and Output

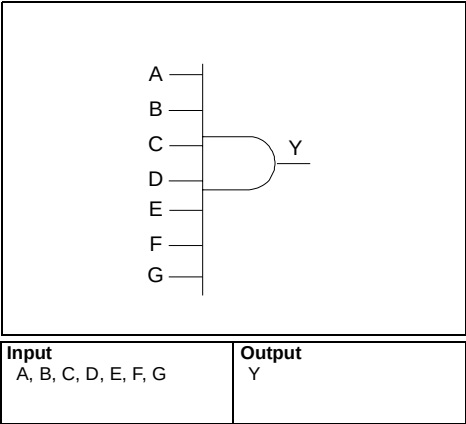
Truth Table

PRE	G	Q _{n+1}
0	X	0
1	0	!D
1	1	QN

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others	1	

DXAND7

3200DX, 42MX



Function
Seven-input AND Gate

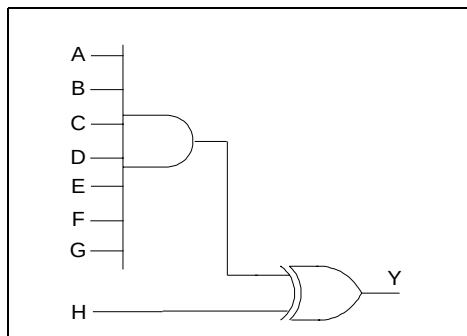
Truth Table

A through G	Y
All inputs = 1	1
Any input = 0	0

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXAX7

3200DX, 42MX

**Function**

Eight-input AND/Exclusive-OR Gate

Truth Table

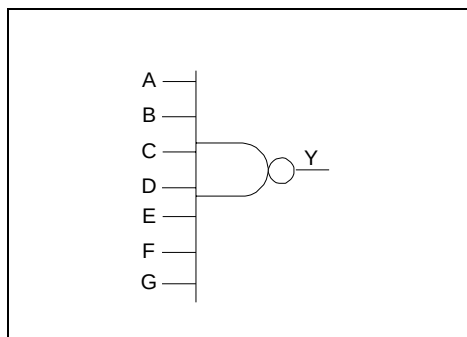
A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

Input A, B, C, D, E, F, G, H	Output Y
--	--------------------

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXNAND7

3200DX, 42MX

**Function**

Seven-input NAND Gate

Truth Table

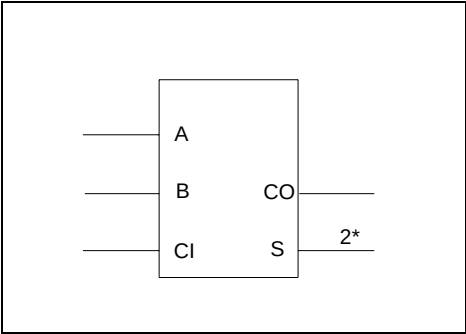
A through G	Y
All inputs = 1	0
Any input = 0	1

Input A, B, C, D, E, F, G	Output Y
-------------------------------------	--------------------

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

FA1

ACT 1, 40MX, 54SX



Input
A, B, CI

Output
CO, S

Function

1 bit adder with active high I/Os

Truth Table

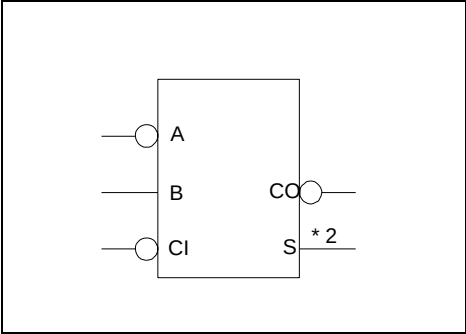
A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		3
54SX		2

* A 2 on the symbol implies 2 logic module delays only in ACT 1 and 40MX.

FA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input
A, B, CI

Output
CO, S

Function

1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

Truth Table

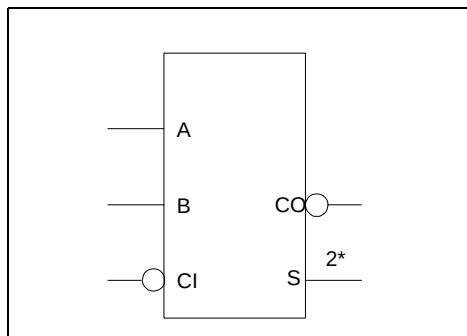
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

FA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input
A, B, CI

Output
CO, S

Function

1-bit Adder, with active low Carry In and Carry Out

Truth Table

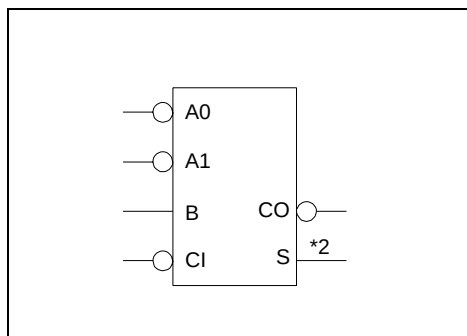
A	B	CI	CO	S
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

FA2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input
A0, A1, B, CI

Output
CO, S

Function

1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

Truth Table ¹

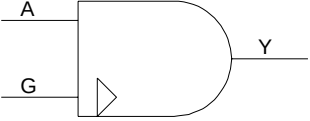
A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families.

GAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input AND Clock Net

Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

Input
A, G

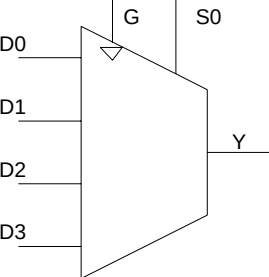
Output
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GMX4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-to-1 Mux Clock Net

Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

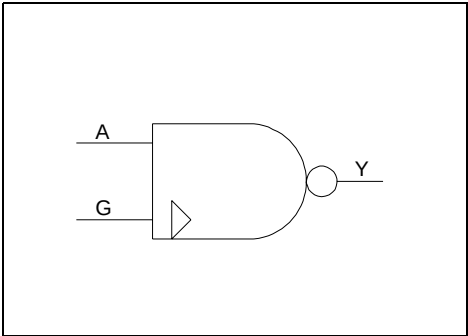
Input
D0, D1, D2, D3, S0, G

Output
Y

Family	Modules	
	Seq	Comb
All		1

GNAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input NAND Clock Net

Truth Table

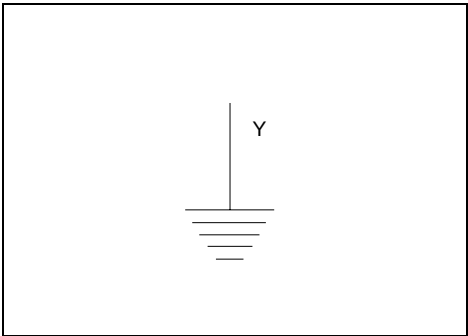
A	G	Y
X	0	1
0	X	1
1	1	0

Input A, G	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

GND

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



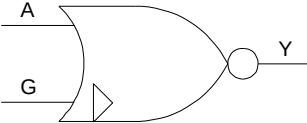
Function
Ground

Input	Output Y
--------------	--------------------

NOTE: Ground does not use any modules.

GNOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2-Input NOR Clock Net

Truth Table

A	G	Y
0	0	1
X	1	0
1	X	0

Input

A, G

Output

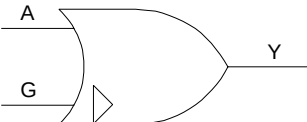
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2-Input OR Clock Net

Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

Input

A, G

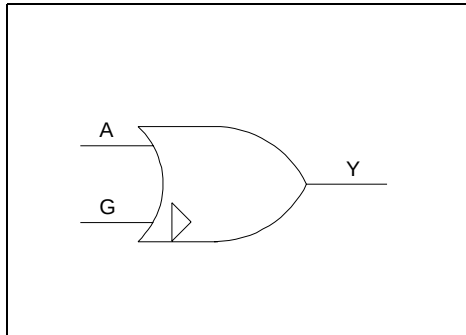
Output

Y

Family	Modules	
	Seq	Comb
All		1

GXOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input XOR Clock Net

Truth Table

A	G	Y
0	0	0
0	1	1
1	0	1
1	1	0

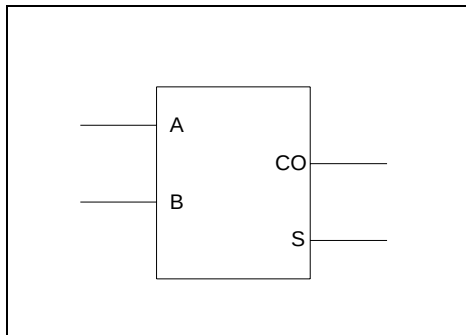
Input A, G	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

HA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

Half Adder

Truth Table

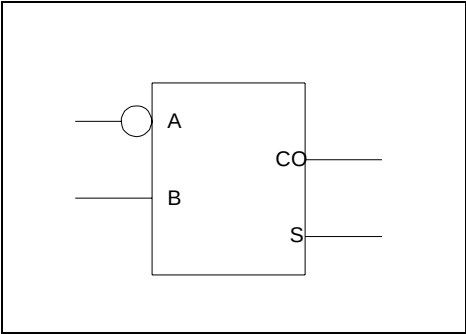
A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Input A, B	Output CO, S
----------------------	------------------------

Family	Modules	
	Seq	Comb
All		2

HA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Half-Adder with active low A-Input

Truth Table

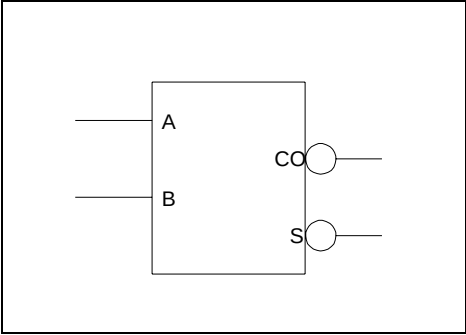
A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

Input A, B	Output CO, S
----------------------	------------------------

Family	Modules	
	Seq	Comb
All		2

HA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Half-Adder with active low Carry Out and Sum

Truth Table

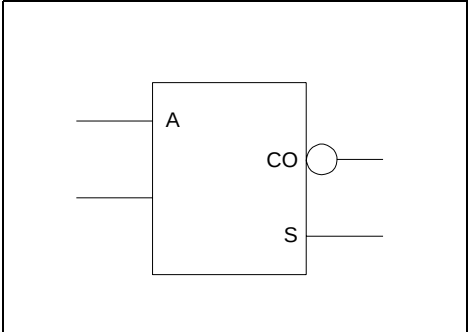
A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

Input A, B	Output CO, S
----------------------	------------------------

Family	Modules	
	Seq	Comb
All		2

HA1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Half-Adder with active low Carry Out

Truth Table

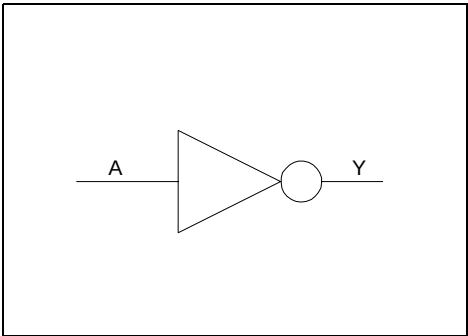
A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

Input A, B	Output CO, S
----------------------	------------------------

Family	Modules	
	Seq	Comb
All		2

INV

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Inverter with active low Output

Truth Table

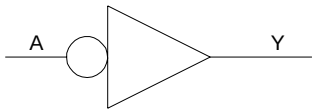
A	Y
0	1
1	0

Input A	Output Y
-------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

INVA

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

Inverter with active low Input

Truth Table

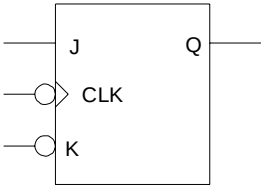
A	Y
0	1
1	0

Input A	Output Y
-------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

JKF1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

JK Flip-Flop with active low Clock and K-Input

Truth Table

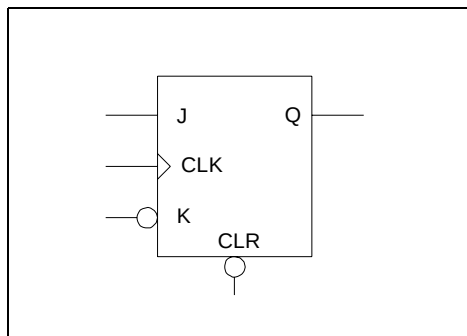
J	K	CLK	Q_{n+1}
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

Input J, K, CLK	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1
Others	1	

JKF2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

JK Flip-Flop with active low Clear and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	$\uparrow$	0
1	0	1	$\uparrow$	Q
1	1	0	$\uparrow$	$!Q$
1	1	1	$\uparrow$	1

Input

CLR, J, K, CLK

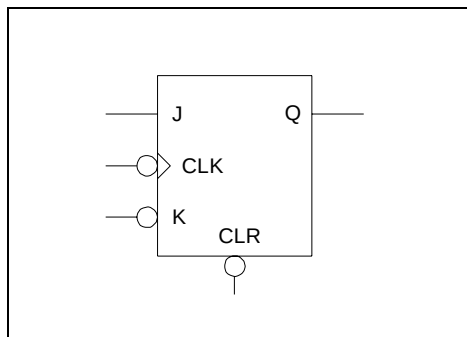
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1
Others	1	

JKF2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

JK Flip-Flop with active low Clear, Clock and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	$\downarrow$	0
1	0	1	$\downarrow$	Q
1	1	0	$\downarrow$	$!Q$
1	1	1	$\downarrow$	1

Input

CLR, J, K, CLK

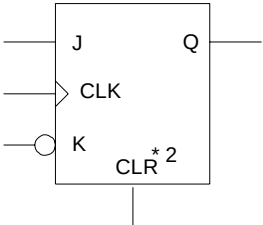
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1
Others	1	

JKF2C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Input
CLR, J, K, CLK

Output
Q

Function

JK Flip-Flop with active high Clear, and active low K-Input

Truth Table

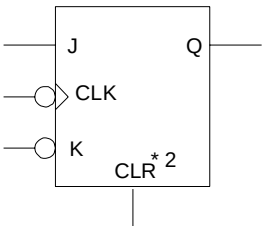
CLR	J	K	CLK	Q _{n+1}
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

JKF2D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Input
CLR, J, K, CLK

Output
Q

Function

JK Flip-Flop with active high Clear, and active low Clock and K-Input

Truth Table

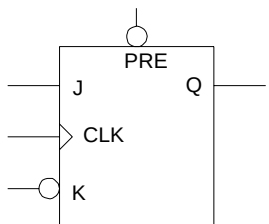
CLR	J	K	CLK	Q _{n+1}
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

JKF3A

ACT 1, 40MX, 54SX

**Function**

JK Flip-Flop with active low Preset and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	$\uparrow$	0
1	0	1	$\uparrow$	Q
1	1	0	$\uparrow$	!Q
1	1	1	$\uparrow$	1

Input

J, K, PRE, CLK

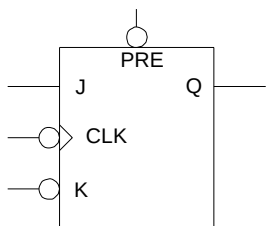
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1

JKF3B

ACT 1, 40MX, 54SX

**Function**

JK Flip-Flop with active low Preset, Clock and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	$\downarrow$	0
1	0	1	$\downarrow$	Q
1	1	0	$\downarrow$	!Q
1	1	1	$\downarrow$	1

Input

J, K, PRE, CLK

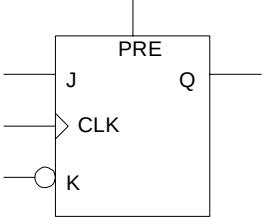
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
54SX	1	1

JKF3C

ACT 1, 40MX



Function

JK Flip-Flop with active high Preset, and active low K-Input

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Input

J, K, PRE, CLK

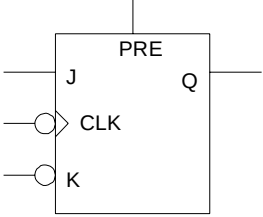
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

JKF3D

ACT 1, 40MX



Function

JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Input

J, K, PRE, CLK

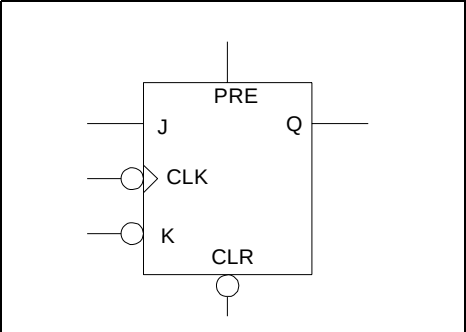
Output

Q

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

JKF4B

ACT 1, 40MX



Input
CLR, J, K, PRE, CLK

Output
Q

Function

JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

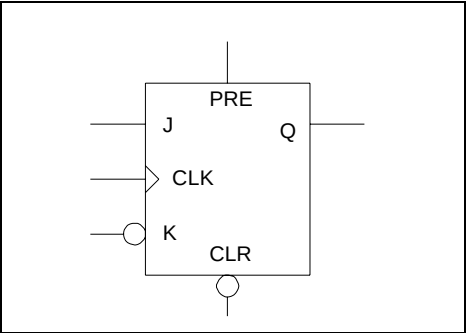
Truth Table

CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

JKFPC

ACT 1, 40MX



Input
CLR, J, K, PRE, CLK

Output
Q

Function

JK Flip-Flop with active high Preset, and active low Clear and K- Input

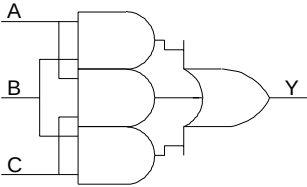
Truth Table

CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2

MAJ3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
3-Input majority function

Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

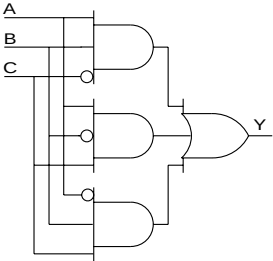
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

MAJ3X

54SX



Function
2 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

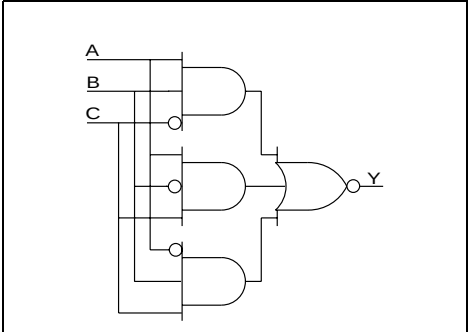
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

MAJ3XI

54SX



Input A, B, C	Output Y
-------------------------	--------------------

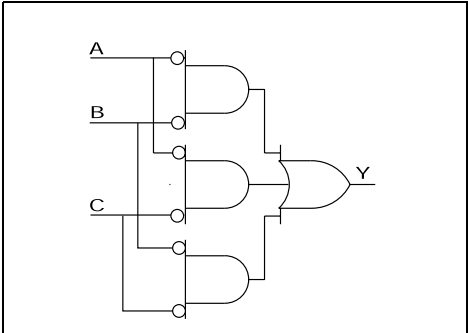
Function
2 of 3 function with active low output

Truth Table			
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

MIN3

54SX



Input A, B, C	Output Y
-------------------------	--------------------

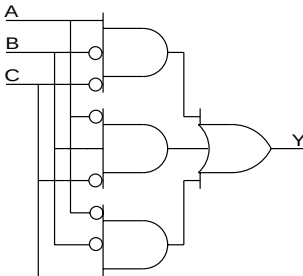
Function
3-Input minority function

Truth Table			
A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Family	Modules	
	Seq	Comb
54SX		1

MIN3X

54SX



Function

1 of 3 function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Input

A, B, C

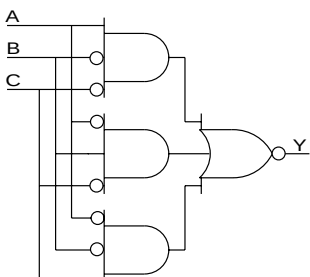
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

MIN3XI

54SX



Function

1 of 3 function with active low output

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Input

A, B, C

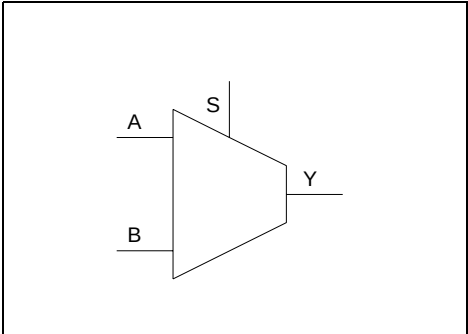
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

MX2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2 to 1 Multiplexer

Truth Table

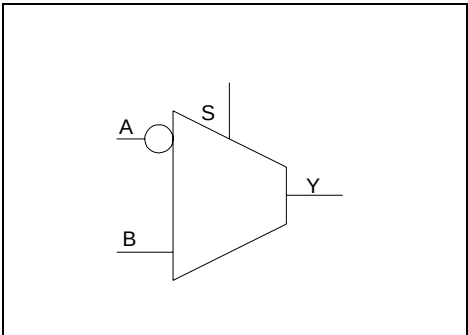
S	Y
0	A
1	B

Input A, B, S	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

MX2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2 to 1 Multiplexer with active low A-Input

Truth Table

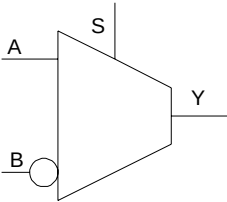
S	Y
0	!A
1	B

Input A, B, S	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

MX2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2 to 1 Multiplexer with active low B-Input

Truth Table

S	Y
0	A
1	!B

Input

A, B, S

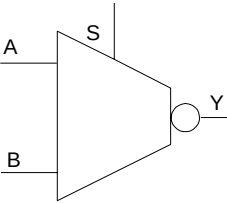
Output

Y

Family	Modules	
	Seq	Comb
All		1

MX2C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2 to 1 Multiplexer with active low Output

Truth Table

S	Y
0	!A
1	!B

Input

A, B, S

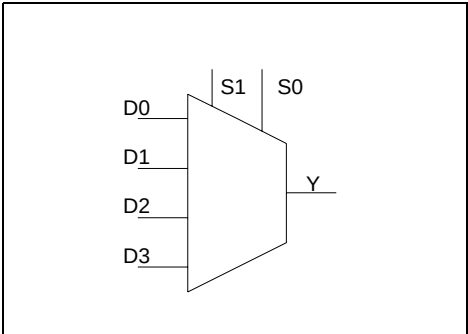
Output

Y

Family	Modules	
	Seq	Comb
All		1

MX4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4 to 1 Multiplexer

Truth Table

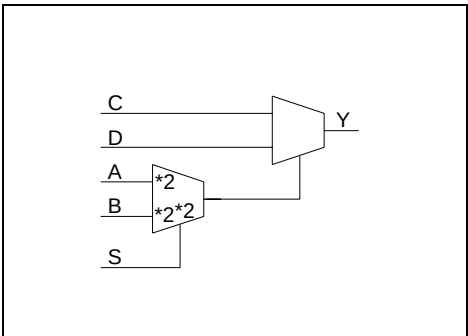
S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Input D0, S0, S1, D1, D2, D3	Output Y
--	--------------------

Family	Modules	
	Seq	Comb
All		1

MXC1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
Carry select multiplexer, used in adders

Truth Table

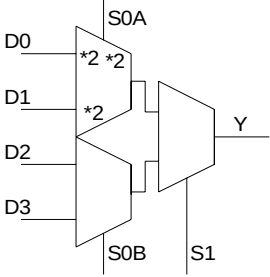
A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

Input S, A, B, C, D	Output Y
-------------------------------	--------------------

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

MXT

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
Multiplexer with separate select lines

Truth Table

SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

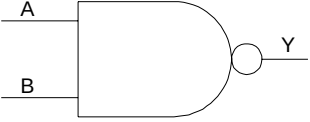
Input
D0 , D1, D2, D3, S0A,
S0B, S1

Output
Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		1
Others		2

NAND2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input NAND

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

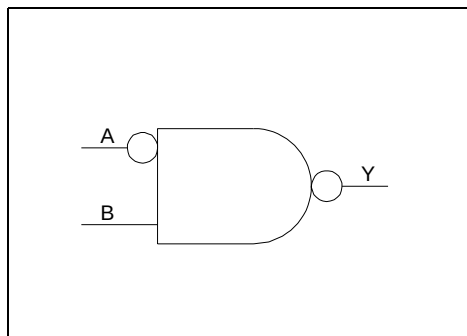
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

NAND2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input NAND with active low A-Input

Truth Table

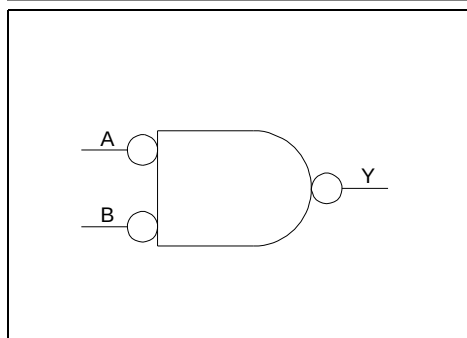
A	B	Y
X	0	1
0	1	0
1	X	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NAND2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input NAND with active low Inputs

Truth Table

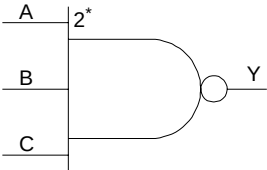
A	B	Y
0	0	0
X	1	1
1	X	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NAND3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input NAND

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input

A, B, C

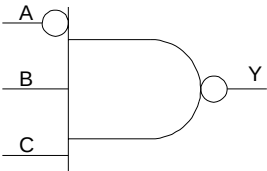
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NAND3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input NAND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

Input

A, B, C

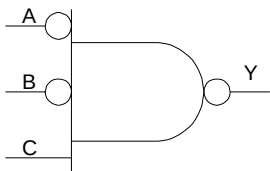
Output

Y

Family	Modules	
	Seq	Comb
All		1

NAND3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input NAND with active low A- and B-Inputs

Truth Table

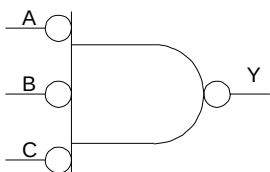
A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NAND3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input NAND with active low Inputs

Truth Table

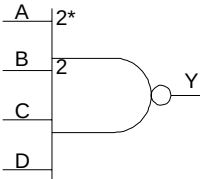
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

NAND4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input NAND

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Input

A, B, C, D

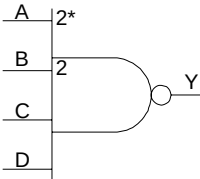
Output

Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

NAND4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input NAND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	1	1	1	0
1	X	X	X	1

Input

A, B, C, D

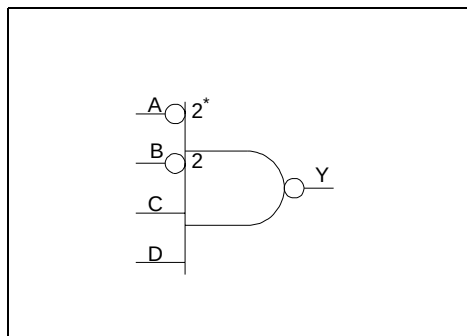
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NAND4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input NAND with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

Input

A, B, C, D

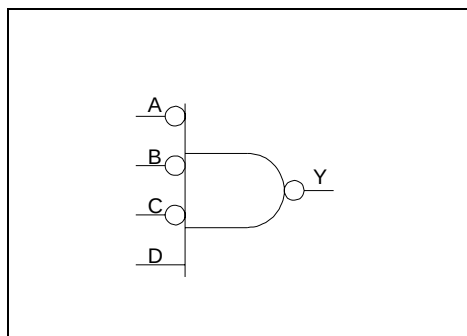
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NAND4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input NAND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Input

A, B, C, D

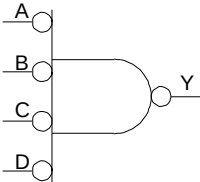
Output

Y

Family	Modules	
	Seq	Comb
All		1

NAND4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input NAND with active low Inputs

Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

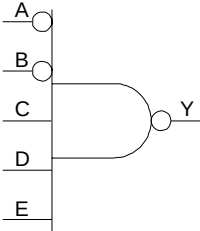
Input
A, B, C, D

Output
Y

Family	Modules	
	Seq	Comb
All		1

NAND5B

54SX



Function
5-input NAND with active low A- and B-inputs

Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

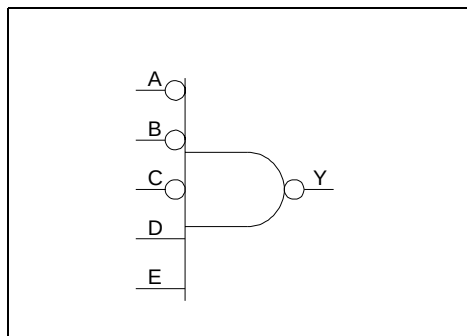
Input
A, B, C, D, E

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

NAND5C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX

**Function**

5-Input NAND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Input

A, B, C, D, E

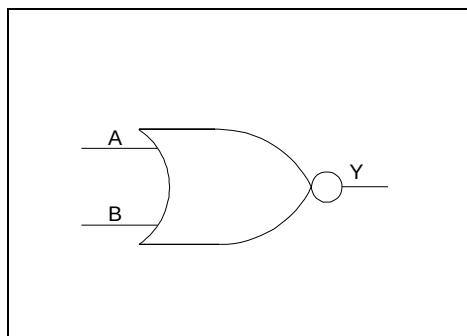
Output

Y

Family	Modules	
	Seq	Comb
All		1

NOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input NOR

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

Input

A, B

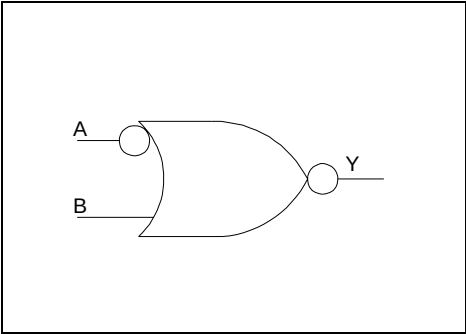
Output

Y

Family	Modules	
	Seq	Comb
All		1

NOR2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input NOR with active low A-Input

Truth Table

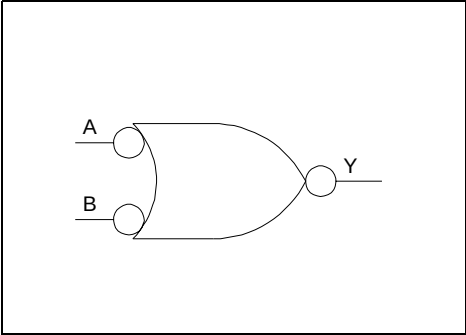
A	B	Y
0	X	0
1	0	1
X	1	0

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2-Input NOR with active low Inputs

Truth Table

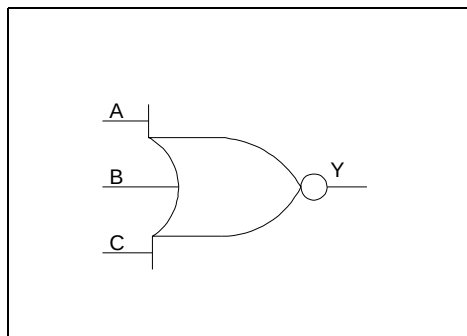
A	B	Y
X	0	0
0	X	0
1	1	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input NOR

Truth Table

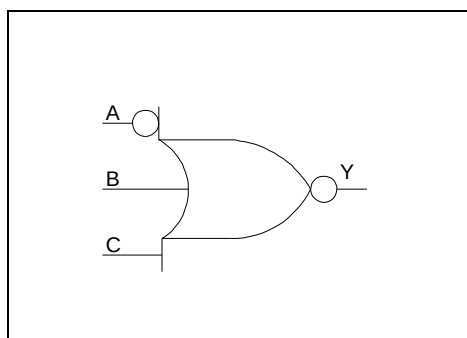
A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input NOR with active low A-Input

Truth Table

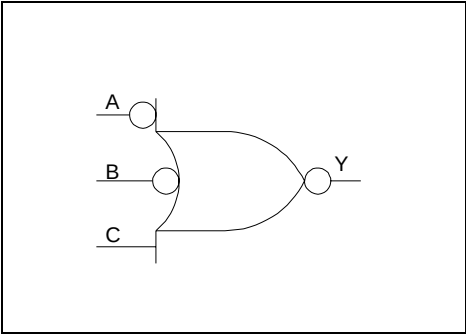
A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
3-Input NOR with active low A- and B-Inputs

Truth Table

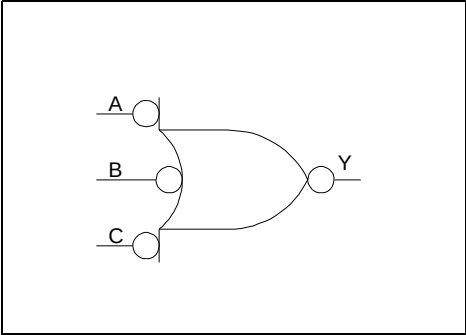
A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
3-Input NOR with active low Inputs

Truth Table

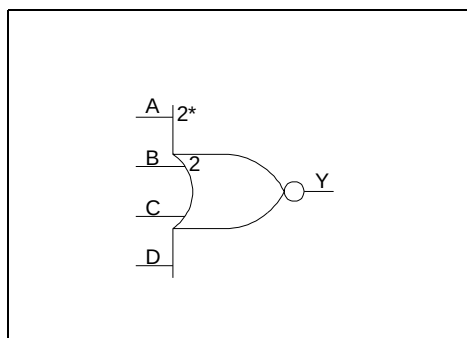
A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

NOR4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input NOR

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Input

A, B, C, D

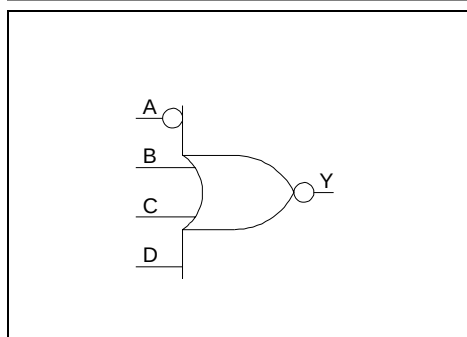
Output

Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

NOR4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input NOR with active low A-Input

Truth Table

A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

Input

A, B, C, D

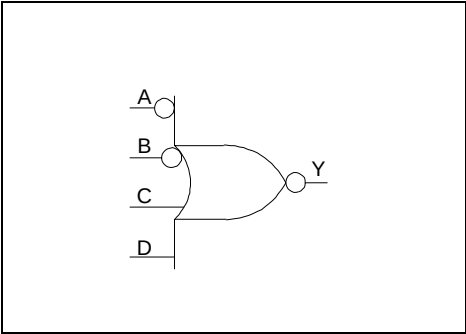
Output

Y

Family	Modules	
	Seq	Comb
All		1

NOR4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input NOR with active low A- and B-Inputs

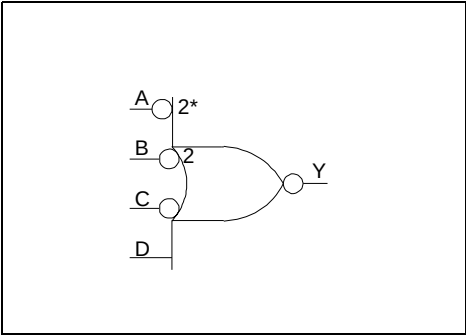
Truth Table				
A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
All		1

NOR4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
4-Input NOR with active low A-, B- and C-Inputs

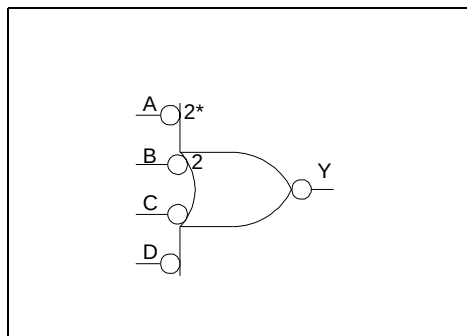
Truth Table				
A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

Input	Output
A, B, C, D	Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NOR4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input NOR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Input

A, B, C, D

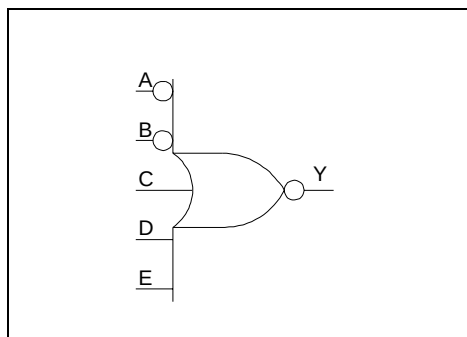
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

NOR5B

54SX

**Function**

5-Input NOR with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Input

A, B, C, D, E

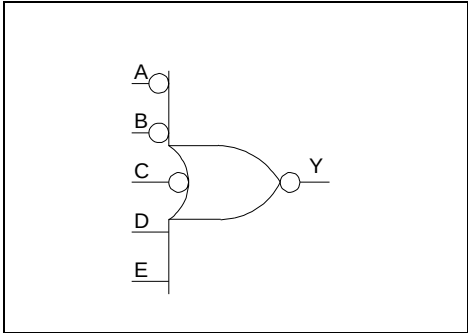
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

NOR5C

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Input A, B, C, D, E	Output Y
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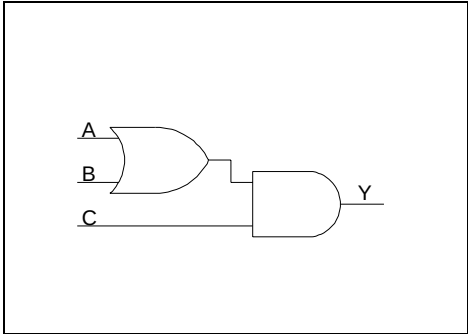
Function
5-Input NOR with active low A-, B- and C-Inputs

Truth Table					
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Family	Modules	
	Seq	Comb
All		1

OA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Input A, B, C	Output Y
-------------------------	--------------------

Function
3 Input OR-AND

Truth Table			
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Family	Modules	
	Seq	Comb
All		1

OA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

```
graph LR; A((A)) --- OR1[OR]; B((B)) --- OR1; C((C)) --- OR1; OR1 --- AND1[AND]; C --- AND1; AND1 --- Y((Y))
```

Function
3 Input OR-AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
54SX		1

OA1B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

```
graph LR; A((A)) --- OR1[OR]; B((B)) --- OR1; C((C)) --- OR1; OR1 --- AND1[AND]; C --- AND1; AND1 --- Y((Y))
```

Function
3 Input OR-AND with active low C-Input

Truth Table

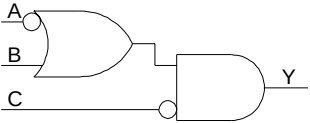
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Input A, B, C	Output Y
-------------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

OA1C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3 Input OR-AND with active low A- and C-Inputs

Truth Table

A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

Input

A, B, C

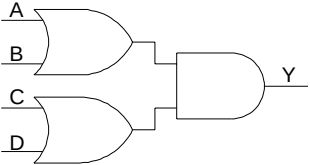
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2-wide 4-Input OR-AND

Truth Table

A	B	C	D	Y
X	X	0	0	0
0	0	X	X	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1

Input

A, B, C, D

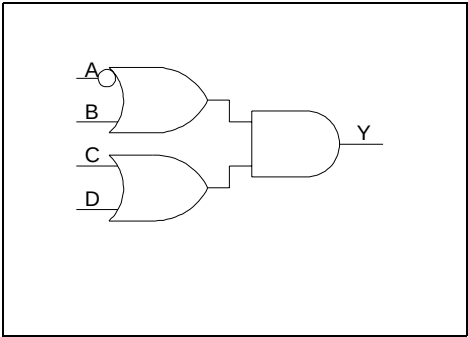
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2 wide 4-Input OR-AND with active low A-Input

Truth Table

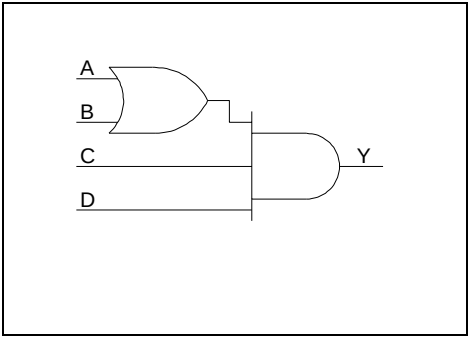
A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

Input A, B, C, D	Output Y
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Family	Modules	
	Seq	Comb
All		1

OA3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4- Input OR-AND

Truth Table

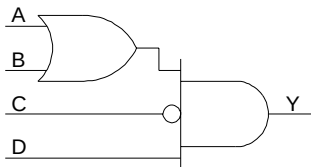
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

Input A, B, C, D	Output Y
---------------------	-------------

Family	Modules	
	Seq	Comb
All		1

OA3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input OR-AND with active low C-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

Input

A, B, C, D

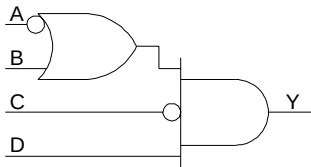
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input OR-AND with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

Input

A, B, C, D

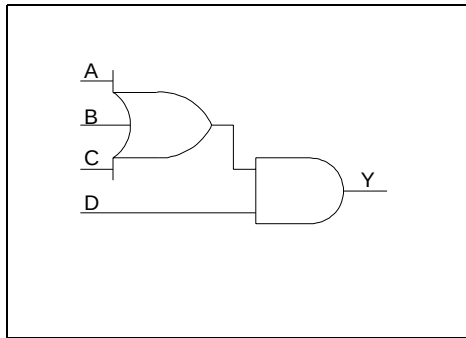
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA4

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX

**Function**

4-Input OR-AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

Input

A, B, C, D

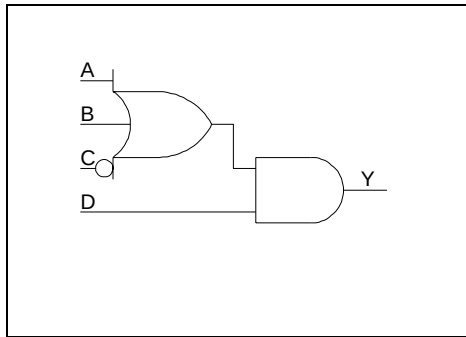
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input OR-AND with active low C-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Input

A, B, C, D

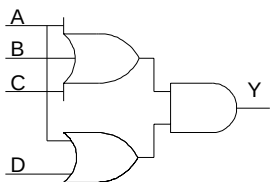
Output

Y

Family	Modules	
	Seq	Comb
All		1

OA5

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input complex OR-AND

Truth Table

A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Input

A, B, C, D

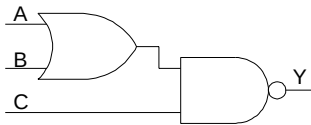
Output

Y

Family	Modules	
	Seq	Comb
All		1

OAI1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input OR-AND-INVERT

Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Input

A, B, C

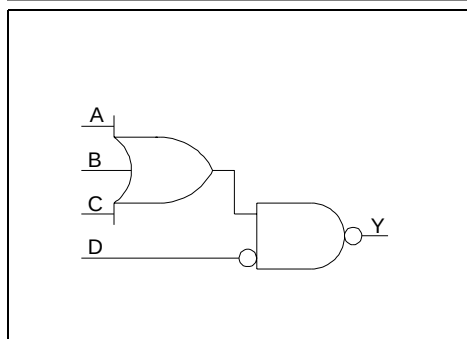
Output

Y

Family	Modules	
	Seq	Comb
All		1

OAI2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input OR-AND-INVERT with active low D-Input

Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Input

A, B, C, D

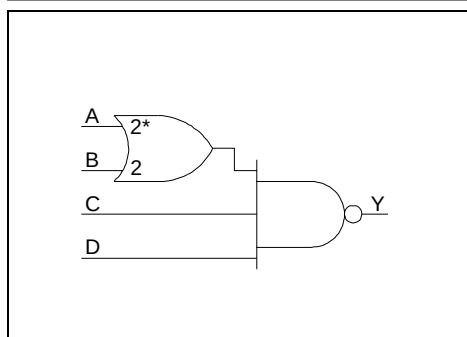
Output

Y

Family	Modules	
	Seq	Comb
All		1

OAI3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4 Input OR-AND-INVERT

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Input

A, B, C, D

Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

OAI3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

```
graph LR; A --- OR1(( )); B --- OR1; OR1 --- AND1(( )); C --- AND1; D --- AND1; AND1 --- NOT1[ ]; NOT1 --- Y
```

Function

4 Input OR-AND-INVERT with active low C- and D-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Input

A, B, C, D

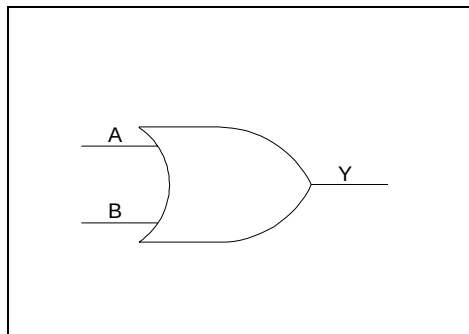
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input OR

Truth Table

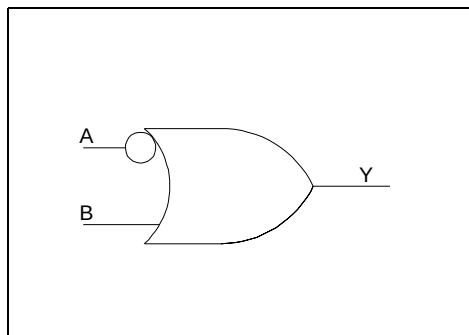
A	B	Y
0	0	0
X	1	1
1	X	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

OR2A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input OR with active low A-Input

Truth Table

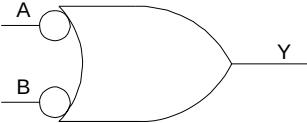
A	B	Y
0	X	1
1	0	0
X	1	1

Input A, B	Output Y
----------------------	--------------------

Family	Modules	
	Seq	Comb
All		1

OR2B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

2-Input OR with active low Inputs

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

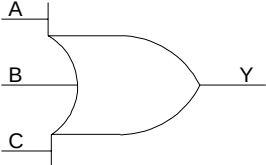
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

OR3

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input OR

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

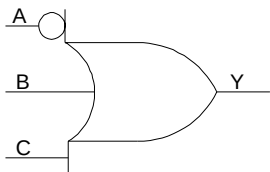
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
All		1

OR3A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input OR with active low A-Input

Truth Table

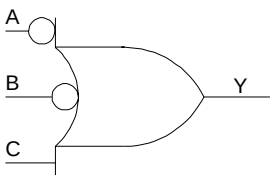
A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR3B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input OR with active low A- and B-Inputs

Truth Table

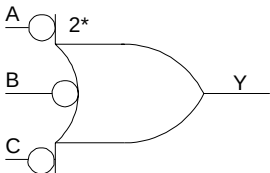
A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

OR3C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Input

A, B, C

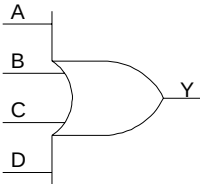
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

OR4

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input OR

Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Input

A, B, C, D

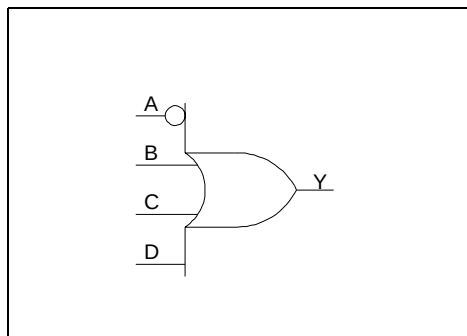
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR4A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input OR with active low A-Input

Truth Table

A	B	C	D	Y
0	X	X	X	1
1	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1

Input

A, B, C, D

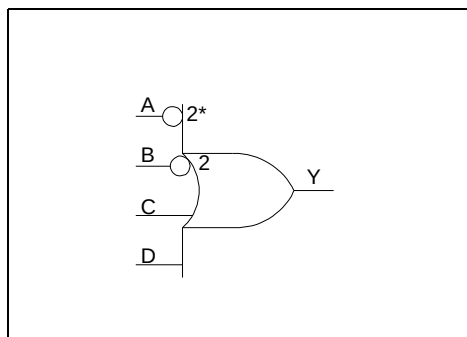
Output

Y

Family	Modules	
	Seq	Comb
All		1

OR4B

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

4-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

Input

A, B, C, D

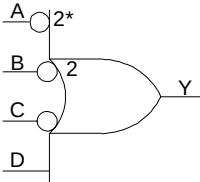
Output

Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

OR4C

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

Input

A, B, C, D

Output

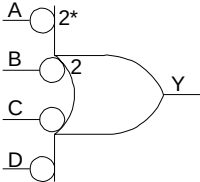
Y

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		2
Others		1

*A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4D

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

4-Input OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Input

A, B, C, D

Output

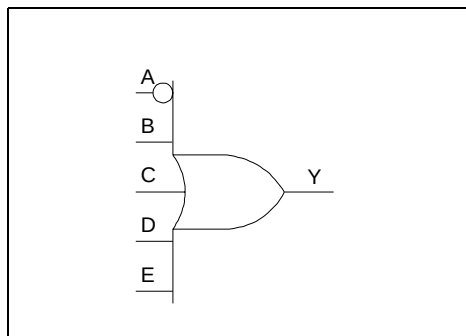
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except for 54SX.

OR5A

54SX



Function

5-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Input

A, B, C, D, E

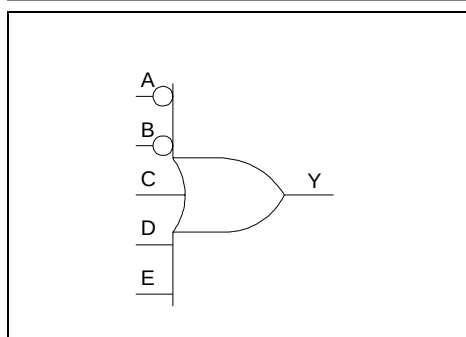
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

OR5B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function

5-Input OR with active low A-Input

Truth Table

A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

Input

A, B, C, D, E

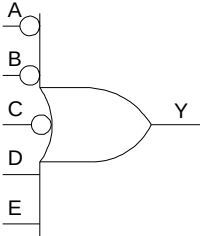
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

OR5C

54SX



Function

5-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

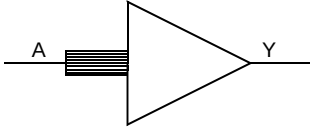
Input
A, B, C, D, E

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

QCLKINT

3200DX, 42MX



Function

Internal Clock Interface

Truth Table

A	Y
0	0
1	1

Input
A

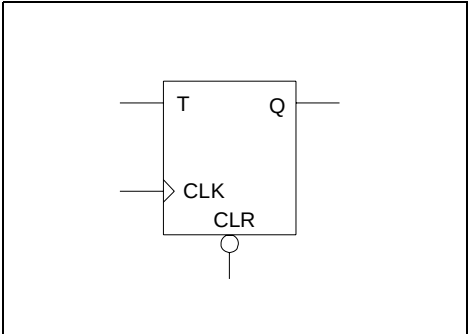
Output
Y

NOTE: QCLKIN does not use any modules

For more information on the Global Clock Network, refer to Actel's Data Book.

TF1A

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
T-Type Flip-Flop with active low Clear

Truth Table

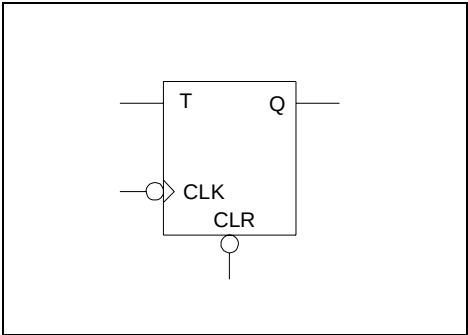
CLR	T	CLK	Q _{n+1}
0	X	X	0
1	1	↑	!Q
1	0	↑	Q

Input CLR, T, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All	1	

TF1B

ACT 2/1200XL, ACT 3, 3200DX, 42MX, 54SX



Function
T-Type Flip-Flop with active low Clear and Clock

Truth Table

CLR	T	CLK	Q _{n+1}
0	X	X	0
1	1	↓	!Q
1	0	↓	Q

Input CLR, T, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All	1	

VCC

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

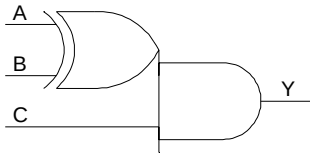


Function
Power

Input	Output Y
-------	-------------

XA1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
3-Input XOR-AND

Truth Table

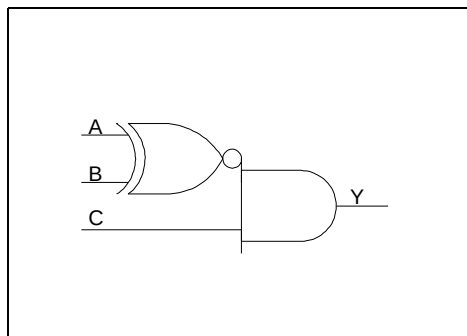
A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

Input A, B, C	Output Y
------------------	-------------

Family	Modules	
	Seq	Comb
All		1

XA1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input XNOR-AND

Truth Table

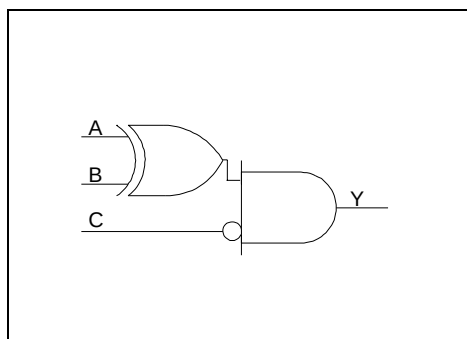
A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

XA1B

54SX

**Function**

3-Input XNOR-AND with active low C-input

Truth Table

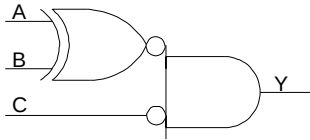
A	B	C	Y
X	X	1	0
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
54SX		1

XA1C

54SX



Function

3-Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1

Input

A, B, C

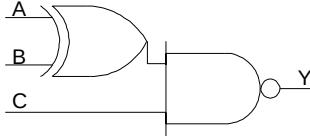
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

XA11

54SX



Function

3-Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Input

A, B, C

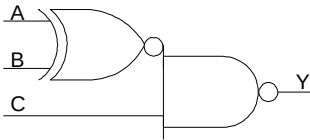
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

XA11A

54SX



Function
3-Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

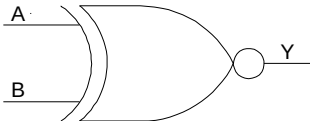
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

XNOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
2- Input XNOR

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

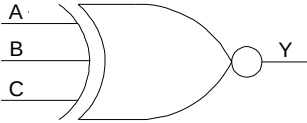
Input
A, B

Output
Y

Family	Modules	
	Seq	Comb
All		1

XNOR3

54SX



Function

3-Input XNOR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Input

A, B, C

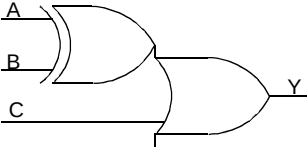
Output

Y

Family	Modules	
	Seq	Comb
54SX		1

XO1

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

3-Input XOR-OR

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

Input

A, B, C

Output

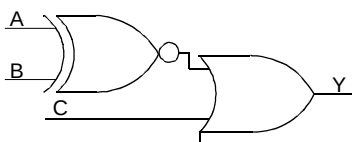
Y

Family	Modules	
	Seq	Comb
All		1

180

XO1A

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

3-Input XOR-OR

Truth Table

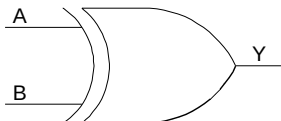
A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

Input
A, B, C**Output**
Y

Family	Modules	
	Seq	Comb
All		1

XOR2

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

2-Input XOR

Truth Table

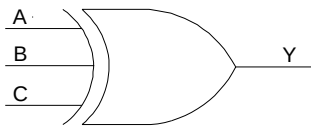
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Input
A, B**Output**
Y

Family	Modules	
	Seq	Comb
All		1

XOR3

54SX



Function
3-Input XOR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

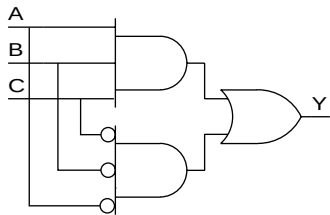
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

ZOR3

54SX



Function
3-Input function

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

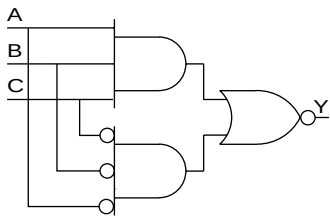
Input
A, B, C

Output
Y

Family	Modules	
	Seq	Comb
54SX		1

ZOR3I

54SX



Function
3-Input function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Input
A, B, C

Output
Y

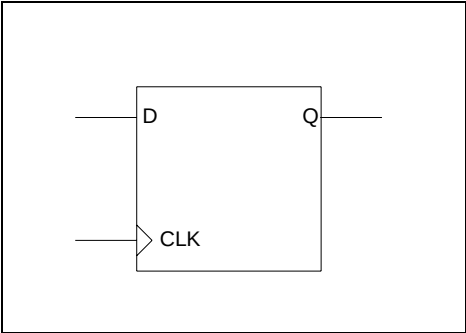
Family	Modules	
	Seq	Comb
54SX		1

CC-Module Flip Flops

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays*.)

DF1_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop

Truth Table

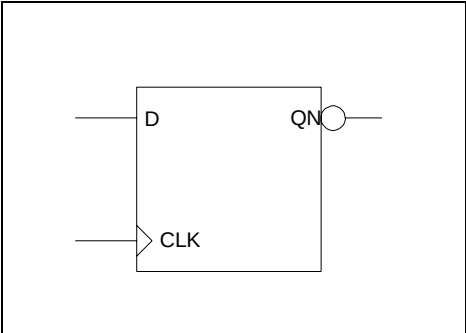
CLK	Q _{n+1}
↑	D

Input D, CLK	Output Q
------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DF1A_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with active low Output

Truth Table

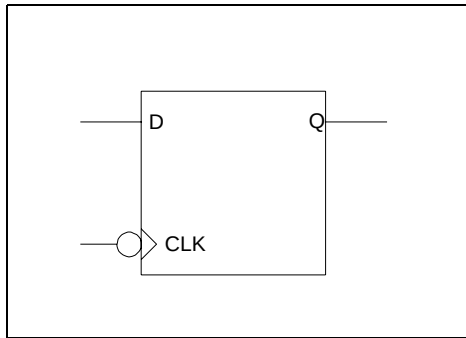
CLK	QN _{n+1}
↑	!D

Input D, CLK	Output QN
------------------------	---------------------

Family	Modules	
	Seq	Comb
All		2

DF1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Clock

Truth Table

CLK	Q_{n+1}
↓	D

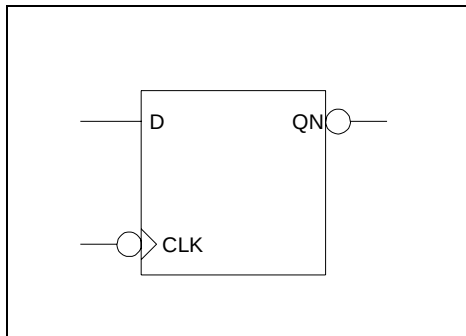
Input
D, CLK

Output
Q

Family	Modules	
	Seq	Comb
All		2

DF1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Clock and Output

Truth Table

CLK	QN_{n+1}
↓	!D

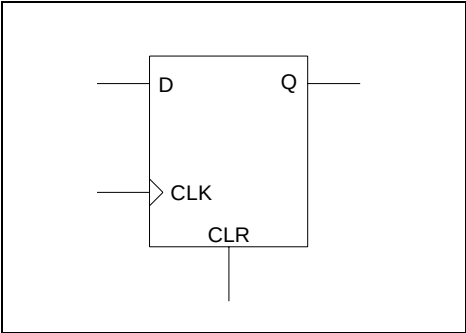
Input
D, CLK

Output
QN

Family	Modules	
	Seq	Comb
All		2

DFC1_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active high Clear

Truth Table

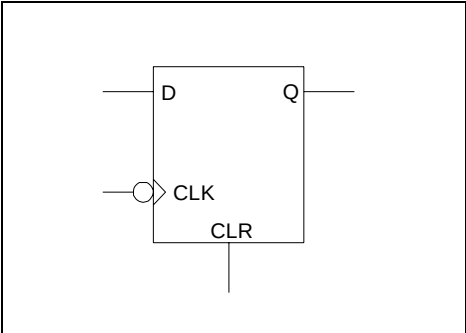
CLR	CLK	Q _{n+1}
1	X	0
0	↑	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFC1A_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

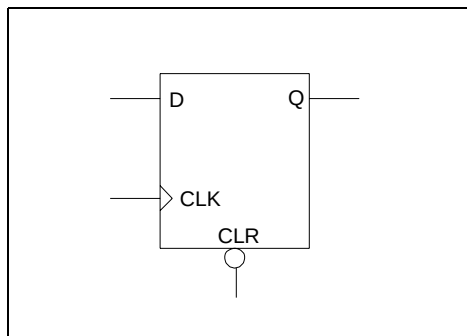
CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFC1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop, with active low Clear

Truth Table

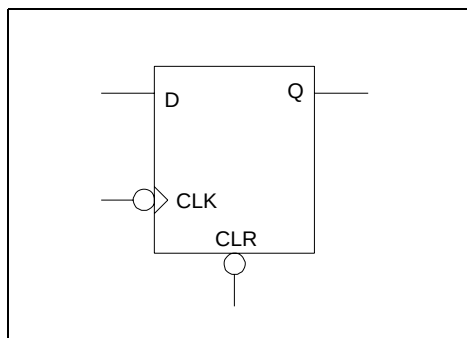
CLR	CLK	Q_{n+1}
0	X	0
1	$\uparrow$	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFC1D_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop, with active low Clear and Clock

Truth Table

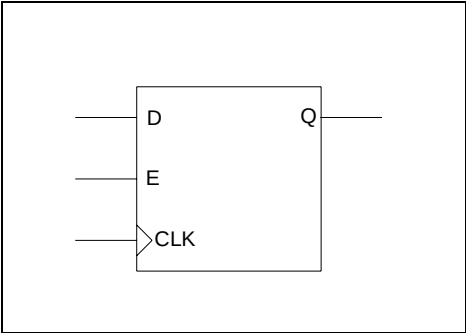
CLR	CLK	Q_{n+1}
0	X	0
1	$\downarrow$	D

Input D, CLK, CLR	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFE_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active high Enable

Truth Table

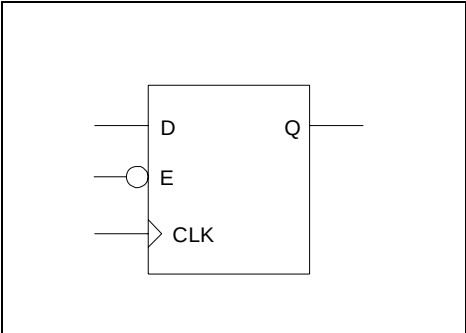
E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Input D, E, CLK	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFE1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop, with active low Enable

Truth Table

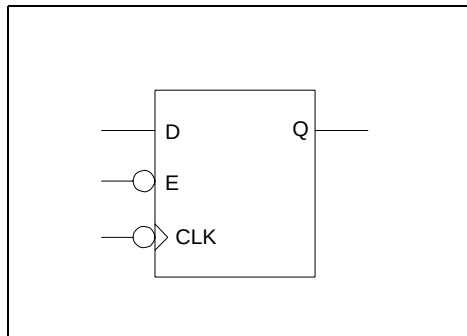
E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Input D, E, CLK	Output Q
---------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFE1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Input

D, E, CLK

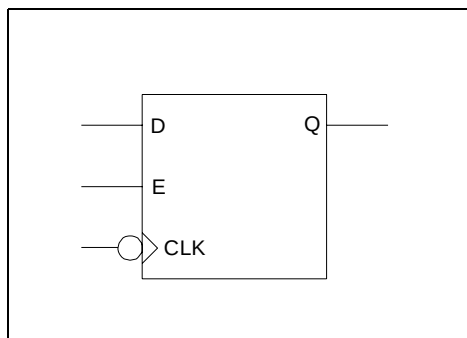
Output

Q

Family	Modules	
	Seq	Comb
All		2

DFEA_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Input

D, E, CLK

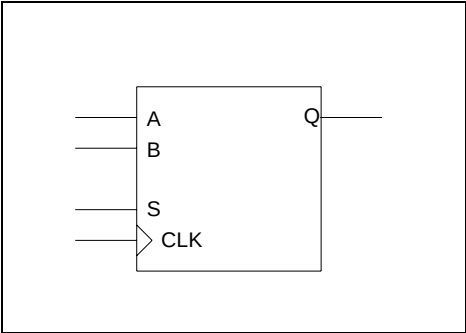
Output

Q

Family	Modules	
	Seq	Comb
All		2

DFM_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

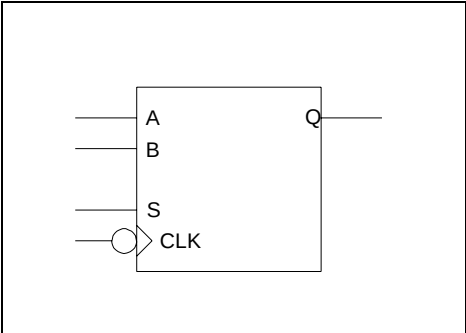
S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Input A, B, S, CLK	Output Q
------------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFMA_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

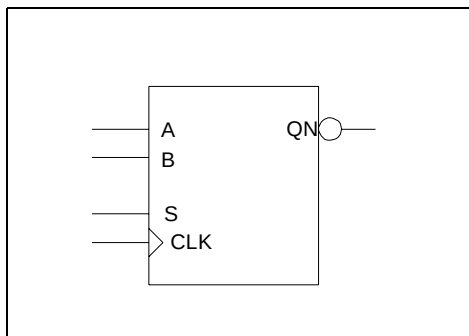
S	CLK	Q_{n+1}
0	↓	A
1	↓	B

Input A, B, S, CLK	Output Q
------------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

DFM1B_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

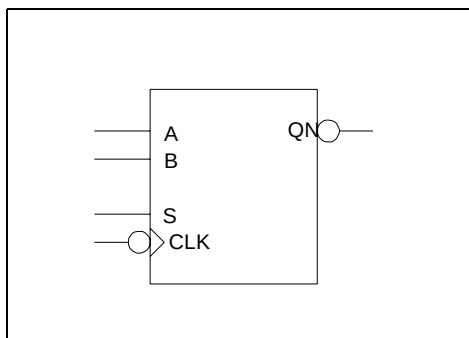
S	CLK	Q _N _{n+1}
0	↑	!A
1	↑	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All		2

DFM1C_CC

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

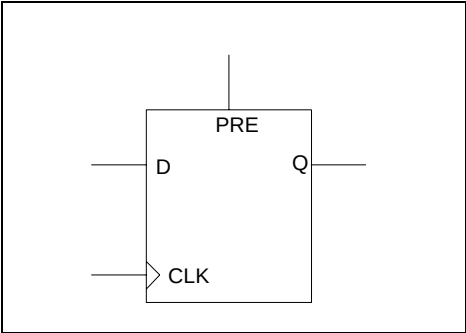
S	CLK	Q _N _{n+1}
0	↓	!A
1	↓	!B

Input	Output
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All		2

DFP1_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↑	D

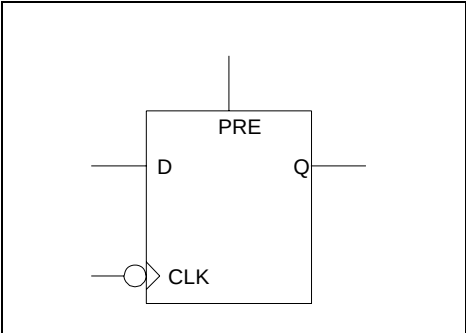
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1.

DFP1A_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↓	D

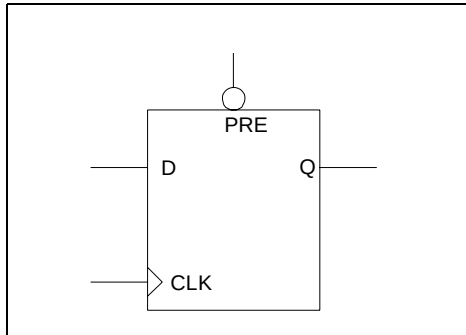
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1A.

DFP1B_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

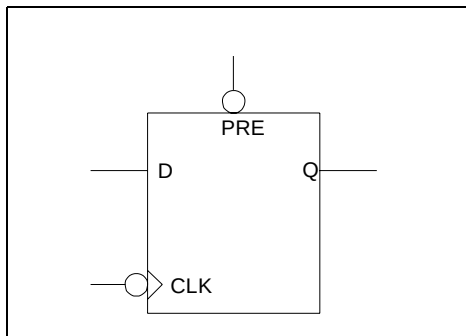
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1B.

DFP1D_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

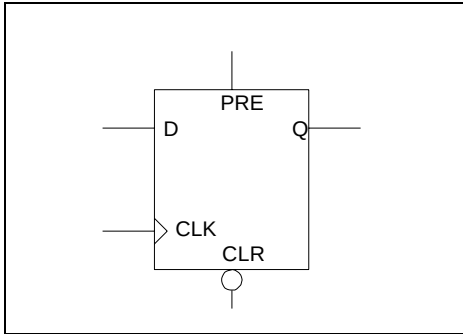
Input D, PRE, CLK	Output Q
-----------------------------	--------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1D.

DFPC_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	1	X	1
1	0	↓	D

Input
CLR, D, PRE, CLK

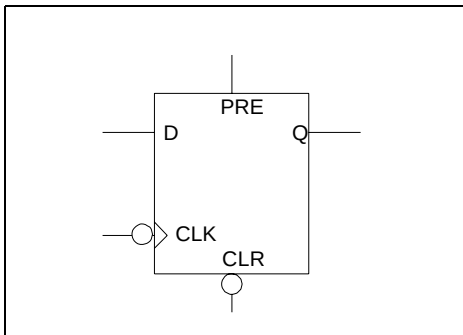
Output
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFPC.

DFPCA_CC*

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

Input
CLR, D, PRE, CLK

Output
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to Macro DFPCA.

** Your design should not allow both PRE and CLR to be asserted at the same time.

RAM Macros

RAM4FA

3200DX, 42MX,

RDAD5

RDAD4

RDAD3

READ2

RDAD1

RDAD0

RD3

RD2

RD1

RD0

WD3

WD2

WD1

WD0

WRAD5

WRAD4

WRAD3

WRAD2

WRAD1

WRAD0

WEN

BLKEN

BLKENS

WCLK

Input

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output

RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with falling Write clock and asynchronous Read

Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

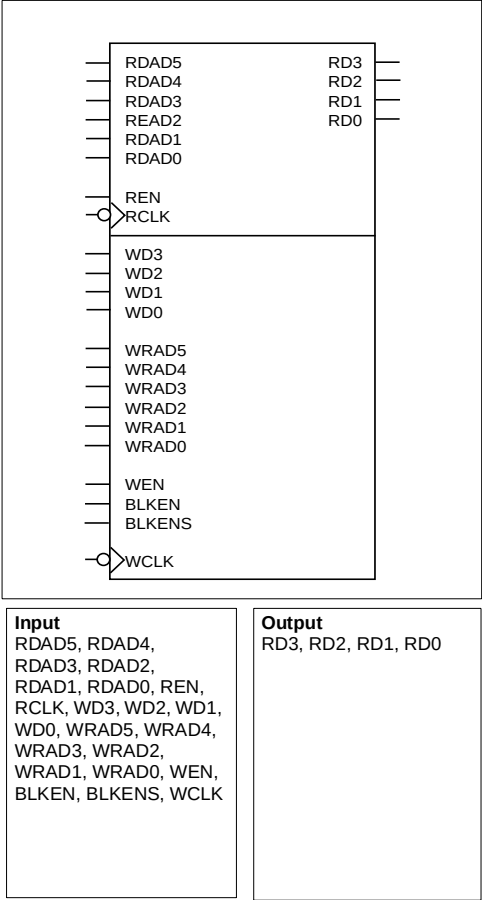
NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM4FF

3200DX, 42MX,



Function
64X4 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

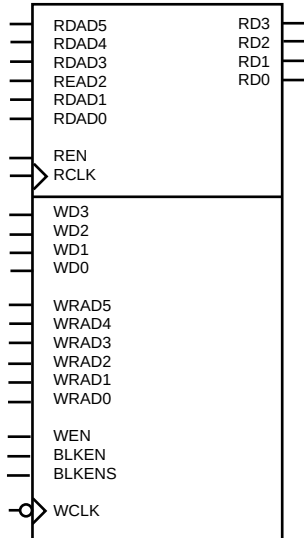
RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM4FR



Function

64X4 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

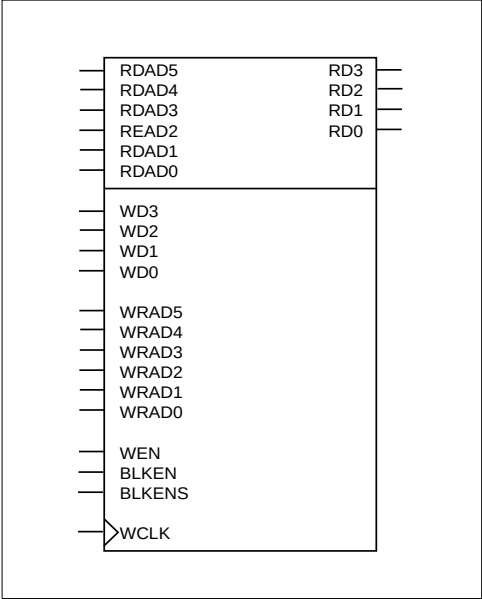
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM4RA

3200DX, 42MX,



Function
64X4 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

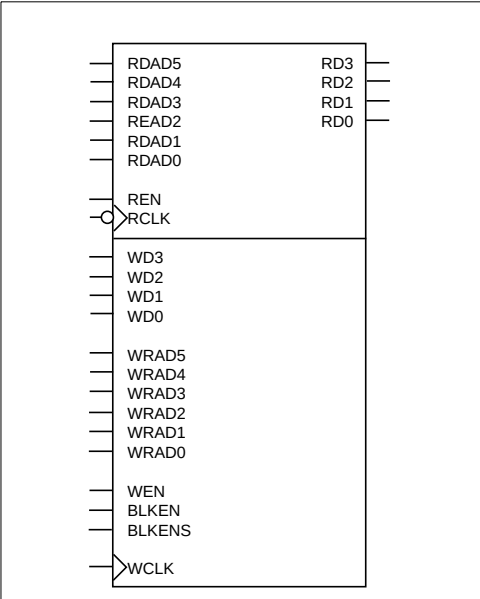
Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM4RF

3200DX, 42MX,



Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

Function
64X4 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

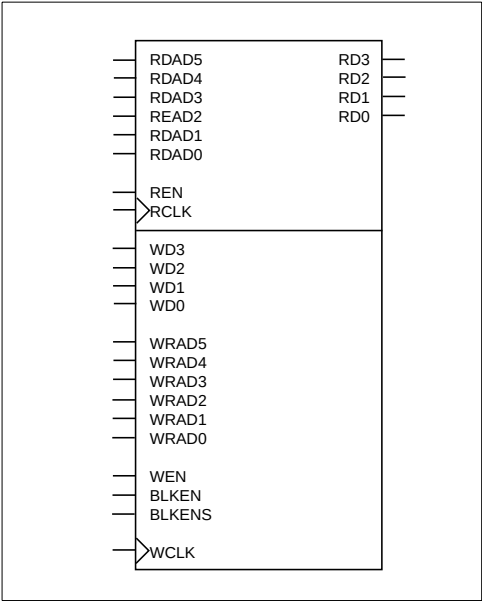
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM4RR

3200DX, 42MX,



Function
64X4 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Input
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8FA

3200DX, 42MX,

RDAD4

RDAD3

RDAD2

RDAD1

RDAD0

RD7

RD6

RD5

RD4

RD3

RD2

RD1

RD0

WD7

WD6

WD5

WD4

WD3

WD2

WD1

WD0

WRAD4

WRAD3

WRAD2

WRAD1

WRAD0

WEN

BLKEN

BLKENS

WCLK

Function

32X8 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Input

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

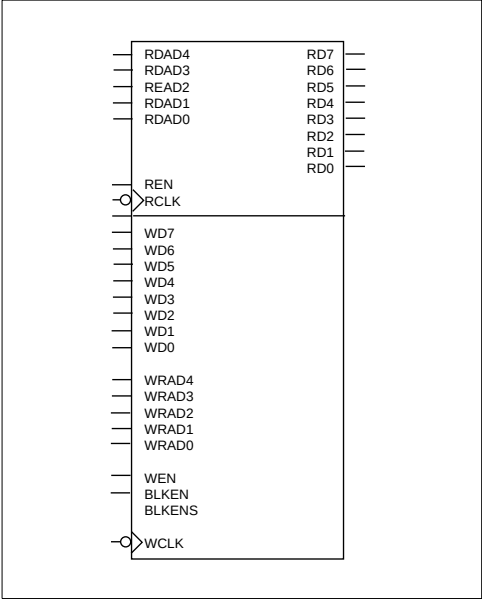
Output

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM8FF

3200DX, 42MX,



Input
RDAD4, RDAD3,
RDAD2, RDAD1,
RDAD0, REN, RCLK,
WD3, WD2, WD1, WD0,
WRAD4, WRAD3,
WRAD2, WRAD1,
WRAD0, WEN, BLKEN,
BLKENS, WCLK

Output
RD7, RD6, RD5, RD4,
RD3, RD2, RD1, RD0

Function
32X8 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

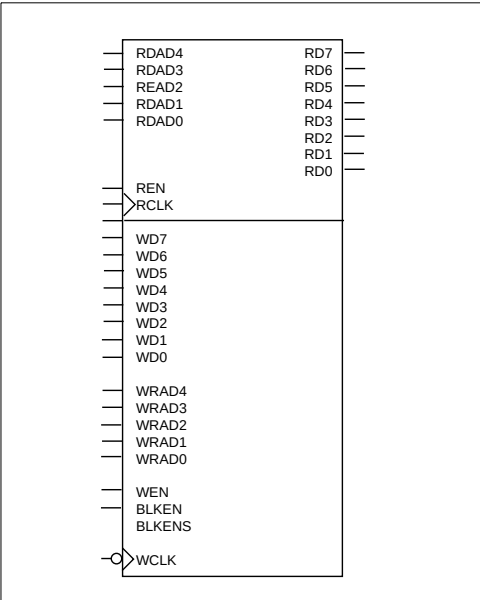
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8FR

3200DX, 42MX,



Function
32X8 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

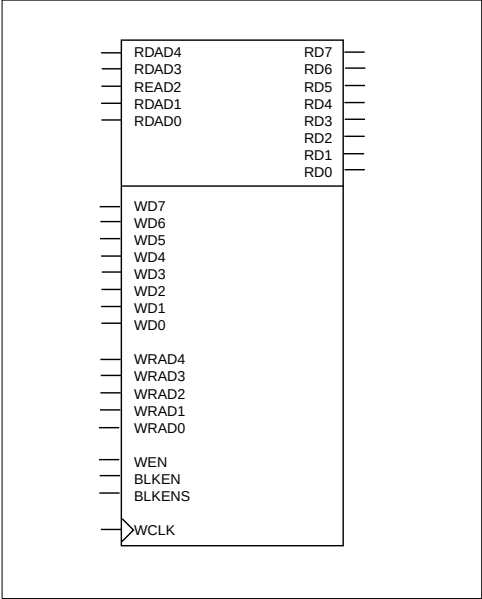
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8RA

3200DX, 42MX,



Function
32X8 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

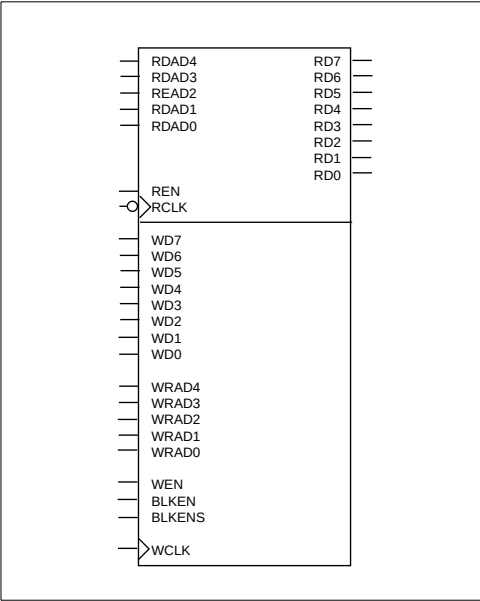
Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM8RF

3200DX, 42MX,



Input
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Output
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function
32X8 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

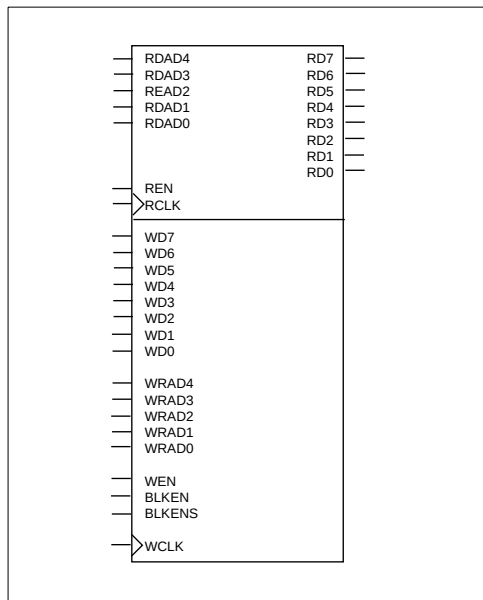
NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8RR

3200DX, 42MX,

**Input**

RDAD4, RDAD3,
RDAD2, RDAD1,
RDAD0, REN, RCLK,
WD7, WD6, WD5, WD4,
WD3, WD2, WD1, WD0,
WRAD4, WRAD3,
WRAD2, WRAD1,
WRAD0, WEN, BLKEN,
BLKENS, WCLK

Output

RD7, RD6, RD5, RD4,
RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

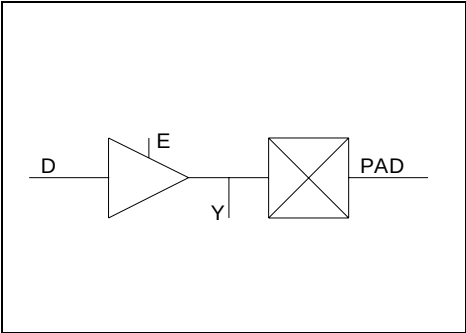
RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Family	Modules
	RAM
All	1

I/O Macros

BIBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

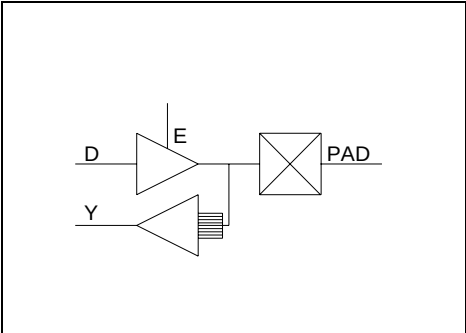
MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
All		1

CLKBIBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX



Function
Bidirectional with Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

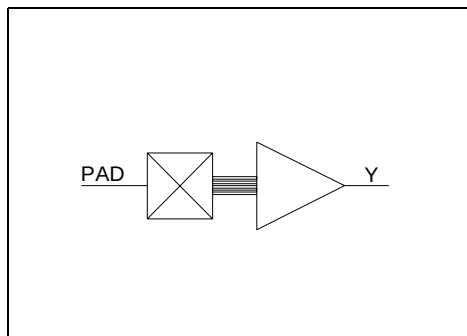
Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for more Clock Network information.

CLKBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX

**Function**

Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Input D, PAD	Output Y
------------------------	--------------------

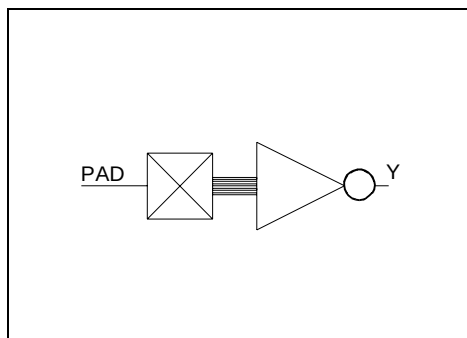
Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

CLKBUFI

54SX

**Function**

Inverting Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	1
1	0

Input PAD	Output Y
---------------------	--------------------

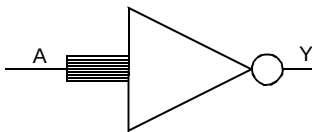
Family	Modules	
	Seq	I/O
54SX		1

NOTE 1: For an internal Clock net, refer to the CLKINTI macro.

NOTE 2: Refer to Actel's Databook for more Clock Network information.

CLKINTI

54SX



Function

Inverting Internal Clock Interface

Truth Table

A	Y
0	1
1	0

Input

A

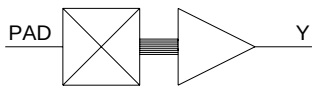
Output

Y

NOTE: CLKINTI does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

HCLKBUF

ACT 3, 54SX



Function

Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

Input

PAD

Output

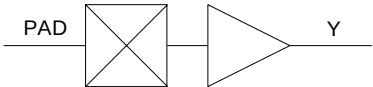
Y

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for more Clock Network information.

INBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

Input Buffer

Truth Table

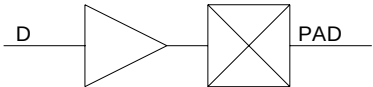
PAD	Y
0	0
1	1

Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All		1

OUTBUF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function

Output Buffer, High Slew

Truth Table

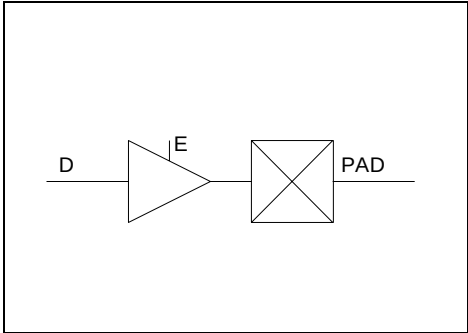
D	PAD
0	0
1	1

Input	Output
D	PAD

Family	Modules	
	Seq	I/O
All		1

TRIBUFF

ACT 1, ACT 2/1200XL, ACT 3, 3200DX, 40MX, 42MX, 54SX



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

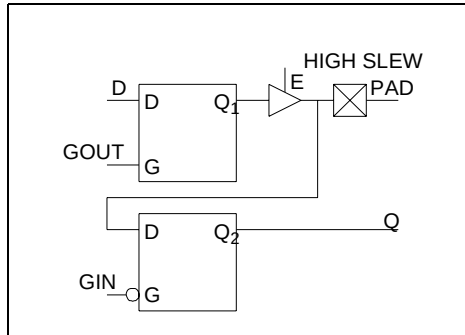
Input D, E	Output PAD
----------------------	----------------------

Family	Modules	
	Seq	I/O
All		1

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

BBDLHS

ACT 2/1200XL, 3200DX, 42MX



Function

Bidirectional with Input Latch and Output Latch

Truth Table

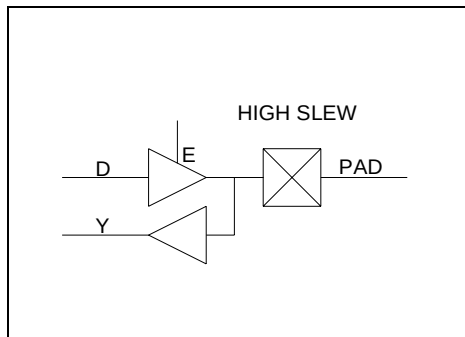
MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD _{n-1}	Q _{n-1}
	1	1	0	D	D
INPUT	0	X	1	X	Q _{n-1}
	0	X	0	X	PAD

Input D, E, GOUT, GIN, PAD	Output PAD, Q
--------------------------------------	-------------------------

Family	Modules	
	Seq	I/O
All		1

BBHS

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function

Bidirectional Buffer, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

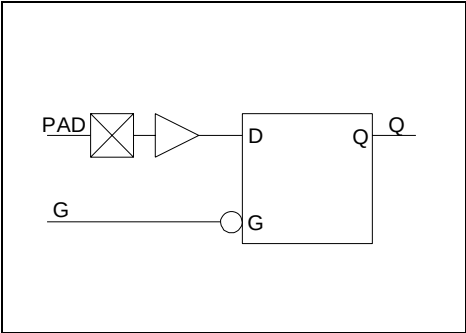
Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of BBHS we recommend that you use "BIBUF" on page 212.

IBDL

ACT 2/1200XL, 3200DX, 42MX



Function
Input Buffer with Input Latch, with active low Clock

Truth Table

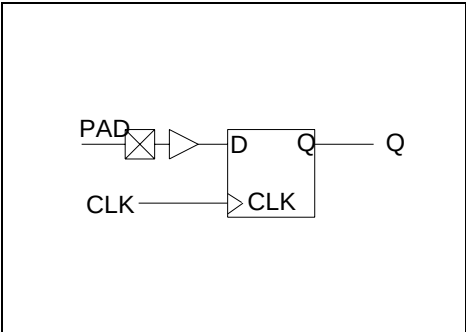
G	Q
1	Q_{n-1}
0	PAD

Input G, PAD	Output Q
------------------------	--------------------

Family	Modules	
	Seq	I/O
All		1

IR

ACT 2/1200XL, 3200DX, 42MX



Function
Input Register

Truth Table

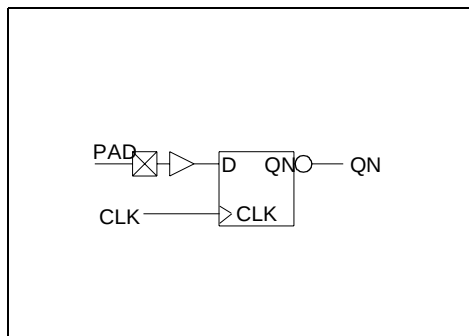
CLK	Q
↑	PAD

Input PAD, CLK	Output Q
--------------------------	--------------------

Family	Modules	
	Seq	I/O
All	1	1

IRI

ACT 2/1200XL, 3200DX, 42MX



Function

Input register with active Low output

Truth Table

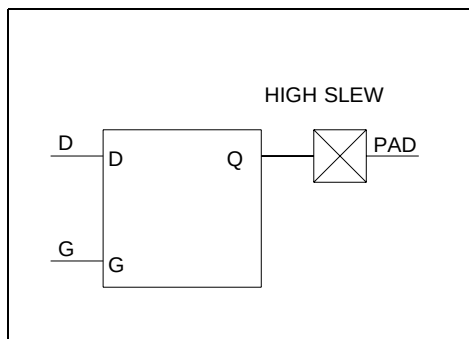
CLK	QN
↑	!PAD

Input PAD, CLK	Output QN
--------------------------	---------------------

Family	Modules	
	Seq	I/O
All	1	1

OBDLHS

ACT 2/1200XL, 3200DX, 42MX



Function

Output Buffer with Output Latch, High Slew

Truth Table

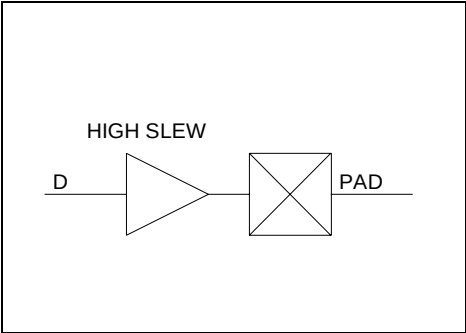
G	PAD
0	PAD _{n-1}
1	D

Input D, G	Output PAD
----------------------	----------------------

Family	Modules	
	Seq	I/O
All		1

OBHS

ACT 2/1200XL, ACT 3, 3200DX, 42MX



Function
Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

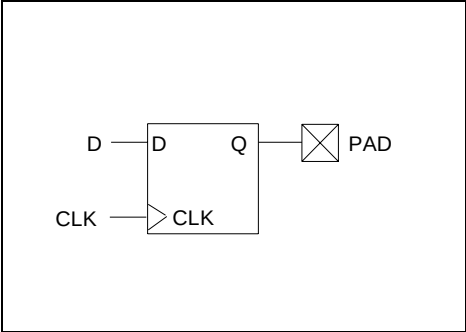
Input D	Output PAD
-------------------	----------------------

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of OBHS we recommend that you use “OUTBUF” on page 215.

ORH

ACT 2/1200XL, 3200DX, 42MX



Function
Output Register, High Slew

Truth Table

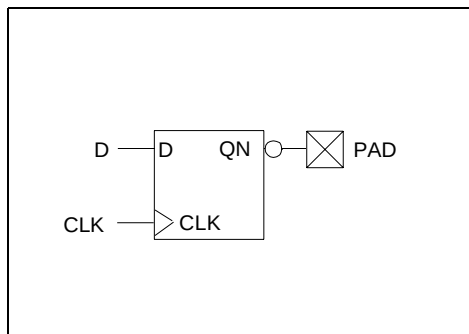
CLK	PAD _{n+1}
↑	D

Input D, CLK	Output PAD
------------------------	----------------------

Family	Modules	
	Seq	I/O
All	1	1

ORIH

ACT 2/1200XL, 3200DX, 42MX



Function

Inverted Output Register, High Slew

Truth Table

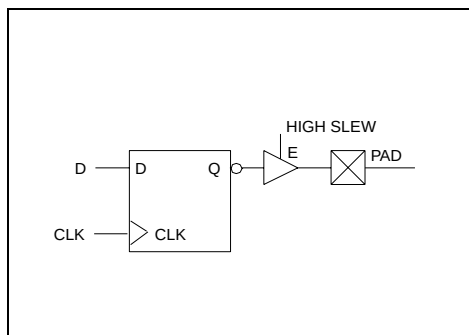
CLK	PAD _{n+1}
↑	!D

Input	Output
D, CLK	PAD

Family	Modules	
	Seq	I/O
All	1	1

ORITH

ACT 2/1200XL, 3200DX, 42MX



Function

Inverted Output Register, Tristate Enable, High Slew

Truth Table

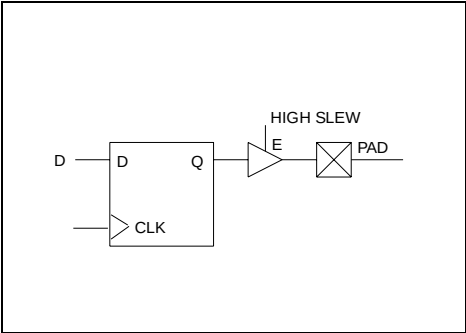
E	CLK	PAD _{n+1}
0	X	Z
1	↑	!D

Input	Output
D, E, CLK	PAD

Family	Modules	
	Seq	I/O
All	1	1

ORTH

ACT 2/1200XL, 3200DX, 42MX



Function
Output Register, Tristate Enable, High Slew

Truth Table

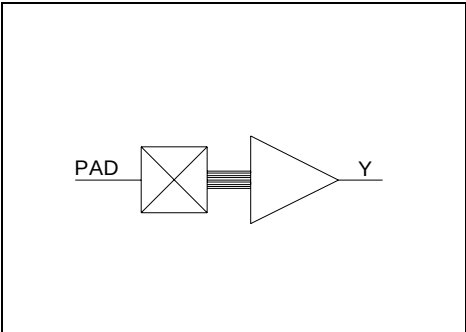
E	CLK	PAD _{n+1}
0	X	Z
1	↑	D

Input	Output
D, E, CLK	PAD

Family	Modules	
	Seq	I/O
All	1	1

QCLKBUF

ACT 2/1200XL, 3200DX, 42MX



Function
Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

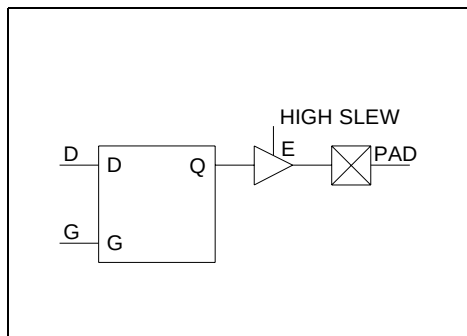
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
All		1

NOTE 1: For an internal Clock net, refer to the CLKINT macro.

TBDLHS

ACT 2/1200XL, 3200DX, 42MX

**Function**

Tristate Output with Latch, High Slew

Truth Table

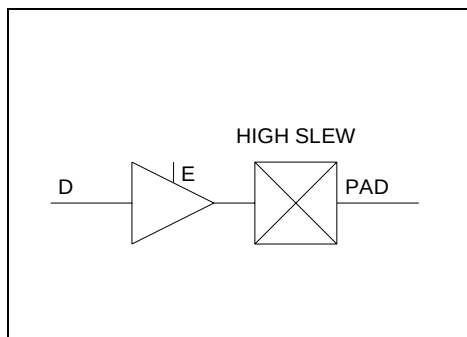
E	G	PAD
0	X	Z
1	1	D
1	0	PAD _{n-1}

Input	Output
D, E, G	PAD

Family	Modules	
	Seq	I/O
All		1

TBHS

ACT 2/1200XL, 3200DX, 42MX

**Function**

Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

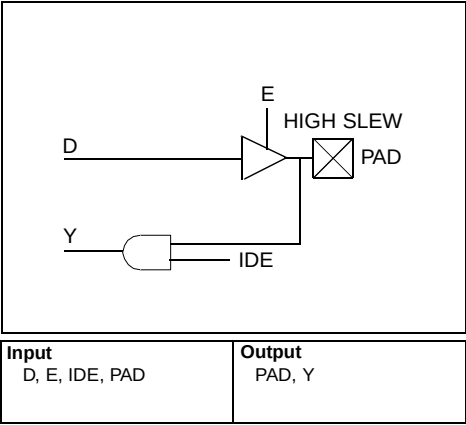
Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of TBHS we recommend that you use "TRIBUFF" on page 216.

BBHSA

ACT 3



Function
Bidirectional buffer with AND gate, High Slew

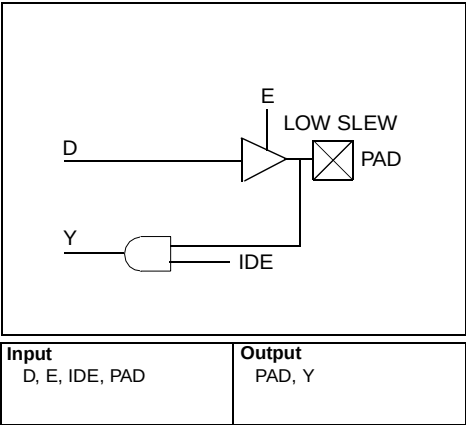
Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Family	Modules	
	Seq	I/O
ACT 3		1

BBLSA

ACT 3



Function
Bidirectional buffer with AND gate, Low Slew

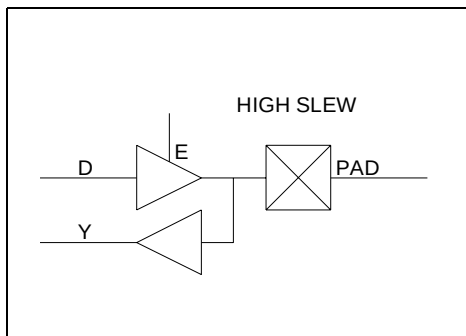
Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTH

ACT 3



Function

Bidirectional Buffer, Tristate Enable, High Slew

Truth Table

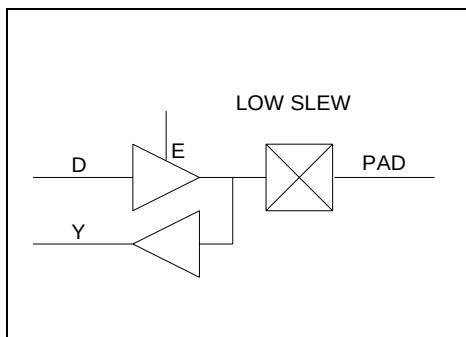
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTL

ACT 3



Function

Bidirectional Buffer, Tristate Enable, Low Slew

Truth Table

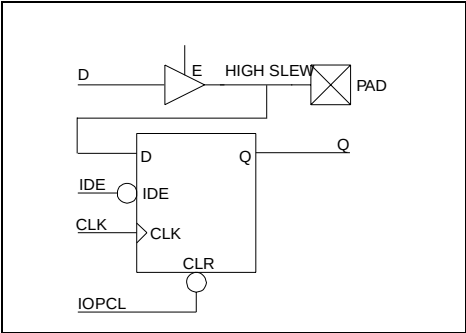
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Input D, E, PAD	Output PAD, Y
---------------------------	-------------------------

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTH

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

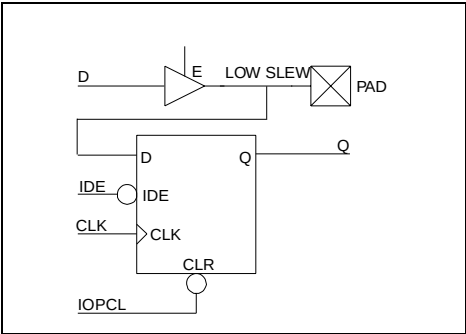
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTL

ACT 3



Input	Output
D, E, IDE, CLK, IOPCL, PAD	PAD, Q

Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

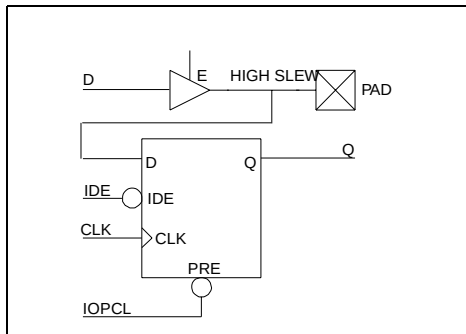
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPH

ACT 3



Input
D, E, IDE, CLK, IOPCL, PAD

Output
PAD, Q

Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

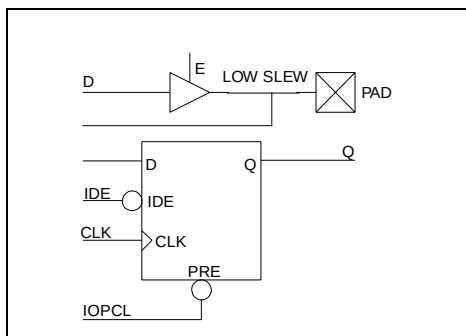
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTL

ACT 3



Input
D, E, IDE, CLK, IOPCL, PAD

Output
PAD, Q

Function

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

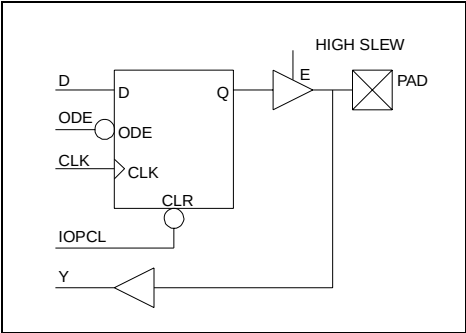
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTH

ACT 3



Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

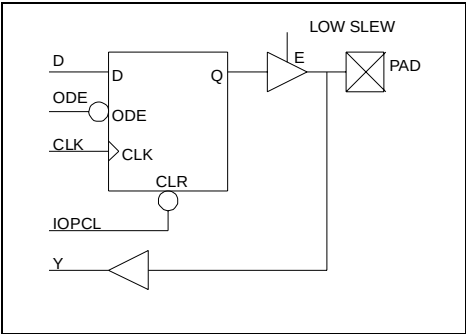
MODE	E	IOPC L	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTL

ACT 3



Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

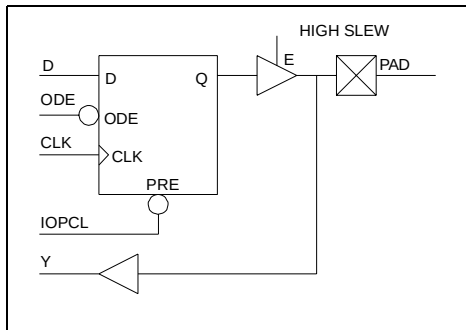
MODE	E	IOPC L	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTH

ACT 3



Function

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

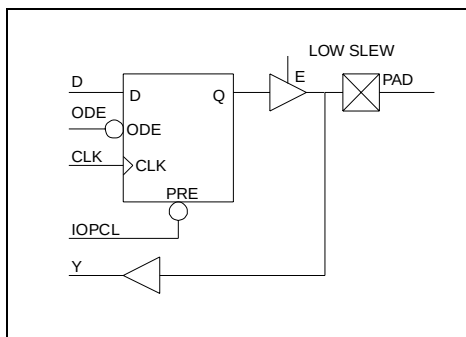
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTL

ACT 3



Function

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

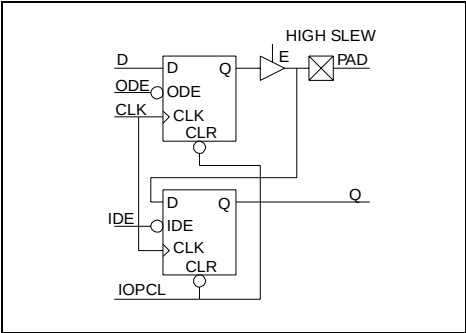
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

DECETH

ACT 3



Input	Output
D, E, ODE, CLK, IOPCL, PAD	PAD, Q

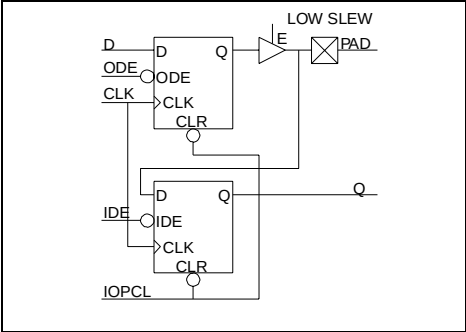
Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table							
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

DECETL

ACT 3



Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD	PAD, Q

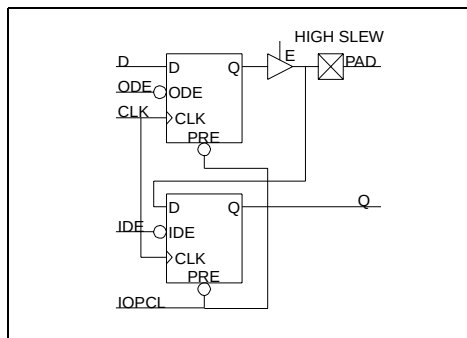
Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table							
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETH

ACT 3



Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD	PAD, Q

Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

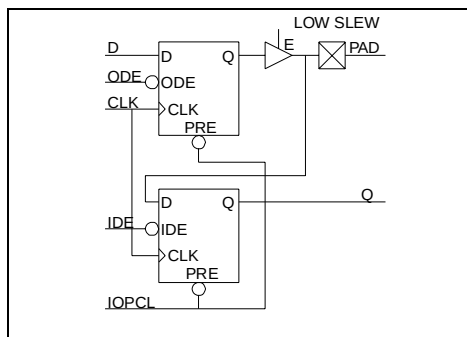
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETL

ACT 3



Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD	PAD, Q

Function

Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

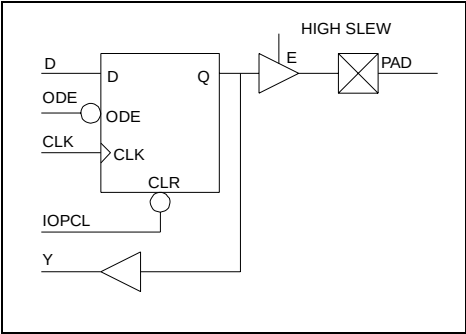
Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

FECTH

ACT 3



Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

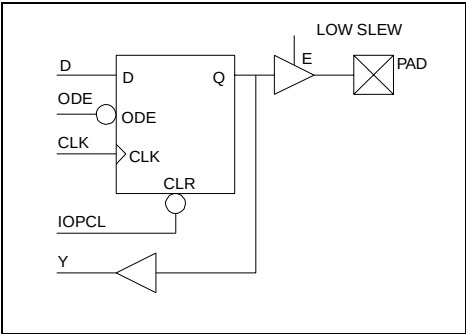
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FECTL

ACT 3



Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

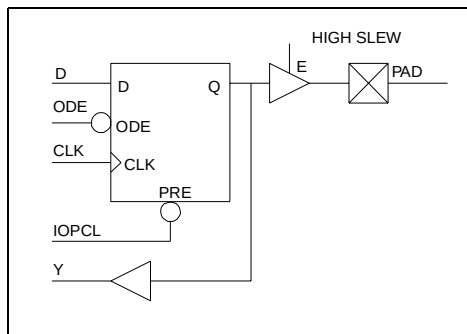
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTH

ACT 3



Input
D, E, ODE, CLK, IDE, IOPCL,
PAD

Output
PAD, Y

Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

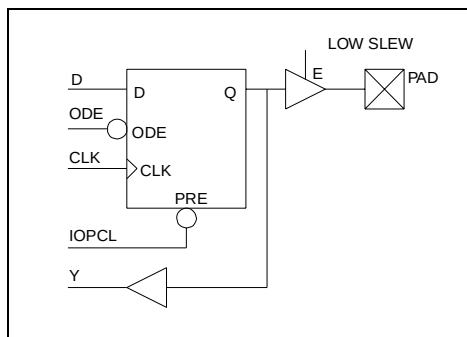
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTL

ACT 3



Input
D, E, ODE, CLK, IDE, IOPCL,
PAD

Output
PAD, Y

Function

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

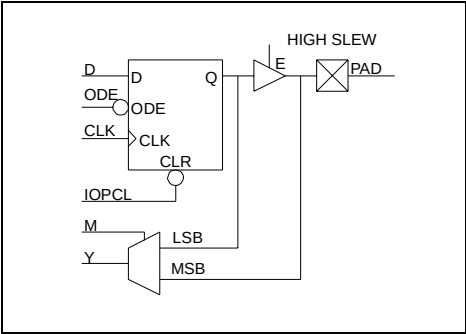
Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

FECTMH

ACT 3



Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD, M	PAD, Y

Function
Output Register with Muxed Feedback, with Clear, Output Data Enable, Tristate Enable, High Slew

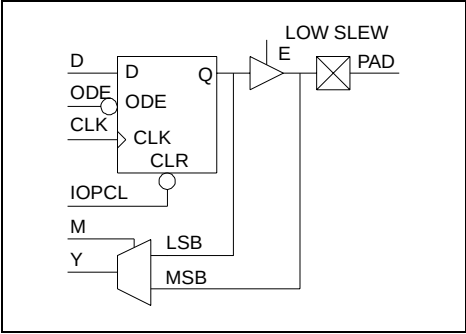
Truth Table							
MOD E	E	IOP CL	OD E	CL K	PA D	M	Y
OUTP UT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PA D _{n-1}	X	Y _{n-1}
INPU T	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PA D

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FECTML

ACT 3



Input	Output
D, E, ODE, CLK, IDE, IOPCL, PAD, M	PAD, Y

Function
Output Register with Muxed Feedback, with Clear, Output Data Enable, Tristate Enable, Low Slew

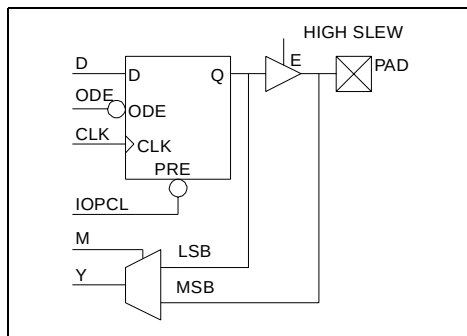
Truth Table							
MOD E	E	IOP CL	OD E	CL K	PA D	M	Y
OUTP UT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PA D _{n-1}	X	Y _{n-1}
INPU T	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PA D

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTMH

ACT 3



Input
D, E, ODE, CLK, IDE, IOPCL,
PAD, M

Output
PAD, Y

Function

Output Register with Muxed Feedback, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table ¹

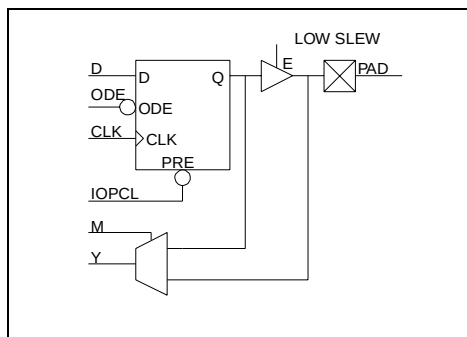
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

FEPTML

ACT 3



Input
D, E, ODE, CLK, IDE, IOPCL,
PAD, M

Output
PAD, Y

Function

Output Register with Muxed Feedback, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table ¹

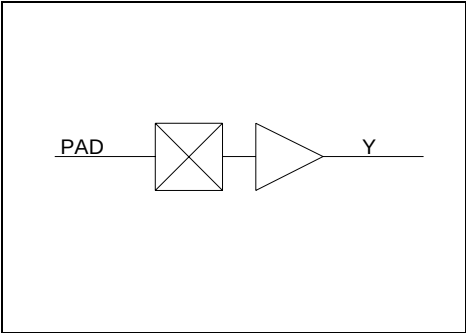
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

IBUF

ACT 3



Function
Input Buffer

Truth Table

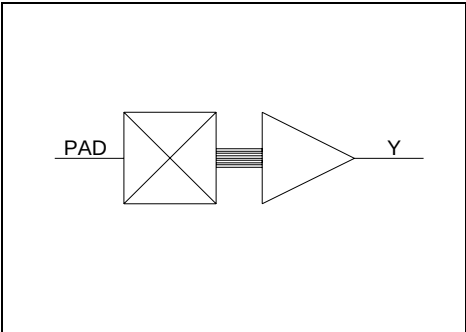
PAD	Y
0	0
1	1

Input PAD	Output Y
---------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

IOCLKBUF

ACT 3



Function
Dedicated I/O Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

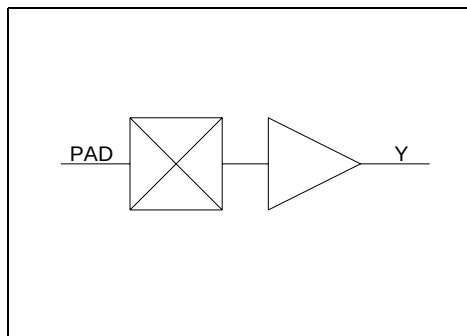
Input PAD	Output Y
---------------------	--------------------

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IOPCLBUF

ACT 3



Function

Dedicated I/O Preset Clear Buffer

Truth Table

PAD	Y
0	0
1	1

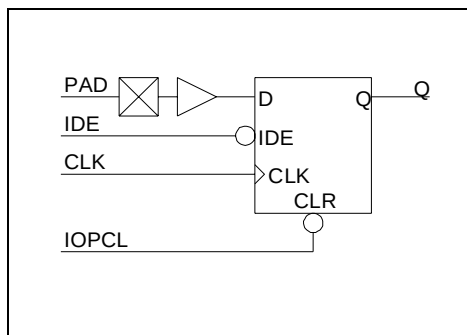
Input	Output
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

NOTE: Refer to Actel's Databook for more Clock Network information.

IREC

ACT 3



Function

Input Register, with Clear, Input Data Enable

Truth Table

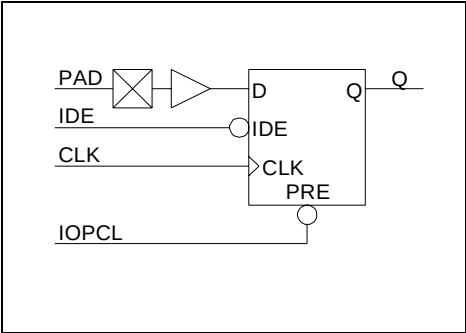
IOPCL	IDE	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	PAD

Input	Output
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

IREP

ACT 3



Function
Input Register, with Preset, Input Data Enable

Truth Table

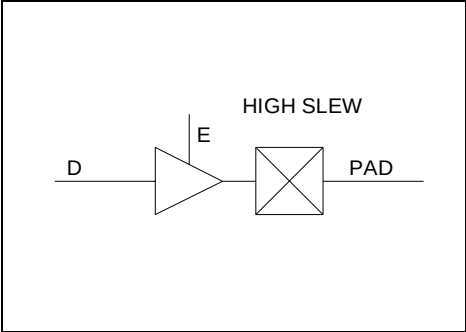
IOPCL	IDE	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	PAD

Input	Output
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTH

ACT 3



Function
Output Buffer, Tristate Enable, High Slew

Truth Table

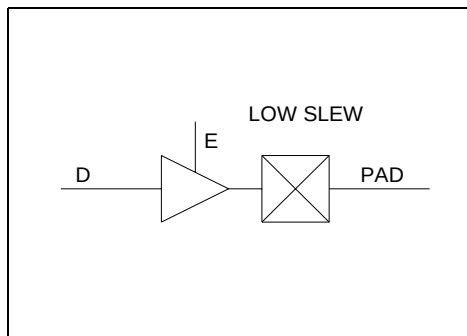
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E, PAD	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTL

ACT 3



Function

Output Buffer, Tristate Enable, Low Slew

Truth Table

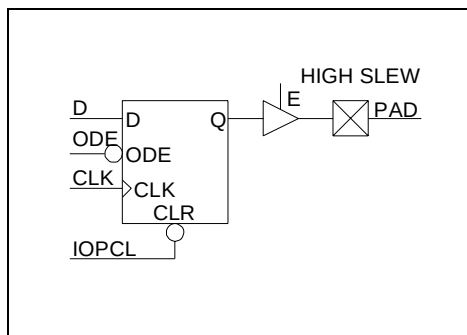
D	E	PAD
X	0	Z
0	1	0
1	1	1

Input	Output
D, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTH

ACT 3



Function

Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

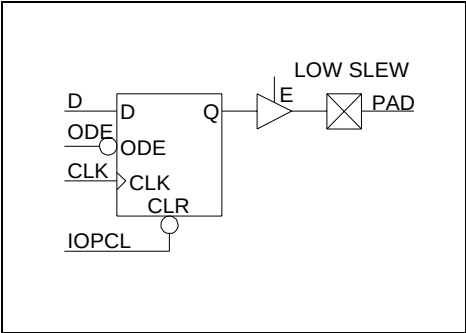
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTL

ACT 3



Function
Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

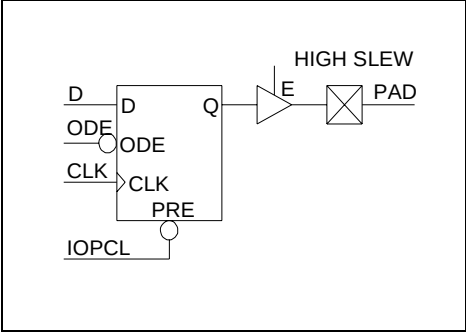
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTH

ACT 3



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

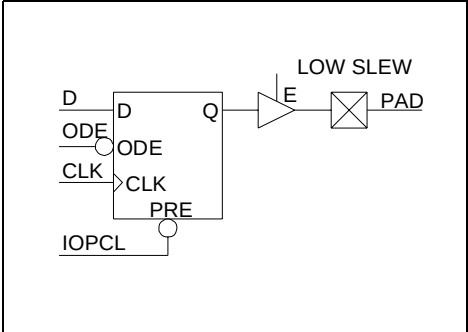
IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input	Output
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTL

ACT 3



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Input D, ODE, CLK, IOPCL, E	Output PAD
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Family	Modules	
	Seq	I/O
ACT 3		1

