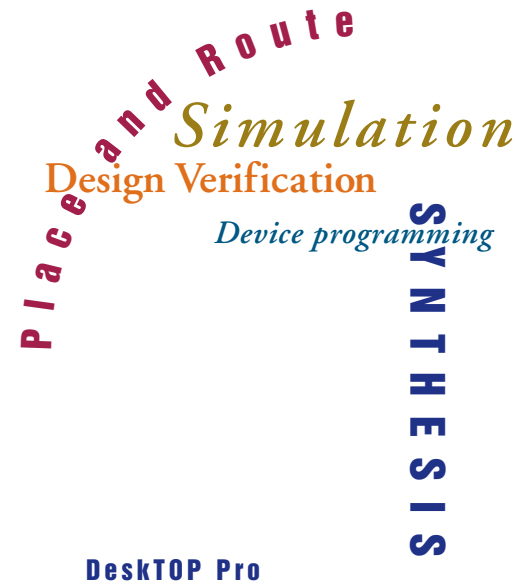


Actel DeskTOP Series

Integrated FPGA Design Tools

The Actel DeskTOP series is an alliance between Actel, Synplicity, and VeriBest that combines the best in FPGA silicon, synthesis, and simulation to provide an integrated tool set for logic designers today. Committed to making the FPGA design process as effortless as possible, the DeskTOP series offers designers an intuitive design flow in an easy to use, integrated design environment.

The DeskTOP series allows designers to move up to more powerful tools as their FPGA density requirements grow. All major design methodologies are supported, offering designers the flexibility to design using their preferred design entry method.

Designers now have an integrated tool set that enables them to move rapidly and efficiently from concept to silicon. The Actel DeskTOP series provides a flexible environment to design Actel FPGAs and to take advantage of the inherent benefits of antifuse–saving time and money.

DeskTOP

The Complete, Integrated Solution

Ideal for designers who work in low densities, DeskTOP allows synthesis of selected Actel devices up to 50K gates and contains all the tools necessary for designing Actel FPGAs.

DeskTOP Pro

Upward Mobility

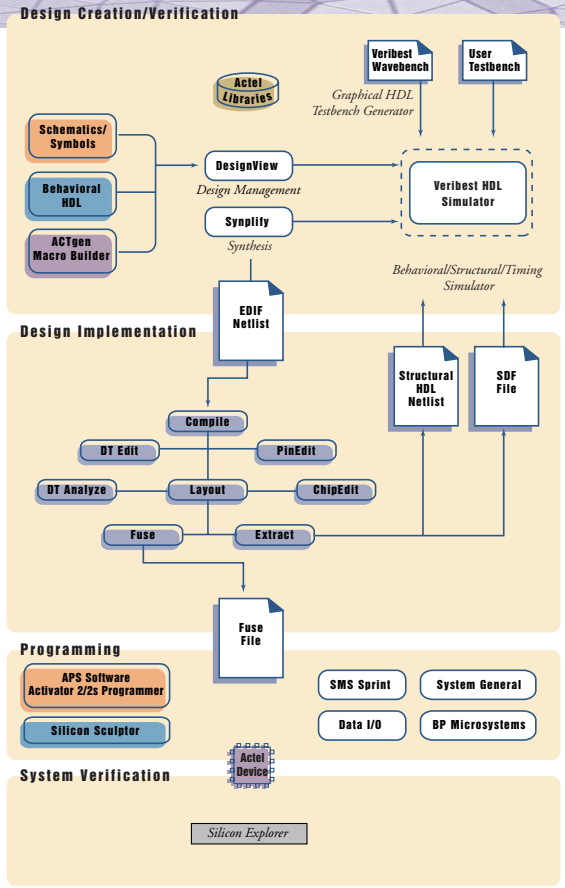
For designers who want to move to higher densities, DeskTOP Pro, in addition to the tools and capabilities offered by DeskTOP, allows simulation of designs as large as 400K gates and unlimited synthesis. DeskTOP Pro also includes VeriBest's State Diagram Editor and Synplicity's SCOPE HDL Constraints Editor to increase productivity.

DeskTOP Open

Open Synthesis

ASIC designers are increasingly using FPGAs for their designs and have invested heavily in synthesis tools. These designers use a broad range of densities but are familiar with an ASIC tool flow. DeskTOP Open fills this need by allowing designers to choose a synthesis tool from industry leading synthesis vendors, while still providing all of the other tools available in DeskTOP Pro. DeskTop Open currently supports Synplicity Synplify and Synopsys FPGA Express synthesis tools.

Actel



DeskTOP Series Tools

VeriBest DesignView design management environment integrates the design flow and tools. It includes Schematic and HDL design entry and supports mixed mode entry in which HDL and schematic symbols can be mixed (All DeskTOP series packages).

VeriBest Schematic/HDL Editor specifically targets the creation of HDL code. HDL Editor supports VHDL and Verilog while color coding keywords of the HDL language, allowing designers to easily verify that the coding is correct (All DeskTOP series packages).

VeriBest WaveBench graphical test bench generation tool, ideal for designers unfamiliar with the process of creating test benches, automatically converts stimulus files into HDL test benches and maintains multiple test benches. It also allows designers to create complex formula based waveforms in Excel and easily transfer them into WaveBench (All DeskTOP series packages).

VeriBest VHDL Simulator enables source level verification that allows designers to verify HDL code line by line. Behavioral simulation capabilities make pre-synthesis simulation possible, enabling designers to catch and correct errors early in the process. Structural and timing simulation can also be performed (All DeskTOP series packages).

VeriBest State Diagram Editor generates graphical state machines in high level design. This tool saves designers the difficult task of generating the HDL code themselves (DeskTOP Pro and DeskTOP Open only).

Synplicity Synplify/Synplify Lite synthesis tool is integrated as part of the design flow in the design management environment (DeskTOP Pro and DeskTOP only).

Synplicity SCOPE HDL Constraints Editor allows the designer to set timing constraints in the design (DeskTOP Pro only).

Actel Designer Advantage/Lite place and route software with the capability to fix pins, modify placed gates, export programming files, and perform timing analysis and design verification (All DeskTOP series packages).

Actel Silicon Explorer accelerates device verification. Actel's antifuse FPGAs contain ActionProbe circuitry that provides built-in, no-cost access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that attaches to a PC's standard COM port, turning the PC into a fully functional logic analyzer (All DeskTOP series packages).

Product	Design Entry	Synthesis	Simulation	Place and Route	Programming*	Additional Tools
DeskTOP	VeriBest *(Schematic, HDL)*	Synplify-Lite *(32k gate limit)*	VeriBest *(50k gate limit)*	Designer Lite *(32k gate limit)*	APS, Silicon Sculptor	WaveBench Silicon Explorer
DeskTOP Pro	VeriBest *(Schematic, HDL)*	Synplify *(no limit)*	VeriBest *(400k gate limit)*	Designer Advantage *(no limit)*	APS, Silicon Sculptor	WaveBench SCOPE HDL Constants Editor State Diagram Editor Silicon Explorer
DeskTOP Open	VeriBest *(Schematic, HDL)*	None	VeriBest *(400k gate limit)*	Designer Advantage *(no limit)*	APS, Silicon Sculptor	WaveBench State Diagram Editor Silicon Explorer

*Device Programmers must be purchased separately

For more information about Actel's products, call 1.888.99.ACTEL or visit our Web site at http://www.actel.com

Actel Corporation • 955 East Arques Avenue • Sunnyvale, California 94086 • USA
Tel: 408.739.1010 • Fax: 408.739.1540
Actel Europe, Ltd. • Daneshill House, Lutyens Close • Basingstoke, Hampshire RG24 8AG • United Kingdom
Tel: +44.(0)1256.305600 • Fax: +44.(0)1256.355420
Actel Japan • EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan
Tel: +81.(0)3.3445.7671 • Fax: +81.(0)3.3445.7668

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