ChipEditor v6.1 User's Guide

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Welcome to ChipEditor

ChipEditor is a graphical application for viewing and assigning I/O and logic macros. This tool is particularly useful when you need maximum control over your design placement.

Note: ChipEditor supports the ACT1, ACT2, ACT3, MX, DX, eX, SX, and SX-A families.

If you are designing for the ProASIC3E, ProASIC3, ProASIC PLUS, Axcelerator, and ProASIC families, use ChipPlanner. See the MultiView Navigator User's Guide for more information.

Use ChipEditor to:

- View macro assignments made during layout
- Assign, unassign, or move macros
- Lock macro assignments
- View net connections using a Ratsnest, Minimum Spanning Tree, or Route view
- View architectural boundaries
- View and edit silicon features
- Select probes when used with Silicon Explorer
- View assignment and routing of paths when used with Timer

Starting and Exiting ChipEditor

To start ChipEditor:

1. If you have not done so, compile your design.
2. From the **Tools** menu, choose **ChipEditor**, or click the ChipEditor icon in the Designer Design Flow window. ChipEditor opens in a separate window.

To exit ChipEditor, from the **File** menu, choose **Close**. If you haven't committed your changes, you will be asked if you want to commit your changes**.**

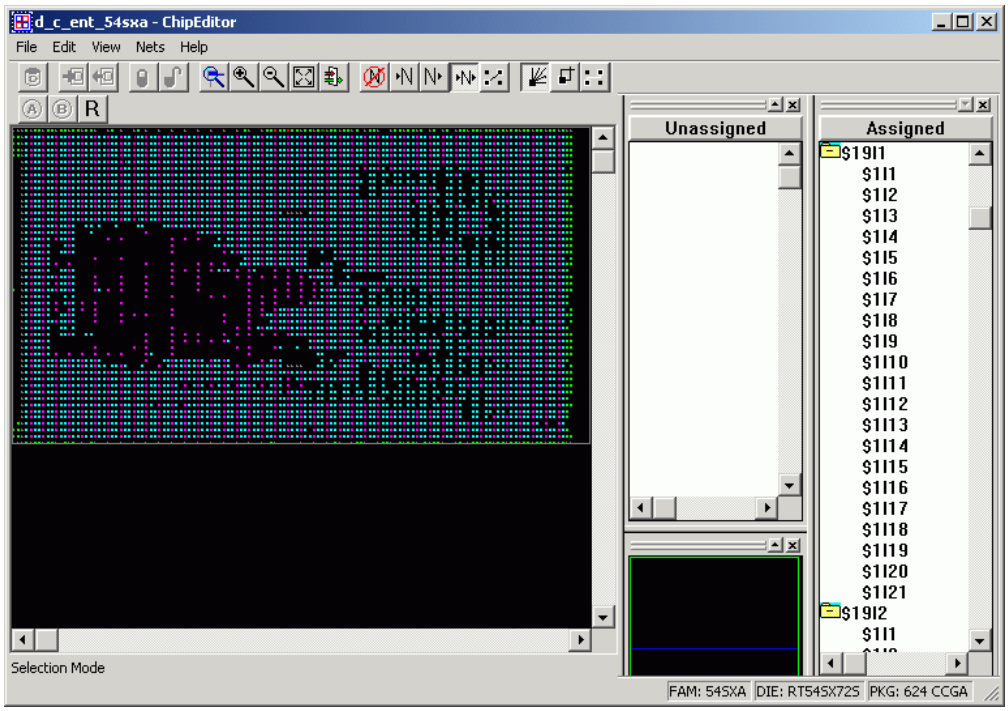
Components of ChipEditor

The ChipEditor interface is divided into four windows:

- ChipView window - view your design elements
- Assigned list box - assign macros to pins
- Unassigned list box- unassign macros from pins
- World View window - select the area of the design to display in the Package window

These windows are highly integrated; anything selected in one is selected or highlighted in all. Commands are accessible from the menu bar and frequently-used commands are on the toolbar.

All the windows and bars are independently sizeable, dockable, and closable. In UNIX, floating windows are not sizeable. To redock or refloat a window, simply double-click the window's title bar.



ChipEditor Standalone

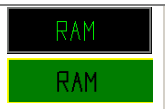
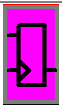
ChipView window

The ChipEditor ChipView window displays logic modules and assigned macros. When you select a macro in the ChipView window, the macro location is highlighted in the World View window and the macro name is selected in the Assigned list box.

To see a magnified or reduced view of your design, use the **Zoom** commands in the **View** menu or toolbar. To use hot keys, place your mouse over the desired zoom area and use **SHIFT** and the "+" plus key to zoom in on the location and **SHIFT** and the "-" minus key to zoom out.

Colors and Symbols

Colors and symbols differentiate the I/O and logic macros in ChipEditor. The following table defines the default colors assigned to symbols. You can change these colors per design.

Color/Symbol	Definition
White Border	A white border denotes a selected object.
Black Background	A black background denotes an unused or unassigned module.
Blue	Blue denotes a combinatorial module.
Yellow	Yellow denotes *locked* logic modules. If the module is selected, the symbol appears yellow. If the module is unselected, the border appears yellow.
Green	Green denotes I/O modules.
Red	Red denotes clock modules.
Magenta	Magenta denotes sequential modules.
	Reserved modules that are not user definable are gray, crossed-out symbols on a black background.
	Clock modules are red. Unused/unassigned modules are red symbols on a black background. Used/assigned modules are black symbols on a red background.
	Input/Output modules are green. Unused/unassigned modules are green symbols on a black background. Used/assigned modules are black symbols on a green background.
	Combinatorial modules are blue. Unused/unassigned modules are blue symbols on a black background. Used/assigned modules are black symbols on a blue background.
	Sequential modules are magenta. Unused/unassigned modules are magenta symbols on a black background. Used/assigned modules are black symbols on a magenta background.
	Buffer modules are blue.
	RAM modules are green. Unused/unassigned modules are green symbols (RAM) on a black background. Used/assigned modules are black on a green background.
	PLL modules are green. Unused/unassigned modules are green symbols (PLL) on a black background. Used/assigned modules are black on a green background.
	I/O Inbuff modules are pink on a black background. Used/assigned modules are black on a pink background.

Assigned and Unassigned List Boxes

The **Assigned** and **Unassigned** list boxes display assigned or unassigned macros in the design. By default, all assigned macros appear in the Assigned list box and all unassigned macros appear in the Unassigned list box.

You can filter which macros are visible in these list boxes. To customize the **Assign** and **Unassign** list boxes, from the **View** menu, choose **Configure List Boxes**.

World View Window

Use the World View window to control which portion of the ChipView is displayed in the ChipView window. The blue rectangle (known as the ChipView rectangle) represents the chip. The green rectangle (known as the Viewing rectangle) represents the area displayed in the ChipView window.

To move the displayed area to another part of the chip, click the left mouse button and drag the **Viewing rectangle** to the area on the **ChipView rectangle** you would like to display. To specify a new display area, click the right mouse button and drag out a new **Viewing rectangle** on the **ChipView rectangle**.

Status Bar

Family, die, and package information appears in the right corner of the status bar. In addition, the status bar displays information on commands, pins, placed macros, nets, error messages, and the family, die, and package.

- Hold your mouse over an assigned macro in the **ChipView** window to see the pin number, instance name, net name, macro cell, and locked or unlocked status in the status bar.
- Select a macro, zoom in, and click one of the **Ratsnest** lines to see nets displayed in the status bar.
- Hold your mouse over a toolbar button or menu command to see a short description of the command in the status bar.

Error messages in the status bar provide details about invalid assignment attempts. From the **Help** menu, choose **Extended Error Messages** to view more information about the last failed command or assignment attempt.

Changing an Object's Color

Customize the colors used to display nets, clusters, and SuperClusters in the ChipView window by using the Color Manager.

To customize colors in the ChipView window:

1. From the **View** menu, choose **Color Manager**.
2. In the Color Manager, click the color box in front of the net, cluster, or SuperCluster to change.
3. In the Color dialog box, select a new color for the item, and then click **OK**. The new color appears in the Color Manager dialog box.
4. When finished customizing colors, click **OK**. The nets, clusters, and SuperClusters will appear in their newly assigned colors.

Color Manager Dialog Box

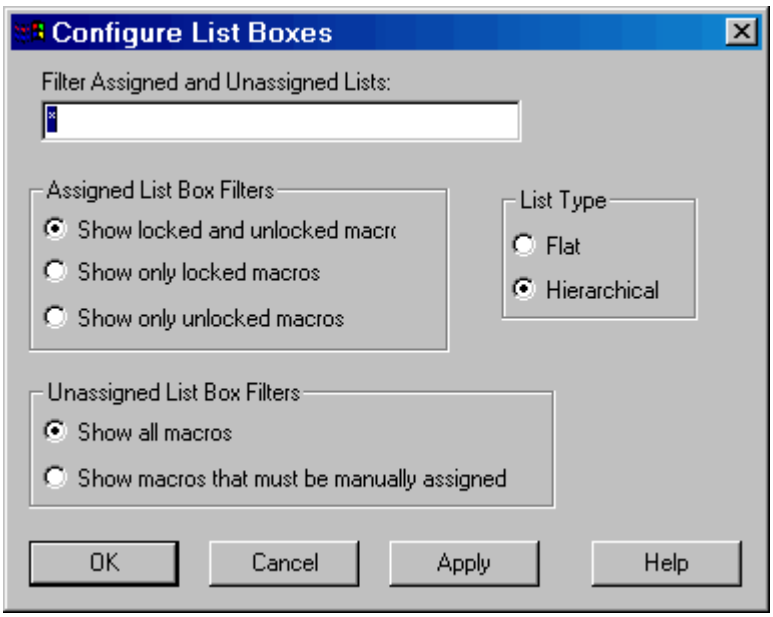
Customizing Assigned and Unassigned list boxes

The ChipEditor **Assigned** and **Unassigned** list boxes display all assigned and unassigned macros in the design. All assigned macros appear in the Assigned list box and all unassigned macros appear in the Unassigned list box.

You can customize which macros are visible in the Assigned and Unassigned list boxes.

To customize the list boxes:

1. From the View menu, choose Configure List Boxes.
   - **Filter Assigned and Unassigned Lists** - Entering a specific macro name in this field filters out all other macros in the Assigned and Unassigned List Boxes. Use the * wildcard character to filter for groups.
   - **Show locked and unlocked macros** - Select this option to display all locked and unlocked macros in the Assigned list box.
   - **Show only locked macros** - Select this option to filter out all unlocked macros from the Assigned list box.
   - **Show only unlocked macros** - Select this option to filter out all locked macros from the Assigned list box.
   - **Show all macros**: Select this option to display all the macros in the Unassigned list box.
   - **Show macros that must be manually assigned** - Select this option to display only the macros that must be manually assigned in the Unassigned list box.
   - **List Type** - Use the List Type filters to display macro instance names in a flat or hierarchical list in the Assigned and Unassigned list boxes. When instance names are displayed hierarchically, collapsed levels are preceded by a plus sign (+) and expanded levels are preceded by a minus sign (-). Clicking the plus sign expands the hierarchy of a macro, while clicking the minus sign collapses the hierarchy. Macros, both locked and unlocked, are displayed hierarchically by default.
2. Click **Apply** to see changes. When done, click **OK**.



Configure List Boxes Dialog Box

Committing Changes

Changes you make are not permanent until you use the Commit command. The Commit command saves your changes to your design session. Changes are not reversible. To commit your changes, from the **File** menu, choose **Commit**.

Assigning Logic

Manually assigning logic is an optional methodology to help you improve the performance and density of your design.

You do not need to manually assign logic in your design. However, should you have specific design requirements, ChipEditor allows you to have maximum control over your design. You can use ChipEditor before and/or after running **Layout** to place and route your design.

To assign logic using ChipEditor:

1. Select the logic in the **Unassigned** list box.
2. Drag the logic to the desired location in the **ChipEditor** window.

If the logic placement is valid, the logic is assigned. To remove the placement, from the **Edit** menu, choose **Unassign**.

Error messages in the status bar notify you about invalid placement attempts. Choose **Extended Error Message** from the Help menu for more details on a specific error message. If you want to ensure that the logic is not moved during layout, you must Lock the logic assignment and commit your changes before exiting ChipEditor.

Note: Assigning logic to a location that already has logic unassigns the previously assigned logic, even if its assignment was locked.

To assign multiple logic macros:

1. While holding down the **CTRL** or **SHIFT** key, select the logic in the order you want it assigned.
2. From the **Edit** menu, choose **Assign**.
3. One by one, select the desired location. The macros are assigned in the order selected.

To unassign logic:

1. Select the logic.
2. From the **Edit** menu, choose **Unassign**.

To unassign multiple logic macros:

1. Hold down the **CTRL** or **SHIFT** key and select the logic you want to unassign. To select all logic, from the **Edit** menu, choose **Select All**. To select all assigned logic, from the **Edit** menu, choose **Select All Assigned**.
2. From the **Edit** menu, choose **Unassign**.

Moving Logic to Other Locations

You can move logic that was assigned manually or automatically during Layout.

To move logic:

1. Select the logic to move.
2. Drag the logic to the new location.

Tip: To remove the assigned macro, from the **Edit** menu, choose **Unassign**.

Locking Logic to Locations

Locked logic is not moved during Layout. Locked logic only becomes permanent if you commit the changes to your design before exiting.

To lock macros:

1. Select the macro to lock. To select multiple macros, hold down the **CTRL** key and select multiple macros. To select all macros, from the **Edit** menu, choose **Select All**.
2. From the **Edit** menu, choose **Lock**.
3. From the **File** menu, choose **Commit** to make the changes permanent and update your .adb file.

To unlock a macro:

1. Select the macro. To select multiple macros, hold down the **CTRL** key and select multiple macros. To select all macros, from the **Edit** menu, choose **Select All**.
2. From the **Edit** menu, choose **Unlock**.

Ratsnest View

The Ratsnest view displays net connectivity between assigned logic macros by connecting lines from the output pins to all input pins. Use the Ratsnest to understand how logic macros are connected to each other. The Ratsnest view is activated by default, showing all input and output nets for the selected macro.

To display the Ratsnest view:

1. From the **Nets** menu, choose **Display**, and then choose **Input**, **Output**, or **Both**, depending on which type of nets you want to display.
2. From the **Nets** menu, choose **Display Algorithm**, and then choose **Ratsnest**, or click the Ratsnest button in the toolbar.
3. Select the assigned macro in the **ChipView** window or **Assigned** list box. ChipEditor displays all nets connected to the assigned macro. To see nets assigned to multiple macros, hold down the **CTRL** key while you click on each assigned macro.

Route View

The Route view displays a representation of the routes for assigned macros. This feature shows the general location of routing segments used by the design.

To display the route view:

1. Complete **Layout**. To display routes, Layout must be completed before running ChipEditor.
2. From the **Nets** menu, choose **Display**, and then choose **Input**, **Output**, or **Both** to tell ChipEditor which routes to display.
3. From the **Nets** menu, choose **Display Algorithm**, and then choose **Routes** tell ChipEditor that you want to display routes.
4. Select the macro in the **ChipView** window or **Assigned** list box, or select multiple macros by holding down the **CTRL** key as you select the macros you want to see. The routes for the selected macros appear in the ChipView window.

Note: If a macro is moved or unassigned, you must use the Ratsnest view to display the nets connected to it.

Clusters and SuperClusters

A cluster is a group of logic elements. The type of elements that make up the cluster is determined by the device type.

A SuperCluster is at least two clusters (SX). Modules in a cluster can be connected by fast or direct connects.

Use these areas as guides to ensure that the nets are fast/direct connect for implementation. Nets that connect within a rectangle can be implemented as fast or direct connects, depending on availability. For details about fast connects and direct connects, please see the FPGA datasheet for your device on the Actel web site.

Note: This feature is only available for the SX, SX-A, and eX families.

To view clusters or SuperClusters, from the **View** menu, choose **Static Objects**, and then choose **Cluster** or **SuperCluster**. The cluster areas appear in the ChipView window.

Locating a Net by Name

To locate a net by name:

1. From the **Nets** menu, choose **Select Net**.
2. In the **Select Net** dialog box, type the name of the net to find, and click **Find**. The found net appears highlighted in the **ChipView** window.

Using ChipEditor with Silicon Explorer

Use ChipEditor to select probes for Silicon Explorer. To use ChipEditor with Silicon Explorer, you must have installed and be familiar with Silicon Explorer.

To select probes using ChipEditor:

1. Open Silicon Explorer.
2. Load the probe file of the current design.
3. Start ChipEditor.
4. **Synchronize data**. Click the **R** (Re-sync) button in ChipEditor's toolbar. When completed, the A and B buttons in the toolbar are activated.
5. Select a module in ChipEditor.
6. Click the **A** button in ChipEditor's toolbar to assign the selected module's output to probe A in Silicon Explorer.
7. Select another module in ChipEditor.
8. Click the **B** button in ChipEditor's toolbar to assign the selected module's output to probe B in Silicon Explorer.
9. From Silicon Explorer, click the **Acquire** toolbar button. Waveforms are displayed in Silicon Explorer.

Using ChipEditor with Timer

Use ChipEditor and Timer together to view the place-and-route of paths in ChipEditor.

To view paths:

1. Open **Timer** and **ChipEditor** from Designer.
2. In **Timer**, click the **Paths** tab.
3. Select a **Path** set in the path set grid. Paths within that set are displayed in the path grid.
4. Select the path you wish to expand in the lower path grid.
5. Expand the path by double-clicking on the path, or from the **Edit** menu, choose **Expand Path**. The Expanded Paths window opens and displays a path in the Expanded Paths Grid and a graphical representation of the path in the Chart Window. The Expanded Paths grid shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay, and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge.
6. Anything selected in the Expanded Paths grid or Graph window is reflected in both windows. Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
    - Selecting an instance, net, or macro in the Expanded Paths grid highlights that selection in the Chart window.
    - Selecting a logic macro in the Chart window highlights all instances of the macro in the Expanded Paths grid.
    - Toggle the **Graph window** on and off by choosing **Graph Window** from the **Window** menu. Use the commands on the **View** menu to zoom in and out. In the Graph window, dragging the mouse downward and to the left will make the selection fit within the window. Dragging down and to the right drags out a zoom in area.
    - In some cases, long instance names may overlap and be difficult to read in the Graph window. To resolve this, move the module. Select the module and while holding down the **SHIFT** key, click and drag the module to another location.
7. Select a module or net in the Expanded Paths dialog box. The module or net is shown in ChipEditor.

Note: You can add and remove break points in Timer while using the ChipEditor tool.

See the *Timer User's Guide* for more information.

Menus, Toolbar Buttons, and Shortcut Keys

The PC and workstation (UNIX) versions of ChipEditor have the same menus. However, some dialog boxes may look slightly different due to the different windowing environments. The functionality is the same, though the locations of the fields and buttons on the dialog boxes may vary. Field names may also vary between platforms.

File menu

Command	Icon	Shortcut	Function
Commit			Saves your changes to the working design for this Designer session only **Note: To save changes to disk, you must also save your file in Designer**.
Print		CTRL + P	Prints the design displayed in the ChipView window
Close			Closes ChipEditor

Edit menu

Command	Icon	Shortcut	Function
Assign		CTRL + L	Assigns the selected macro to the next selected module location
Unassign		DEL key	Unassigns the selected macro
Lock		CTRL + F	Locks the selected macro in the designated location
Unlock			Unlocks the selected macro
Select All		CTRL + A	Selects all macros in your design
Select All Assigned			Selects all assigned macros in your design
Select All Unassigned			Selects all unassigned macros in your design
Configure I/O Banks			Not used

View menu

Command	Icon	Shortcut	Function
Zoom Area			Drag out an area to enlarge
Zoom In		+	Magnifies the view by a factor of 2 (scale = 2x)
Zoom Out		-	Reduces the view by a factor of 2 (scale = .5x)
Fit in Window		CTRL + W	Fits the entire design within the ChipView window
Redraw		F2	Redraws the design in the ChipView window
Mark		CTRL + G	Sets a pointer to the current cursor location, which you can return to by choosing **Go to Mark**
Go to Mark		CTRL + H	Moves the cursor to your last marked location
Configure List Boxes...			Displays the Configure List Boxes dialog box, in which you can filter which macros appear in the Assigned and Unassigned list boxes
Color Manager			Displays the Color Manager dialog box, in which you set the default highlight colors for nets, clusters, and super clusters in the ChipView window
Static Objects > Cluster			Highlights clusters in their default highlight color
Static Objects > Super Cluster			Highlights SuperClusters in their default highlight color
I/O Banks			Not used
Toolbar			Hides or displays the toolbar buttons
Assigned List Box			Hides or displays the Assigned List Box
Unassigned List Box			Hides or displays the Unassigned List Box
World View			Hides or displays the World View window
Status bar			Hides or displays the status bar

Nets menu

Command	Icon	Shortcut	Function
Display			Use options in the submenu with the Ratsnest or Minimum Spanning Tree modes: • None - Hides all nets
		CTRL + I	• Input - Displays all input nets for the selected macro • Output - Displays all output nets for the selected macro
			• Both - Displays all input and output nets for the selected macro
		CTRL + B	
			• Selection Only - Limits the Ratsnest to show nets between selected modules only
Display Algorithm			Use options in this submenu with the Display options Input, Output, or Both:
		CTRL + T	• Ratsnest: Displays net connectivity between assigned macros by connecting lines from the output pins to all input pins
		CTRL + M	• Miniumum Spanning Tree: Activates minimum spanning-tree view mode
			• Routes: Displays a representation of the routes
Select Net		CTRL + N	Locates a net by name
Show Net Details		CTRL + D	Displays detailed information about a net

Help menu

Command	Shortcut	Function
Help Topics		Displays online Help for this version of ChipEditor
Reference Manual		Opens the ChipEditor User's Guide (.pdf file) in Adobe Acrobat
Extended Error Message		Displays a dialog box with more detailed information

Contacting Actel

Actel Headquarters

Actel Corporation is a supplier of innovative programmable logic solutions, including field-programmable gate arrays (FPGAs) based on Antifuse and Flash technologies, high-performance intellectual property (IP) cores, software development tools, and design services targeted for the high-speed communications, application-specific integrated circuit (ASIC) replacement, and radiation-tolerant markets.

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Technical Support

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M. Pacific Time, Monday through Friday.

Visit Tech Support Online

For 24-hour support resources, visit Actel Technical Support at http://www.actel.com/custsup/search.html.

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Contact us with your technical questions via e-mail or by phone. When sending your request to us, please be sure to include your full name, company name, email address and telephone number.

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