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Information Technology - AT Attachment Interface with Extensions (ATA-2)

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ABSTRACT

This standard defines an integrated interface between devices and host processors. It provides a common point of attachment for systems manufacturers, system integrators, and suppliers of intelligent devices.

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American National Standard
for Information Technology -

AT Attachment Interface with Extensions (ATA-2)

Secretariat
Information Technology Industry Council

Approved Month dd, yy

American National Standards Institute, Inc.

Abstract

This standard defines an integrated interface between devices and host processors. It provides a common point of attachment for systems manufacturers, system integrators, and suppliers of intelligent devices.

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Foreword (This foreword is not part of American National Standard X3.279 -1996.)

When the first IBM PC(TM) (Personal Computer) was introduced, there was no hard disk storage capability. Successive generations of products resulted in the inclusion of a hard disk as the primary storage device. When the PC AT(TM) was developed, a hard disk was the key to system performance, and the controller interface became a de facto industry interface for the inclusion of hard disks in PC ATs.

The price of desktop systems has declined rapidly because of the degree of integration which reduced the number of components and interconnects. A natural outgrowth of this integration was the inclusion of controller functionality into the hard disk.

In October 1988 a number of device suppliers formed the Common Access Method Committee to encourage an industry-wide effort to adopt a common software interface to dispatch input/output requests to SCSI devices. Although this was the primary objective, a secondary goal was to specify what was known as the AT Attachment interface. The resulting AT Attachment Interface For Disk Drives standard fulfilled that requirement.

As personal computer type systems continued to evolve, there was a need to extend the capabilities of the interface. The lap-top and small computer systems needed to modify the mechanical aspects of the interface. High performance systems needed to have enhanced transfer rates. In addition, there were a number of issues in the AT Attachment standard that needed to be addressed.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the X3 Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

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Introduction

This standard is divided into the following clauses and annexes.

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 lists the normative references.

Clause 3 provides definitions, abbreviations, and conventions used within this document.

Clause 4 contains the electrical and mechanical characteristics; covering the interface cabling requirements of the DC, data cables and connectors.

Clause 5 contains the signal descriptions of the AT Attachment Interface.

Clause 6 contains descriptions of the registers of the AT Attachment Interface.

Clause 7 describes the general operating requirements of the AT Attachment Interface.

Clause 8 contains descriptions of the commands of the AT Attachment Interface.

Clause 9 contains an overview of the protocol of the AT Attachment Interface.

Clause 10 contains the interface timing diagrams.

Annexes A through E are informative.

American National Standard
for Information Systems -

Information Technology -
AT Attachment Interface with Extensions (ATA-2)

1. Scope

This standard extends the AT Attachment Interface with the addition of new commands, and defines improved interface transfer rates. In addition, general improvements have been made in content for completeness and to improve clarity.

This standard defines the AT Attachment Interface and integrated interfaces between devices and host processors. It provides a common point of attachment for systems manufacturers, system integrators, and suppliers of intelligent devices.

The application environment for the AT Attachment Interface is any device which uses internal storage.

The PC AT Bus(TM) is a widely used and implemented interface for which a variety of devices have been manufactured. As a means of reducing size and cost, a class of products has emerged which embed the controller functionality in the device. Because of their compatibility with existing AT hardware and software this interface quickly became a de facto industry standard. While the AT Attachment Interface has its roots in the PC AT Bus(TM), its use has extended to many other systems.

2. Normative references

None.

3. Definitions, abbreviations, and conventions

3.1 Definitions and Abbreviations

For the purposes of this American National Standard, the following definitions apply.

3.1.1 ATA (AT attachment): ATA defines the physical, electrical, transport, and command protocols for the internal attachment of block storage devices.

3.1.2 ATA-1 device: A device which complies with ANSI X3.221-1994, the AT Attachement Interface for Disk Drives.

3.1.3 AWG: American Wire Gauge.

3.1.4 Command acceptance: A command is considered accepted whenever the host writes to the Command Register and the device currently selected has its BSY bit equal to zero. An exception exists for the EXECUTE DIAGNOSTIC command (see the description of the EXECUTE DIAGNOSTIC command).

3.1.5 CHS (Cylinder-head-sector): This term defines the addressing of the device as being by cylinder number, head number and sector number.

3.1.6 Data block: This term describes a unit of data words transferred using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of a READ MULTIPLE, WRITE MULTIPLE, READ LONG and WRITE LONG commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command. In the cases of READ LONG and WRITE LONG, the size of the data block is a sector plus a vendor specific number of bytes. The default length of the vendor specific bytes associate with the READ LONG and WRITE LONG commands is four bytes, but may be changed by use of the SET FEATURES command.

3.1.7 Device: Device is a storage peripheral. Traditionally, a device on the ATA interface has been a hard disk drive, but any form of storage device may be placed on the ATA interface provided it adheres to this standard.

3.1.8 Device selection: A device is selected when the DEV bit of the Drive/Head register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.

3.1.9 DMA (Direct memory access): A means of data transfer between device and host memory without processor intervention.

3.1.10 LBA (Logical block address): This term defines the addressing of the device as being by the linear mapping of sectors.

3.1.11 Master: Previous to this standard, Device 0 has also been referred to as the master. Throughout this document the term Device 0 shall be used.

3.1.12 Optional: This term describes features which are not required by the standard. However, if any optional feature defined by the standard is implemented, it shall be done in the way defined by the standard. Describing a feature as optional in the text is done to assist the reader.

3.1.13 PIO (Programmed input/output): A means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

3.1.14 Reserved: Reserved bits, bytes, words, fields and code values are set aside for future standardization. Their use and interpretation may be specified by future xtensions to this or other standards. A reserved bit, byte, word or field all e set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words or fields. Receipt of reserved code values in defined fields shall be treated as an error.

3.1.15 Sector: A uniquely addressable set of 256 words (512 bytes).

3.1.16 Slave: Previous to this standard, Device 1 has also been referred to as the slave. Throughout this document the term Device 1 shall be used.

3.1.17 Unrecoverable error: An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one and the BSY bit to zero in the Status register when processing a command.

3.1.18 VS (Vendor specific): This term is used to describe bits, bytes, fields and code values which are reserved for vendor specific purposes. These bits, bytes, fields and code values are not described in this

standard, and may be used in a way that varies between vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

3.2 Conventions

If there is a conflict between text and tables, the table shall be accepted as being correct.

3.2.1 Keywords

Lower case is used for words having the normal English meaning. Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.2.4 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

3.2.2 Numbering

Numbers that are not immediately followed by a lower-case "b" or "h" are decimal values. Numbers that are immediately followed by a lower-case "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lower-case "h" (e.g., 3Ah) are hexadecimal values.

3.2.3 Signal conventions

Signal names are shown in all upper case letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates it is a low active signal. A low active signal is true when it is below ViL, and is false when it is above ViH. No dash at the end of a signal name indicates it is a high active signal. A high active signal is true when it is above ViH, and is false when it is below ViL.

Asserted means that the signal is driven by an active circuit to its true state.

Negated means that the signal is driven by an active circuit to its false state.

Released means that the signal is not actively driven to any state. Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal. These cases are noted under the description of the signal, and their released state is stated.

Control signals that may be used for two mutually exclusive functions are identified with their two names separated by a colon e.g.; SPSYNC:CSEL can be used for either the Spindle Sync (SPSYNC) or the Cable Select (CSEL) functions.

3.2.4 Bit conventions

Bit names are shown in all upper case letters except where a lower case n precedes a bit name. If there is no preceding n, then when BIT is equal to one the meaning of the bit is true, and when BIT is equal to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is equal to zero the meaning of the bit is true and when nBIT is equal to one the meaning of the bit is false.

3.2.5 Byte ordering for 8-bit and 16-bit data transfers

Assuming a block of data contains "n" bytes of information, and the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the field, and Byte(n-1) is the last byte of the block.

When such a block of data is transferred on the ATA interface in 16 bit wide transfer mode, then the bytes shall be presented in the following order:

	DD DD DD DD DD DD DD DD 15 14 13 12 11 10 09 08	DD DD DD DD DD DD DD DD 07 06 05 04 03 02 01 00
First transfer	--------Byte(1)--------	--------Byte(0)--------
Second transfer	--------Byte(3)--------	--------Byte(2)--------
.....		
Last transfer	-------Byte(n-1)-------	-------Byte(n-2)-------

When such a block of data is transferred on the ATA interface in 8 bit wide transfer mode, then the bytes shall be presented in the following order:

	DD DD DD DD DD DD DD DD 07 06 05 04 03 02 01 00
First transfer	--------Byte(0)--------
Second transfer	--------Byte(1)--------
.....	
Next to last transfer	-------Byte(n-2)-------
Last transfer	-------Byte(n-1)-------

NOTE 1 - The above description is for data on the ATA Interface. Host systems and/or host adapters may cause the order of data, as seen in the memory of the host, to be different.

4. Interface physical and electrical requirements

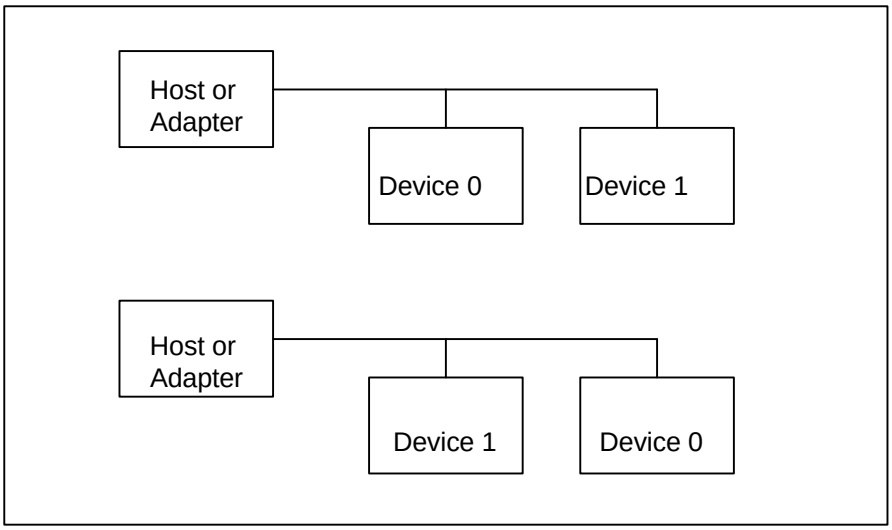
The traditional 40-pin ATA interface is documented in this clause as one of the connection schemes being utilized. Annex B and annex C provide a basic definition of two alternative connection schemes.

4.1 Configuration

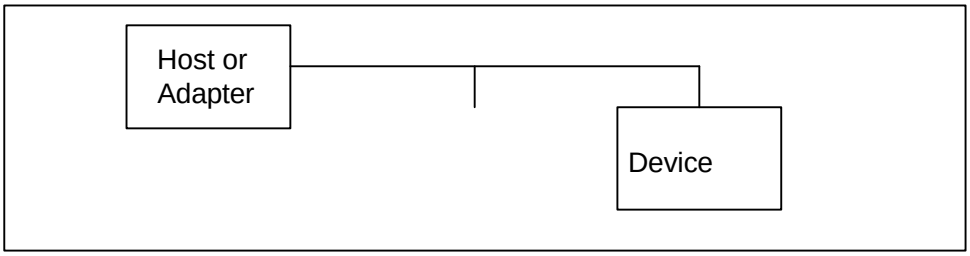
This standard defines the ATA interface containing a single host or host adapter and one or two devices. If two devices are connected to the interface, they are connected in a daisy chained configuration. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways:

- a switch or a jumper on the device
- use of the Cable Select (CSEL) pin



In a two drive configuration, the order of placement of Device 0 and Device 1 on the ATA interface cable is not significant to the operation of the interface.



If only a single device is attached via the ATA interface to a host, it is recommended that the host and the device be placed at the two ends of the cable.

Figure 1 - ATA interface cabling diagram

Also see 5.2.15.2 on CSEL operation.

4.2 DC cable and connector

The device receives DC power through a 4-pin connector.

4.2.1 4-pin power

The pin assignments are shown in table 1. Recommended part numbers for the mating connector to 18 AWG cable are shown below, but compatible parts may be used.

Connector (4 pin)	AMP 1-480424-0 or compatible.
Contacts (loose piece)	AMP 60619-4 or compatible.
Contacts (strip)	AMP 61117-4 or compatible.

Table 1 - DC interface using 4 pin power connector

Power line designation	Pin Number
+12 Volts	1
+12 Volt Return	2
+5 Volt Return	3
+5 Volts	4

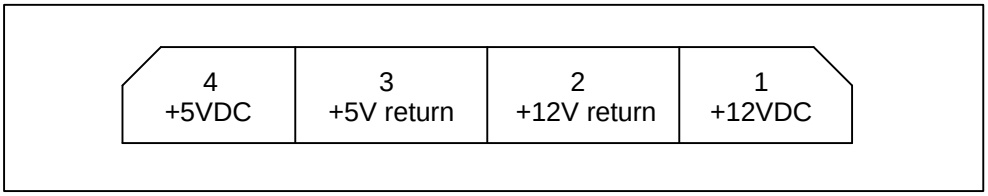


Figure 2 - Drive side connector pin numbering

4.3 I/O connector

The I/O connector is a 40-pin connector as shown in figure 3, with pin assignments as shown in **table 5.** The connector should be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20. The corresponding pin on the cable connector should be plugged.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 should remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in figure 3, conductor 1 on pin 1 of the plug has to be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

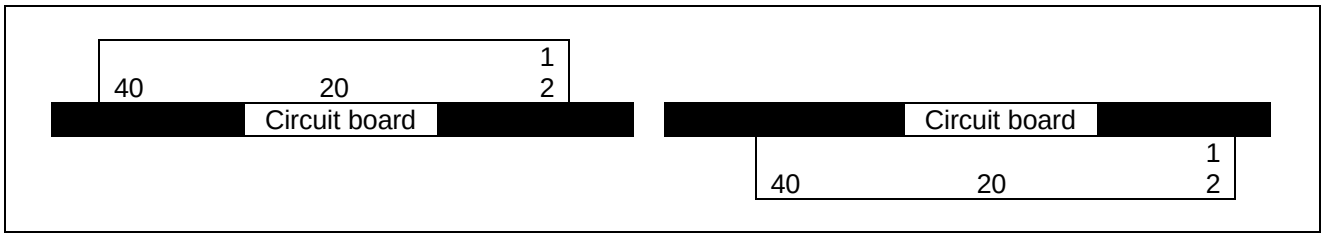


Figure 3 - 40-pin connector mounting

Recommended part numbers for the mating connector are shown below, but equivalent parts may be used.

Connector (40 pin)	3M 3417-7000 or equivalent.
Strain relief	3M 3448-2040 or equivalent.

4.4 I/O cable

The cable specifications affect system integrity and the maximum length that can be supported in any application.

Flat cable (stranded 28 AWG)	3M 3365-40 or equivalent.
Flat cable (stranded 28 AWG)	3M 3517-40 (shielded) or equivalent.

Cable total length shall not exceed 0,46m (18 inches).

Cable capacitance shall not exceed 35 pf.

4.5 Electrical characteristics

Interface signals are defined in tables 2 and 3.

Table 2 - DC characteristics

	Description	Min	Max
I_{OL}	Driver sink current	12 mA	
I_{OH}	Driver source current	400 uA	
V_{IH}	Voltage Input High	2,0 V d.c.	
V_{IL}	Voltage Input Low		0,8 V d.c.
V_{OH}	Voltage Output High (I_{OH} = -400 uA)	2,4 Vd.c.	
V_{OL}	Voltage Output Low (I_{OL} = 12ma)		0,5 V d.c.

Table 3 - AC characteristics

	Description	Min	Max
tRISE	Rise time for any signal on AT interface(1)	5 ns	
tFALL	Fall time for any signal on AT interface(1)	5 ns	
Cin	Input Capacitance(each host or Device)		25 pf
Cout	Output Capacitance(each host or Device)		25 pf
(1) tRISE and tFALL are measured from 10-90% of full signal amplitude with a total capacitive load of 100 pf.			

NOTE 2 - I_{OH} value at 400 uA is insufficient in the case of DMARQ which is typically pulled low by a 5.6k ohm resistor.

4.5.1 ATA-2 driver types and required pull-ups

Table 4 - ATA-2 driver types and required pull-ups

Signal	Source	Driver Type (See note 1)	Pull-up at host (See note 2)	Pull-up at each device (See note 2)	Notes
Reset	Host	TP			
DD 0:15	Bidir.	TS			
DMARQ	Device	TS	5,6K PD		(3)
DIOR- DIOW-	Host	TS			
IORDY	Device	TS	1,0K		(4)
SPSYNC/CSEL					(5)
CSEL	Host		Ground	10K	(6)
SPSYNC	Device	TS/OC		VS	(7)
DMACK-	Host	TP			
INTRQ	Device	TS			
IOCS16-	Device	OC	1,0K		
DA0:2	Host	TP			
PDIAG-	Device	TS		10K	
CS0- CS1-	Host	TP			
DASP-	Device	OC		10K	(5)

NOTES
1 - TS=Tri-State; OC=Open Collector; TP=Totem-Pole; PU=Pull-up; PD=Pull-down; VS=Vendor specific
2 - All resistor values are minimum (lowest) allowed.
3 - ATA-2 defines this line to be tri-stated whenever the device is not selected or is not executing a DMA data transfer. When enabled by DMA transfer, it shall be driven high and low by the device.
4 - This signal should only be enabled during DIOR/DIOW cycles to the selected device.
5 - See signal descriptions for information on dual use of this signal.
6 - When used as CSEL, Line is grounded at Host and 10K Pull-up is required at both devices.
7 - When used as SPSYNC, application is vendor specific.

5. Interface signal assignments and descriptions

5.1 Signal summary

The physical interface consists of receivers and drivers communicating through a 40-conductor flat ribbon non-shielded cable using an asynchronous interface protocol. The pin numbers and signal names are shown in table 5. Reserved signals shall be left unconnected. Table 6 contains an alphabetical listing by pin acronym.

Table 5 - Interface signal names and pin assignments

Description	Source	Pin	Acronym
Reset	Host	1	RESET-
	n/a	2	Ground
Data bus bit 7	Host/Device	3	DD7
Data bus bit 8	Host/Device	4	DD8
Data bus bit 6	Host/Device	5	DD6
Data bus bit 9	Host/Device	6	DD9
Data bus bit 5	Host/Device	7	DD5
Data bus bit 10	Host/Device	8	DD10
Data bus bit 4	Host/Device	9	DD4
Data bus bit 11	Host/Device	10	DD11
Data bus bit 3	Host/Device	11	DD3
Data bus bit 12	Host/Device	12	DD12
Data bus bit 2	Host/Device	13	DD2
Data bus bit 13	Host/Device	14	DD13
Data bus bit 1	Host/Device	15	DD1
Data bus bit 14	Host/Device	16	DD14
Data bus bit 0	Host/Device	17	DD0
Data bus bit 15	Host/Device	18	DD15
Ground	n/a	19	Ground
(keypin)	n/a	20	Reserved
DMA Request	Device	21	DMARQ
Ground	n/a	22	Ground
I/O Write	Host	23	DIOW-
Ground	n/a	24	Ground
I/O Read	Host	25	DIOR-
Ground	n/a	26	Ground
I/O Ready	Device	27	IORDY
Spindle Sync or Cable Select	(See note 1)	28	SPSYNC:CSEL
DMA Acknowledge	Host	29	DMACK-
Ground	n/a	30	Ground
Interrupt Request	Device	31	INTRQ
16 Bit I/O	Device	32	IOCS16-
Device Address Bit 1	Host	33	DA1
PASSED DIAGNOSTICS	(See note 1)	34	PDIAG-
Device Address Bit 0	Host	35	DAO
Device Address Bit 2	Host	36	DA2
Chip Select 0	Host	37	CS0-
Chip Select 1	Host	38	CS1-
Device Active or Slave (Device 1) Present	(See note 1)	39	DASP-
Ground	n/a	40	Ground
Note 1 - See signal descriptions for information on source of these signals.			

Table 6 - Interface signals - Alphabetical listing

Signal	Pin	Signal	Pin
CS0-	37	DD12	12
CS1-	38	DD13	14
DA0	35	DD14	16
DA1	33	DD15	18
DA2	36	DIOR-	25
DASP-	39	DIOW-	23
DD0	17	DMACK-	29
DD1	15	DMARQ	21
DD2	13	INTRQ	31
DD3	11	IOCS16-	32
DD4	9	IORDY	27
DD5	7	PDIAG-	34
DD6	5	RESET-	1
DD7	3	SPSYNC:	28
DD8	4	CSEL	28
DD9	6	keypin	20
DD10	8	ground	2,19,22,24,26,30,40
DD11	10		

5.2 Signal descriptions

5.2.1 CS0- (CHIP SELECT 0)

This is the chip select signal from the host used to select the Command Block Registers. See table 7.

NOTE 3 - This signal has also been known in the industry as CS1FX-.

5.2.2 CS1- (CHIP SELECT 1)

This is the chip select signal from the host used to select the Control Block Registers. See table 7.

NOTE 4 - This signal has also been known in the industry as CS3FX-.

5.2.3 DA2, DA1, and DA0 (DEVICE ADDRESS)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device. See table 7.

5.2.4 DASP- (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10K ohm pull-up resistor.

During power on initialization or after RESET- is negated, DASP- shall be deasserted by both Device 0 and Device 1 within 1 ms, and then Device 1 shall assert DASP- within 400 ms, to indicate that Device 1 is present.

Device 0 shall allow up to 450 ms for Device 1 to assert DASP-.

DASP- shall be negated following acceptance of a command by Device 1 or after 31 s, whichever comes first.

Any time after negation of DASP-, either device may assert DASP- to indicate that a device is active.

If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain Voh and Vol compatibility, given the Ioh and Iol requirements of the DASP- device drivers.

5.2.5 DD0-DD15 (Device Data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit transfers e.g., registers, vendor specific bytes associated with the READ LONG and WRITE LONG commands and, if the device supports the Features register capability to enable 8-bit-only data transfers (see 8.24, Set features).

5.2.6 DIOR- (Device I/O read)

This is the read strobe signal from the host. The falling edge of DIOR- enables data from a register or data port of the device onto the signals, DD0-DD7 or DD0-DD15. The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

5.2.7 DIOW- (Device I/O write)

This is the Write strobe signal from the host. The rising edge of DIOW- latches data from the signals, DD0-DD7 or DD0-DD15, into a register or the data port of the device. The device shall not act on the data until it is latched.

5.2.8 DMACK- (DMA acknowledge) (optional)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

NOTE 5 - This signal may be negated by the Host to suspend the DMA transfer in process. For Multi-Word DMA transfers, the Device may negate DMARQ within the tL specified time (refer to figure 12) once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK-.

5.2.9 DMARQ (DMA request) (optional)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e.; the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, IOCS16-, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

NOTE 6 - In ATA-1 devices, this signal was either totem-pole or tri-state in different implementations. In EISA systems, 5.6K pull-down is used to cause a logic low on undriven lines. ATA-2 defines this line to be in high-impedance mode except when DMA transfer is active from the selected device.

In systems which may use mixed devices where totem-pole drivers are used, and the system shares this line with other non-ATA devices, the ATA host or ATA adapter shall ensure that appropriate protection is employed to protect ATA device DMARQ drivers from damage.

5.2.10 INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

The interrupt pending condition shall be cleared by:

- assertion of RESET-; or
- the setting of the SRST bit of the Device Control register; or
- the host writing the Command register; or
- the host reading the Status register.

On PIO transfers, INTRQ is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the SET MULTIPLE MODE command. An exception occurs on FORMAT TRACK, WRITE SECTOR(S), WRITE BUFFER and WRITE LONG commands - INTRQ shall not be asserted at the beginning of the first data block to be transferred.

On DMA transfers, INTRQ is asserted only once, after the command has completed.

If the system shares this line with non-ATA devices, the ATA host or ATA adapter shall ensure that appropriate protection is employed to protect ATA device INTRQ drivers from damage.

5.2.11 IOCS16- (Device 16-bit I/O)

During PIO transfer modes 0, 1 or 2, IOCS16- indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word. This shall be an open collector output.

– When transferring in any PIO mode and accessing any register except the data port, transfers shall be 8-bit using DD0-7;
– When transferring in PIO modes 0, 1 or 2, if IOCS16- is not asserted, transfers shall be 8-bit using DD0-7;
– When transferring in PIO modes 0, 1 or 2, if IOCS16- is asserted, transfers shall be 16-bit using DD0-15;
– When transferring in PIO modes 3 or 4, IOCS16- shall not be used by the host, and all transfers shall be 16-bit using DD0-15, except for bytes beyond the 512th byte for READ LONG and WRITE LONG commands which shall be 8-bit using DD0-7;
– When transferring in DMA mode, the host shall use a 16-bit DMA channel and IOCS16- shall not be asserted.

5.2.12 IORDY (I/O channel ready) (optional)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If actively asserted, this signal shall only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

The use of IORDY is required for PIO modes 3 and above.

5.2.13 PDIAG- (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10K ohm pull-up resistor shall be used on this signal by each device.

Following a power on reset, software reset or RESET-, Device 1 shall negate PDIAG- within 1 ms (to indicate to Device 0 that it is busy). Device 1 shall then assert PDIAG- within 30 seconds to indicate that it is no longer busy, and is able to provide status. If Device 1 is present, then Device 0 shall wait for up to 31 seconds from power-on reset, software reset or RESET- for Device 1 to assert PDIAG-. If Device 1 fails to assert PDIAG-, Device 0 shall set bit 7 to 1 in the Error register to indicate that Device 1 failed. After the assertion of PDIAG-, Device 1 may be unable to accept commands until it has finished its reset procedure and is Ready (the DRDY bit is equal to one).

Following the receipt of a valid EXECUTE DEVICE DIAGNOSTIC command, Device 1 shall negate PDIAG- within 1 ms to indicate to Device 0 that it is busy and has not yet passed its device diagnostics. Device 1 shall then assert PDIAG- within 5 seconds to indicate that it is no longer busy, and is able to provide status. Device 1 should clear the BSY bit before asserting PDIAG-. If Device 1 is present then Device 0 shall wait for up to 6 seconds from the receipt of a valid EXECUTE DEVICE DIAGNOSTIC command for Device 1 to assert PDIAG-. If Device 1 fails to assert PDIAG-, Device 0 shall set bit 7 to 1 in the Error register to indicate that Device 1 failed.

If DASP- was not asserted by Device 1 during reset initialization, Device 0 shall post its own status immediately after it completes diagnostics, and clear the Device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is Ready (the DRDY bit is equal to one).

It is recommended that the host make no connect to the PDIAG- signal.

5.2.14 RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 usec after voltage levels have stabilized within tolerance during power on and negated thereafter unless some event requires that the device(s) be reset following power on.

5.2.15 SPSYNC:CSEL (Spindle synchronization/cable select) (optional)

This signal shall have a 10K ohm pull-up resistor.

This is a dual purpose signal and neither, either or both functions may be implemented. If both functions are implemented then they cannot be active concurrently: the choice as to which is active is vendor specific.

All devices connected to the same cable should have the same function active at the same time. If SPSYNC and CSEL are mixed on the same cable, then device behavior is undefined.

Prior to the introduction of this standard, this signal was defined as DALE (Device Address Latch Enable), and used for an address valid indication from the host system. If used, the host address and chip selects, DAO through DA2, CS0-, and CS1- were valid at the negation of this signal and remained valid while DALE was negated, therefore, the device did not need to latch these signals with DALE.

5.2.16 SPSYNC (Spindle synchronization) (optional)

The definition of this signal is vendor specific.

5.2.17 CSEL (Cable select) (optional)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL:

- If CSEL is negated then the device address is 0
- If CSEL is asserted then the device address is 1

CSEL shall be maintained at a steady level for at least 31 seconds after the negation of RESET-.

NOTE 7 - Special cabling can be used by the system manufacturer to selectively ground CSEL e.g., CSEL of Device 0 is connected to the CSEL conductor in the cable, and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to CSEL because the conductor is removed, thus the device can recognize itself as Device 1.

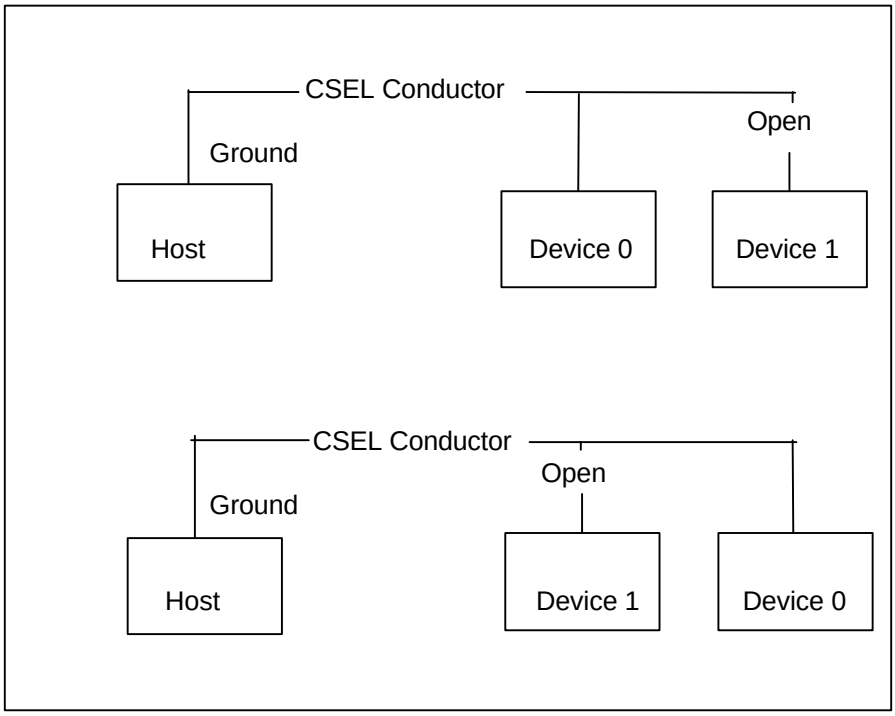


Figure 4 - Cable select example

6. Interface register definitions and descriptions

6.1 Device addressing considerations

In traditional controller operation, only the selected controller receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers). The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel (16 bits) either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisy chained on the interface, commands are written in parallel to both devices, and for all except the Execute Diagnostics command, only the selected device executes the command. On an Execute Diagnostics command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register (see 6.2.7). When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1. When a single device is attached to the interface it shall be set as Device 0.

6.2 I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Table 7 lists these registers and the addresses that select them.

Table 7 - I/O Port functions and selection addresses

Addresses					Functions	
CS0-	**CS1-**	**DA2**	**DA1**	**DA0**	**READ (DIOR-)**	**WRITE (DIOW-)**
N	N	x	x	x	Data bus high imped	Not Used
					Control block registers	
N	A	0	x	x	Data bus high imped	Not Used
N	A	1	0	x	Data bus high imped	Not Used
N	A	1	1	0	Alternate status	Device control
N	A	1	1	1	(Note 1)	Not Used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	* LBA bits 0- 7	* LBA bits 0- 7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	* LBA bits 8-15	* LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	* LBA bits 16-23	* LBA bits 16-23
A	N	1	1	0	Device/Head	Device/Head
A	N	1	1	0	* LBA bits 24-27	* LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address
* Mapping of registers in LBA mode						
Logic conventions are: A = signal asserted, N = signal negated, x = don't care						
Note 1 - This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall be sure not to drive the DD7 signal to prevent possible conflict with floppy disk implementations.						

6.2.1 Alternate status register

This register contains the same information as the Status register in the command block. The only difference being that reading this register does not imply interrupt acknowledge or clear a pending interrupt.

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

See 6.2.12 for definitions of the bits in this register.

6.2.2 Command register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in table 10.

6.2.3 Cylinder high register

In CHS Mode, this register contains the high order bits of the starting cylinder address for any media access. In LBA Mode, this register contains Bits 23-16 of the LBA for any media access.

This register shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

NOTE 8 - Prior to the development of this standard, this register was updated at the end of every media access command to reflect the current media address.

6.2.4 Cylinder low register

In CHS Mode, this register contains the low order bits of the starting cylinder address for any media access. In LBA Mode, this register contains Bits 15-8 of the LBA for any media access.

This register shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

NOTE 9 - Prior to the development of this standard, this register was updated at the end of every media access command to reflect the current media address.

6.2.5 Data register

The data register is either 8-bits or 16-bits depending on the interface width currently selected and/or the type of data being transferred by the current command.

6.2.6 Device control register

The bits in this register are as follows:

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved;
- SRST is the host software reset bit. The device is held reset when this bit is set. If two devices are daisy chained on the interface, this bit resets both simultaneously;
- nIEN is the enable bit for the device interrupt to the host. When the nIEN bit is equal to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is equal to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.

6.2.7 Device/Head register

This register contains device addressing and sector addressing information.

7	6	5	4	3	2	1	0
r	L	r	DEV	HS3	HS2	HS1	HS0

- Bit 7 is reserved;
- L is the sector address mode select. When the L bit is equal to zero, addressing is by CHS mode. When the L bit is equal to one, addressing is by LBA mode;
- Bit 5 is reserved;
- DEV is the device address. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected;
- If the L bit is equal to zero (CHS Mode), the HS3 through HS0 bits contain the head address of the CHS address. The HS3 bit is the most significant bit. If the L bit is equal to one (LBA Mode), the HS3 through HS0 bits contain bits 27 through 24 of the LBA. This field shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

  NOTE 10 - Prior to the development of this standard, the head field (the HS3 through HS0 bits) of this register was updated at the end of every media access command to reflect the current media address.

6.2.8 Error register

This register contains status from the last command executed by the device or a Diagnostic Code.

At the completion of any command except EXECUTE DEVICE DIAGNOSTIC, the contents of this register are valid when the ERR bit is equal to one in the Status register.

Following a power on, a reset, or completion of an EXECUTE DEVICE DIAGNOSTIC command, this register contains a diagnostic code (see table 11).

7	6	5	4	3	2	1	0
r	UNC	MC	IDNF	MCR	ABRT	TKNONF	AMNF

- Bit 7 is reserved;
- UNC (Uncorrectable Data Error) indicates an uncorrectable data error has been encountered;
- MC (Media Changed) is reserved for use by removable media devices and indicates that new media is available to the operating system. The MC bit shall be cleared by either a hardware reset or a power on reset.
- The first command following a media change shall be rejected with the MC bit set in the error register and the ERR bit set in the status register. The media changed state shall then be cleared and subsequent commands accepted normally;
- IDNF (ID Not Found) indicates the requested sector's ID field could not be found;
- ABRT (Aborted Command) indicates the requested command has been aborted because the command code is invalid or another device error has occurred;
- MCR (Media Change Requested) is reserved for use by removable media devices and indicates that a request for media removal has been detected by the device. When a request for media removal is detected, the MCR bit shall be returned in the error register and the ERR bit set in the status register for all subsequent DOOR LOCK commands. The MCR bit shall be cleared by a DOOR UNLOCK command, a MEDIA EJECT command or by a hard reset;
- TK0NF (Track 0 Not Found) indicates track 0 has not been found during a RECALIBRATE command;
- AMNF (Address Mark Not Found) indicates the data address mark has not been found after finding the correct ID field.

6.2.9 Features register

This register is command specific and may be used to enable and disable features of the interface e.g.; by the SET FEATURES Command to enable and disable caching.

This register may be ignored by some devices.

Some hosts, based on definitions prior to the completion of this standard, set values in this register to designate a recommended Write Precompensation Cylinder value.

6.2.10 Sector count register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in this register is zero, a count of 256 sectors is specified.

For media access commands, this register shall be zero at the completion of a command if there is no error indication in the Status register. For media access commands that complete with an error indication in the Status register, this register contains the number of sectors which need to be transferred in order to complete the request.

The contents of this register may be redefined on some commands, e.g.; INITIALIZE DEVICE PARAMETERS or WRITE SAME commands.

6.2.11 Sector number register

In CHS Mode, this register contains the starting sector number for any media access. In LBA Mode, this register contains Bits 7-0 of the LBA for any media access. This register is used by some non-media access commands to pass command specific information from the host to the device, or from the device to the host.

This register shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

NOTE 11 - Prior to the development of this standard, this register was updated at the end of every media access command to reflect the current media address.

6.2.12 Status register

This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device. When the BSY bit is equal to zero, the other bits in this register are valid and the other Command Block register may contain meaningful information. When the BSY bit is equal to one, no other bits in this register and all other Command Block registers are not valid.

NOTE 12 - Although host systems might be capable of generating read cycles shorter than the 400 ns specified for status update following the last command or data cycle, host implementations should wait at least 400 ns before reading the status register to insure that the BSY bit is valid.

For devices that implement the Power Management features, the contents of the Status register and all other Command Block registers are not valid while a device is in the Sleep mode.

If the host reads this register when an interrupt is pending, the interrupt is cleared.

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

- BSY (Busy) is set whenever the device has control of the command Block Registers. When the BSY bit is equal to one, a write to a command block register by the host shall be ignored by the device.

The device shall not change the state of the DRQ bit unless the BSY bit is equal to one. When the last block of a PIO data in command has been transferred by the host, then the DRQ bit is cleared without the BSY bit being set.

When the BSY bit equals zero, the device may only change the IDX, DRDY, DF, DSC and CORR bits in the Status register and the Data register. All of the other command block registers and bits within the Status register shall not be changed by the device.

NOTE 13 - The assertion of CORR by the device while the BSY bit is set to zero might not be recognized by BIOS and drivers which sample status as soon as the BSY bit is equal to zero.

The BSY bit shall be set by the device under the following circumstances:

a) within 400 ns after either the negation of RESET- or the setting of the SRST bit in the Device Control register;

b) within 400 ns after the acceptance of a command if the DRQ bit is not set;

c) between blocks of a data transfer during PIO data in commands if the DRQ bit is not set;

d) after the transfer of a data block during PIO data out commands if the DRQ bit is not set;

e) during the data transfer of DMA commands if the DRQ bit is not set.

The device shall not set the BSY bit at any other time.

When the BSY bit is set due to the negation of RESET- or the setting of the SRST bit, the BSY bit shall remain set until the device has completed processing of the reset condition.

When a command is accepted either the BSY bit shall be set, or if the BSY bit is cleared, the DRQ bit shall be set, until command completion.

NOTE 14 - There may be times when the BSY bit is set and then cleared so quickly, that the host may not be able to detect that the BSY bit had been set.

- DRDY (Device Ready) is set to indicate that the device is capable of accepting all command codes. This bit shall be cleared at power on. Devices that implement the power management features shall maintain the DRDY bit equal to one when they are in the Idle or Standby power modes. When the state of the DRDY bit changes, it shall not change again until after the host reads the Status register.

  When the DRDY bit is equal to zero, a device responds as follows:

  a) the device shall accept and attempt to execute the EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS commands;

  b) the device should reject all other commands codes by setting the ABRT bit in the Error register and setting the ERR bit in the Status register before clearing the BSY bit to signal the command completion. If a device accepts commands other than EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS during the time the DRDY bit is equal to zero, the results are vendor specific.

- DF (Device Fault) indicates a device fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific.
- DSC (Device Seek Complete) indicates that the device heads are settled over a track. When an error occurs, this bit shall not be changed until the Status Register is read by the host, at which time the bit again indicates the current Seek Complete status.
- DRQ (Data Request) indicates that the device is ready to transfer a word or byte of data between the host and the device.
- CORR (Corrected Data) is used to indicate a correctable data error. The definition of what constitutes a correctable error is vendor specific. This condition does not terminate a data transfer.
- IDX (Index) is vendor specific.
- ERR (Error) indicates that an error occurred during execution of the previous command. The bits in the Error register have additional information regarding the cause of the error. Once the device has set the error bit, the device shall not change the contents of the following items until a new command has been accepted, the SRST bit is set to one or RESET- is asserted:

  the ERR bit in the status register
  Error register
  Cylinder High register
  Cylinder Low register
  Sector Count register
  Sector Number register
  Device/Head register.

7. General operational requirements

7.1 Reset response

There are three types of reset in ATA. The following is a suggested method of classifying reset actions:

- Power On Reset: the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values.
- Hardware Reset: the device executes a series of electrical circuitry diagnostics, and resets to default values.
- Software Reset: the device resets the interface circuitry according to the Set Features requirement (See 8.24)

The power on reset, hardware reset, and software reset protocols are defined in 9.1 and 9.2.

7.2 Sector addressing

All addressing of data sectors recorded on the device's media is by a logical sector address. The mapping of logical sector addresses to the actual physical location of the data sector on the media is vendor specific.

An ATA device shall support at least one logical CHS translation mode known as the default translation mode. The device shall enter this translation mode following a reset. A device may support other logical translation modes and the host may use the INITIALIZE DEVICE PARAMETERS command to select the default CHS mode or any of the other supported CHS modes. The default translation mode is described in the Identify Device information. The current translation mode may also be described in the Identify Device information.

A CHS address is made up of three fields: the sector address, the head number and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation

mode but can not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65,535.

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

Sequential access to logical sectors shall be accomplished by treating the sector number as the least significant portion of the logical sector address, the head number as the middle portion of the logical sector address and the cylinder number as the most significant portion of the logical sector address.

A device may support LBA addressing. A device that supports LBA addressing indicates this in the Identify Device information. A host shall not attempt to use LBA addressing unless the device indicates the mode is supported.

A device shall not change the addressing method and shall return status information utilizing the addressing method specified for the command.

If a device supports LBA addressing mode, then the following shall be supported by the device:

a) The host may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the Device/Head register;

b) If LBA addressing is supported, then the device shall supported LBA addressing for all media access commands, except for the FORMAT TRACK command. Implementation of LBA addressing for the FORMAT TRACK command is vendor specific. The L bit of the Device/Head register shall be ignored for commands that do not access the media;

c) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector - 1
where heads_per_cylinder and sectors_per_track are the current translation mode values.

7.3 Power management feature set

The power management feature set permits a host to modify the behavior of a device in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes. A device that implements the power management feature shall implement the following minimum set of functions:

a) A standby timer;
b) Idle command;
c) Idle immediate command;
d) Sleep command;
e) Standby command;
f) Standby immediate command.

Additional vendor specific commands and functions are allowed.

7.3.1 Power modes

The lowest power consumption when the device is powered on occurs in Sleep Mode. When in Sleep Mode, the device requires a reset to be activated. The time to respond could be as long as 30 seconds.

In Standby Mode, the device interface is capable of accepting commands, but as the media may not be immediately accessible, it could take the device as long as 30 seconds to respond.

In Idle Mode, the device is capable of responding immediately to media access requests. A device in Idle Mode may take longer to complete the execution of a command because it may have to activate some circuitry.

In Active mode, the device is capable of responding immediately to media access requests, and commands complete execution in the shortest possible time. During the execution of a media access command a device shall be in Active mode.

7.3.2 Power management commands

The Check Power Mode command allows a host to determine if a device is currently in, going to or leaving Standby mode.

The Idle and Idle Immediate commands move a device to Idle mode immediately from the Active or Standby modes. The Idle command also sets the Standby Timer count and enables or disables the Standby Timer.

The Sleep command moves a device to Sleep mode. The device's interface becomes inactive at the completion of the Sleep command. A reset is required to move a device out of Sleep mode. When a device exits Sleep mode it may enter Active, Idle or Standby mode. The mode selected by the device is based on the type of reset received and on vendor specific implementation.

The Standby and Standby Immediate commands move a device to Standby mode immediately from the Active or Idle modes. The Standby command also sets the Standby Timer count and enables or disables the Standby Timer.

7.3.3 Standby timer

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby Timer is disabled, the device may not automatically enter Standby mode.

7.3.4 Idle mode transition

The transition to Idle mode is vendor specific, and may occur as a result of an IDLE or IDLE IMMEDIATE command, or in vendor specific way.

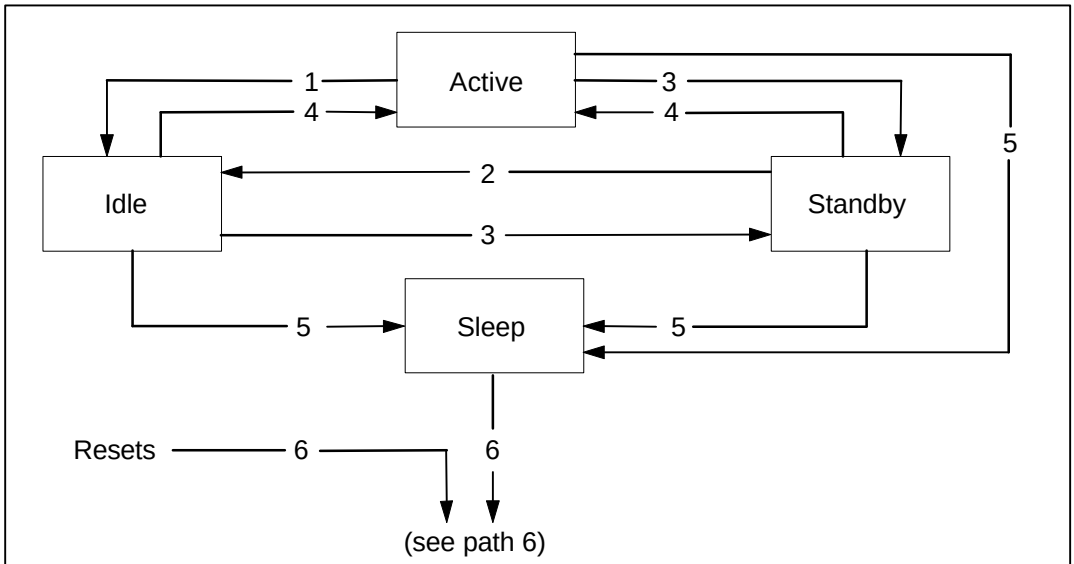
7.3.5 Status

In the Active, Idle, and Standby modes, the device shall have DRDY bit of the Status register set and, if BSY bit is not set, shall be ready to accept any command.

In Sleep mode, the device's interface is not active. A host shall not attempt to read the device's status or issue commands to the device.

7.3.6 Power mode transitions

Figure 5 shows the minimum set of mode transitions that shall be implemented.



Path 1: An IDLE command, IDLE IMMEDIATE command, or vendor specific implementation moves the device to Idle mode.
Path 2: An IDLE command or IDLE IMMEDIATE command moves the device to Idle mode.
Path 3: A STANDBY command, STANDBY IMMEDIATE command, or Standby timer expiration moves the device to Standby mode.
Path 4: A Media access command moves the device to Active mode.
Path 5: A SLEEP command moves the device to Sleep mode.
Path 6: A reset, either hardware or software, moves the device to Active, Idle or Standby as specified by the device vendor.

Figure 5 - Power management modes

7.3.7 Interface capability for power modes

The optional power commands permit the host to modify the behavior of the device in a manner which reduces the power required to operate. These modes also affect the physical interface as defined in the following table:

Table 8 - Power conditions

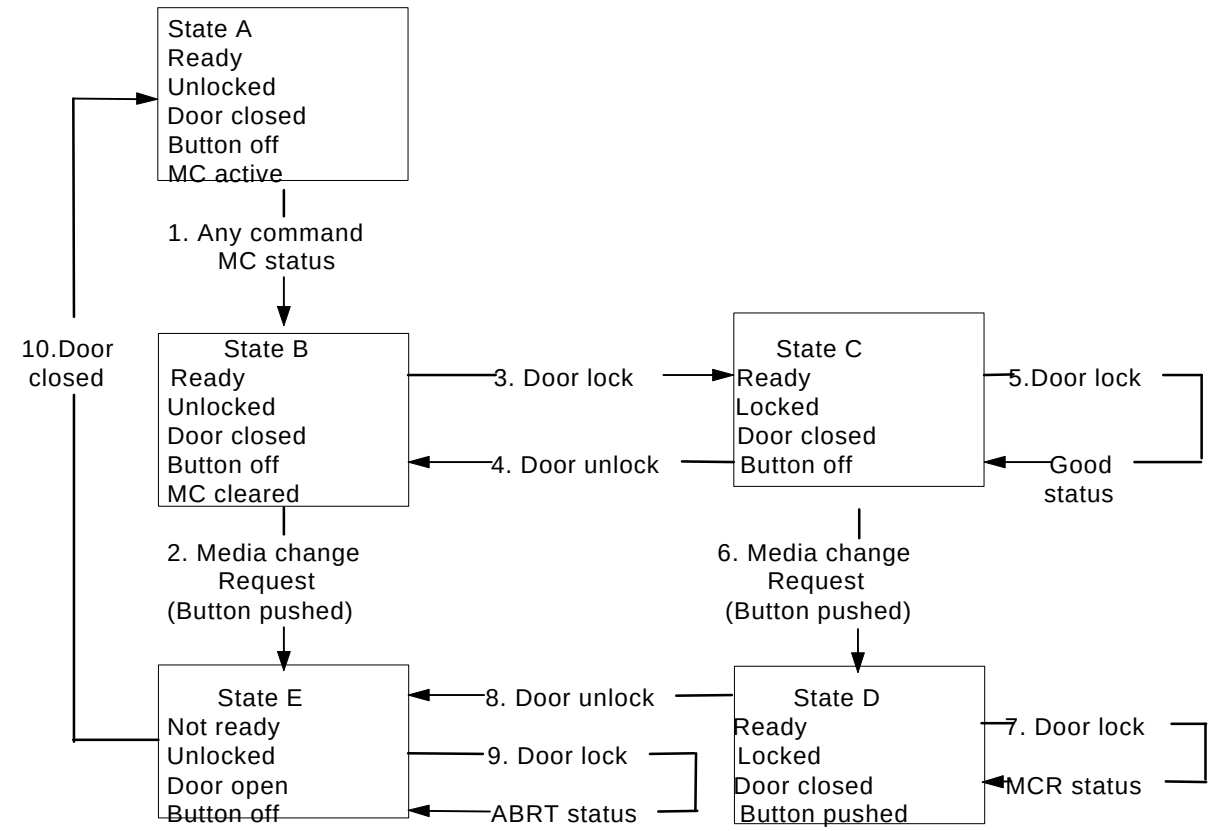
Mode	BSY	DRDY	Interface active	Media
Sleep	x	x	No	I
Standby	0	1	Yes	I
Idle	0	1	Yes	A
Active	x	x	Yes	A
			A=Active	I=Inactive

Ready is not a power condition. A device may post ready at the interface even though the media may not be accessible.

Also see specific power-related commands.

7.4 Removable media mode transitions

Figure 6 shows the minimum set of mode transitions that shall be implemented by removable media devices which contain a media change request mechanism (button) and support the DOOR LOCK and DOOR UNLOCK commands, and the MC and MCR bits in the Error register.



State A: Following a media change, the device is ready, the media is not locked, the door is closed, the media change request button is not active and a media change has been detected.

Path 1: The first command following a media change shall be rejected with the MC bit set in the Error register. The device shall then be moved to state B and the MC condition cleared.

State B: In normal operation, the device is ready, the media is not locked, the door is closed, the media change request button is not active and the MC bit is off.

Path 2: Activating the media change request button shall cause the device to complete any pending operations, spin down the device, if needed, and move to state E, allowing media removal.

Path 3: A DOOR LOCK command shall lock the media and move the device to state C.

State C: In normal operation, the device is ready, the media is locked, the door is closed and the media change request button is not active.

Path 4: A DOOR UNLOCK command shall unlock the media and move the device to state B.

Path 5: A DOOR LOCK command shall return good status.

Path 6: Pushing the media change button shall move the device to state D.

State D: The device is ready, the media is locked, the door is closed and the media change button is active.

Path 7: A DOOR LOCK command shall return MCR status.

Path 8: A DOOR UNLOCK command or a hard reset shall move the device to state E, allowing media removal.

State E: The device is not ready, the media is not locked and the door is open.

Path 9: A DOOR LOCK command shall return an ABRT error status.

Path 10: Closing the door shall move the device to state A (ready) and shall set the MC bit.

Figure 6 - Removable modes

7.5 Status and error posting

The status and errors that are valid for each command are defined in table 9. It is not a requirement that all valid conditions be implemented. See clauses 6.2.8 and 6.2.12 for the definition of the Error register and Status register bits.

Table 9 - Status and error usage

	Status register				Error register					
	DRDY	DF	CORR	ERR	BBK	UNC	IDNF	ABRT	TK0NF	AMNF
ACKNOWLEDGE MEDIA CHANGE	V	V		V				V		
BOOT - POST-BOOT	V	V		V				V		
BOOT - PRE-BOOT	V	V		V				V		
CHECK POWER MODE	V	V		V				V		
DOOR LOCK	V	V		V				V		
DOOR UNLOCK	V	V		V				V		
DOWNLOAD MICROCODE	V	V		V				V		
EXECUTE DEVICE DIAGNOSTIC	V	V		V	See 8.8					
FORMAT TRACK	V	V		V	V	V	V	V	V	V
IDENTIFY DEVICE	V	V		V				V		
IDLE	V	V		V				V		
IDLE IMMEDIATE	V	V		V				V		
INITIALIZE DEVICE PARAMETERS	V	V								
MEDIA EJECT	V	V		V				V		
NOP	V	V		V				V		
READ BUFFER	V	V		V				V		
READ DMA (w/ retry)	V	V	V	V	V	V	V	V		V
READ DMA (w/o retry)	V	V	V	V	V	V	V	V		V
READ LONG (w/ retry)	V	V		V	V		V	V		V
READ LONG (w/o retry)	V	V		V	V		V	V		V
READ MULTIPLE	V	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/ retry)	V	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/o retry)	V	V	V	V	V	V	V	V		V
READ VERIFY SECTOR(S) (w/ retry)	V	V	V	V	V	V	V	V		V
READ VERIFY SECTOR(S) (w/oretry)	V	V	V	V	V	V	V	V		V
RECALIBRATE	V	V		V				V	V	
SEEK	V	V		V			V	V		
SET FEATURES	V	V		V				V		
SET MULTIPLE MODE	V	V		V				V		
SLEEP	V	V		V				V		
STANDBY	V	V		V				V		
STANDBY IMMEDIATE	V	V		V				V		
WRITE BUFFER	V	V		V				V		
WRITE DMA (w/retry)	V	V		V	V		V	V		
WRITE DMA (w/0retry)	V	V		V	V		V	V		
WRITE LONG (w/retry)	V	V		V	V		V	V		
WRITE LONG (w/oretry)	V	V		V	V		V	V		
WRITE MULTIPLE	V	V		V	V		V	V		
WRITE SAME	V	V		V	V		V	V		
WRITE SECTOR(S) (w/ retry)	V	V		V	V		V	V		
WRITE SECTOR(S) (w/o retry)	V	V		V	V		V	V		
WRITE VERIFY	V	V	V	V	V	V	V	V		V
Invalid command code	V	V		V				V		

8. Command descriptions

Commands are issued to the device by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register.

Upon receipt of a command, the device sets the BSY bit or the DRQ bit within 400 ns. Following the setting of BSY bit equal to one or equal to zero and DRQ bit equal to one, the status presented by the device depends on the type of command: PIO data in, PIO data out, non-data transfer or DMA. See the individual command descriptions and clause 9 for the protocol followed by each command and command type.

NOTE 15 - Some older host implementations may require the BSY bit being set to zero and the DRQ bit equal to one in the Status register within 700 ns of receiving some PIO data out commands.

NOTE 16 - For the power mode related commands, it is recommended that the host utilize E0h through E3h, E5h and E6h command values. While command values 94h through 99h command values are valid, they should be considered obsolete and may be removed in future versions of this standard.

In table 10, the “proto” column codes represent the command protocol used:

DM - A DMA command;
ND - A non data command;
PI - A PIO data in command;
PO - A PIO data out command;
VS - A Vendor specific command.

The “typ” column codes represent the command type:

O - Optional—the implementation of this command is optional;
M - Mandatory—all ATA devices shall implement this command;
R - Reserved for use in future ATA standards;
V - Vendor specific implementation.

Table 10 - Command codes and parameters

		Command		Parameters Used				
proto		typ	code	FR	SC	SN	CY	DH
VS	ACKNOWLEDGE MEDIA CHANGE	O	DBh					D
VS	BOOT - POST-BOOT	O	Dch					D
VS	BOOT - PRE-BOOT	O	Ddh					D
ND	CHECK POWER MODE	O	98hE5h		y			D
VS	DOOR LOCK	O	Deh					D
VS	DOOR UNLOCK	O	Dfh					D
PO	DOWNLOAD MICROCODE	O	92h	y	y	y	y	D
ND	EXECUTE DEVICE DIAGNOSTIC	M	90h					D*
VS	FORMAT TRACK	V	50h					d
PI	IDENTIFY DEVICE	M	ECh					D
ND	IDLE	O	97hE3h		y			D
ND	IDLE IMMEDIATE	O	95hE1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	91h		y			y
ND	MEDIA EJECT	O	Edh					D
ND	NOP	O	00h					y
PI	READ BUFFER	O	E4h					D
DM	READ DMA (w/retry)	O	C8h		y	y	y	y
DM	READ DMA (w/o retry)	O	C9h		y	y	y	y
PI	READ LONG (w/retry)	O	22h		y	y	y	y
PI	READ LONG (w/o retry)	O	23h		y	y	y	y
PI	READ MULTIPLE	O	C4h		y	y	y	y
PI	READ SECTOR(S) (w/retry)	M	20h		y	y	y	y
PI	READ SECTOR(S) (w/o retry)	M	21h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/retry)	M	40h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/o retry)	M	41h		y	y	y	y
ND	RECALIBRATE	O	1xh					D
ND	SEEK	M	7xh			y	y	y
ND	SET FEATURES	O	Efh	y				D
ND	SET MULTIPLE MODE	O	C6h		y			D
ND	SLEEP	O	99hE6h					D
ND	STANDBY	O	96hE2h		y			D
ND	STANDBY IMMEDIATE	O	94hE0h					D
PO	WRITE BUFFER	O	E8h					D
DM	WRITE DMA (w/retry)	O	Cah		y	y	y	y
DM	WRITE DMA (w/o retry)	O	CBh		y	y	y	y
PO	WRITE LONG (w/retry)	O	32h	*	y	y	y	y
PO	WRITE LONG (w/o retry)	O	33h	*	y	y	y	y
PO	WRITE MULTIPLE	O	C5h	*	y	y	y	y
PO	WRITE SAME	O	E9h	y	y	y	y	y
PO	WRITE SECTOR(S) (w/retry)	M	30h	*	y	y	y	y
PO	WRITE SECTOR(S) (w/o retry)	M	31h	*	y	y	y	y
PO	WRITE VERIFY	O	3Ch	*	y	y	y	y
VS	Vendor specific	V	9Ah					
VS	Vendor specific	V	C0h-C3h					
VS	Vendor specific	V	8xh					
VS	Vendor specific	V	F0h-FFh					
--	Reserved: all remaining codes	R						

CY = Cylinder registers SC = Sector Count register DH = Device/Head register SN = Sector Number register
FR = Features register (see command descriptions for use)
y - the register contains a valid parameter for this command.
For the Device/Head register, y means both the device and head parameters are used.
D - only the device parameter is valid and not the head parameter.
d - the device parameter is valid, the usage of the head parameter is vendor specific.
D* - Addressed to device 0 but both devices execute it.
* - Maintained for compatibility (see 6.2.9).

Each command description in the following clauses contains the following subclauses:

OPCODE - Indicates the command code for this command.

TYPE - Indicates if the command is mandatory, optional or vendor specific and, if the command is a member of one or more feature sets, which feature sets it belongs to.

PROTOCOL - Indicates which protocol is used by the command.

INPUTS - Describes the Command Block register data that the host shall supply.

NORMAL OUTPUTS - Describes the Command Block register data that shall be returned by the device at the end of a command. The Status register shall always be valid and, if the ERR bit in the Status register is set to one, then the Error register shall be valid.

ERROR OUTPUTS - Describes the Command Block register data that shall be returned by the device at the end of a command which completes with an unrecoverable error.

PREREQUISITES - Any prerequisite commands or conditions that shall be met before the command can be issued.

DESCRIPTION - The description of the command function(s).

7.6 ACKNOWLEDGE MEDIA CHANGES (removable)

OPCODE - DBh

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

7.7 BOOT - POST-BOOT (removable)

OPCODE - DCh

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

7.8 BOOT - PRE-BOOT (removable)

OPCODE - DDh

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

7.9 CHECK POWER MODE

OPCODE - 98h or E5h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - The Sector Count register is set to 0 (00h) if the device is going to, in or leaving Standby mode. The Sector Count register is set to 255 (FFh) if the device is in Active or Idle mode.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - If the device is in, going to, or recovering from the Standby Mode the device shall set the BSY bit, set the Sector Count register to 0 (00h), clear the BSY bit, and assert INTRQ.

If the device is in Active or Idle Mode, the device shall set the BSY bit, set the Sector Count register to 255 (FFh), clear the BSY bit, and assert INTRQ.

7.10 DOOR LOCK (removable)

OPCODE - DEh

TYPE - Optional

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device is not ready or is not capable of locking the media, the ABRT bit in the Error register and the ERR bit in the Status register shall be returned.

If the device is already locked and the media change request button is active, then a Media Change Requested status shall be returned by setting the MCR bit in the Error register and the ERR bit in the Status register.

PREREQUISITES - None.

DESCRIPTION - This command either locks the device or media, or provides the status of the media change request button.

If the device is not locked, the device shall be set to the locked state and good status returned.

If the device is locked, the status returned shall indicate the state of the media change request button. Good status shall be returned while the media change request button is not active, and the MCR bit in the Error register and the ERR bit in the Status register shall be returned when the media change request button is active.

When a device is in a DOOR LOCKED state, the device shall not respond to the media change request button, except by setting the MCR status, until the DOOR LOCKED condition is cleared. A DOOR LOCK condition shall be cleared by a DOOR UNLOCK or MEDIA EJECT command, or by a hardware device reset.

7.11 DOOR UNLOCK (removable)

OPCODE - DFh

TYPE - Optional

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command or is not ready, then the ABRT bit shall be returned in the Error register and the ERR bit shall be returned in the Status register.

PREREQUISITES - None.

DESCRIPTION - This command shall unlock the device, if it is locked, and shall allow the device to respond to the media change request button.

7.12 DOWNLOAD MICROCODE

OPCODE - 92h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The head bits of the Device/Head register shall always be set to zero. The Cylinder High and Low registers shall be set to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support this command or did not accept the microcode data.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number Register and the Sector Count register. The Sector Number Register shall be used to extend the Sector Count register, to create a sixteen bit sector count value. The Sector Number Register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number Register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33 553 920 bytes, in 512 byte increments.
The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

01H - download is for immediate, temporary use
07H - save downloaded code for immediate and future use

All other values are reserved.

7.13 EXECUTE DEVICE DIAGNOSTIC

OPCODE - 90h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - None, except that the device selection bit in the Device/Head register is ignored.

NORMAL OUTPUTS - The diagnostic code written into the Error register is an 8-bit code as shown in table 11, and not as defined in 6.2.8.

Table 11 - Diagnostic Codes

Code	Description
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 1 failed, Device 0 passed
80h, 82h-FFh	Device 1 failed, Device 0 failed

The meaning of values other than 01h and 81h are vendor specific and should be considered a diagnostic failed condition.

ERROR OUTPUTS - None. All error information is returned as a diagnostic code in the Error register.

PREREQUISITES - None.

DESCRIPTION - This command shall perform the internal diagnostic tests implemented by the device. See also 6.2.8 and 6.2.12. The DEV bit in the Drive/Head register is ignored. Both devices, if present, shall execute this command.

Device 0 performs the following operations for this command:

a) Device 0 sets the BSY bit within 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;

b) Device 0 performs diagnostics;

c) Device 0 resets the Command Block registers to the following:

Cylinder Low = 00h Cylinder HigH = 00h
Sector Count = 01h Device/Head = 00h
Sector Number = 01h

d) Device 0 posts diagnostic results to bits 6-0 of the Error Register;

e) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 6 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received for Device 1 to assert PDIAG-. If PDIAG- is asserted within 6 seconds, Device 0 sets bit 7 to zero in the Error Register, else Device 0 sets bit 7 equal to 1 in the Error Register;

If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 sets bit 7 to zero in the Error register;

f) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1;

NOTE 17 - Device 0 shall clear the BSY bit within 6 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received.

g) Device 0 sets the DRDY bit when ready to accept any command.

NOTE 18 - Steps f) and g) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one to occur, a host is advised to allow up to 2 minutes for the DRDY bit to be set to one. See Figure 7.

Device 1 performs the following operations for this command:

a) Device 1 sets the BSY bit within 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;

b) Device 1 negates PDIAG- within 1 ms after the command is received;

c) Device 1 performs diagnostics;

d) Device 1 resets the Command Block registers to the following:

Cylinder Low = 00h Cylinder HigH = 00h
Sector Count = 01h Device/Head = 00h
Sector Number = 01h

e) Device 1 sets bit 7 of the Error register to zero and posts its diagnostic results to bits 6 through 0 of Error register;

f) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to one;

g) If Device 1 passed its diagnostics without error in step c), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step;

NOTE 19 - Device 1 shall clear the BSY bit and assert PDIAG- within 5 seconds of the time that the EXECUTE DEVICE DIAGNOSTIC command is received.

h) Device 1 sets the DRDY bit when ready to accept any command.

NOTE 20 - Steps f), g) and h) may occur at the same time. While no maximum time is specified for the DRDY bit to set to one, a host is advised to allow up to 2 minutes for the DRDY bit to be equal to one. See figure 7.

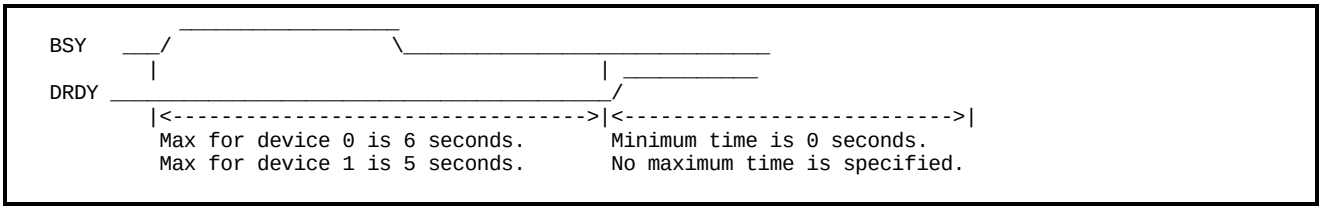


Figure 7 - BSY and DRDY timing for Diagnostic command

7.14 FORMAT TRACK

OPCODE - 50h

TYPE - Vendor specific.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Aborted Command if the device does not support this command. All other errors are vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - The implementation of the FORMAT TRACK command is vendor specific. It is recommended that system implementations not utilize this command.

7.15 IDENTIFY DEVICE

OPCODE - ECh

TYPE - Mandatory

PROTOCOL - PIO data in.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. The parameter words in the buffer have the arrangement and meanings defined in Table 12. All reserved bits or words shall be zero.

The F/V column indicates if the word or part of a word has fixed (F) contents that do not change, variable (V) contents that may change depending on the device state or the commands executed by the device, X for words with vendor specific data which may be fixed or variable, and R for reserved words which shall be zero. For removable media devices, the value of fields indicated as fixed (F) may change when media is removed or changed.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32 bit values (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD15 through DD0 respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD15 through DD0 respectively.

Some parameters are defined as a string of ASCII characters. For the string “Copyright”, the character ‘C’ is the first byte, ‘o’ is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (‘C’) is on bits DD15 through DD8 of the first word
the 2nd character (‘o’) is on bits DD7 through DD0 of the first word
the 3rd character (‘p’) is on bits DD15 through DD8 of the second word
the 4th character (‘y’) is on bits DD7 through DD0 of the second word
etc.

Table 12 - Identify device information

Word	F/V	
0		General configuration bit-significant information:
	F	15 0 reserved for non-magnetic devices
	F	14 Vendor specific (obsolete)
	F	13 Vendor specific (obsolete)
	F	12 Vendor specific (obsolete)
	F	11 Vendor specific (obsolete)
	F	10 Vendor specific (obsolete)
	F	9 Vendor specific (obsolete)
	F	8 Vendor specific (obsolete)
	F	7 1=removable media device
	F	6 1=not removable controller and/or device
	F	5 Vendor specific (obsolete)
	F	4 Vendor specific (obsolete)
	F	3 Vendor specific (obsolete)
	F	2 Vendor specific (obsolete)
	F	1 Vendor specific (obsolete)
	F	0 Reserved
1	F	Number of logical cylinders
2	R	Reserved
3	F	Number of logical heads
4	X	Vendor specific (obsolete)
5	X	Vendor specific (obsolete)
6	F	Number of logical sectors per logical track
7-9	X	Vendor specific
10-19	F	Serial number
20	X	Vendor specific (obsolete)
21	X	Vendor specific (obsolete)
22	F	# of vendor specific bytes avail on READ/WRITE LONG cmds
23-26	F	Firmware revision (8 ASCII characters)
27-46	F	Model number (40 ASCII characters)
47	X	15-8 Vendor specific
	F	7-0 00h=READ/WRITE MULTIPLE commands not implemented
	F	01h-FFh = Maximum number of sectors that can be transferred per interrupt on READ MULTIPLEand WRITE MULTIPLE commands
48	R	Reserved
49		Capabilities
	R	15-14 Reserved
	F	13 1=Standby timer values as specified in this standardare supported
		0=Standby timer values are vendor specific
	R	12 Reserved (for advanced PIO mode support)
	F	11 1=IORDY supported
	F	0=IORDY may be supported
	F	10 1=IORDY can be disabled
	F	9 1=LBA supported
	F	1=DMA supported
	X	7-0 Vendor specific

Table 12 - Identify device information (concluded)

Word	F/V	
50	R	Reserved
51	F	15-8 PIO data transfer cycle timing mode
	X	7-0 Vendor specific
52	F	15-8 DMA data transfer cycle timing mode
	X	7-0 Vendor specific
53	R	15-2 Reserved
	F	1 1=the fields reported in words 64-70 are valid
	F	0=the fields reported in words 64-70 are not valid
	V	0 1=the fields reported in words 54-58 are valid
	V	0=the fields reported in words 54-58 may be valid
54	V	Number of current logical cylinders
55	V	Number of current logical heads
56	V	Number of current logical sectors per track
57-58	V	Current capacity in sectors
59	R	15-9 Reserved
	V	8 1 = Multiple sector setting is valid
	V	7-0h xxh = Current setting for number of sectors that can be transferred per interrupt on R/W multiple command
60-61	F	Total number of user addressable sectors (LBA mode only)
62	V	15-8 Single word DMA transfer mode active
	F	7-0 Single word DMA transfer modes supported
63	V	15-8 Multiword DMA transfer mode active
	F	7-0 Multiword DMA transfer modes supported
64	R	15-8 Reserved
	F	7-0 Advanced PIO Transfer Modes Supported
65		Minimum Multiword DMA Transfer Cycle Time Per Word
	F	15-0 Cycle time in nanoseconds
66		Manufacturer's Recommended Multiword DMA Transfer Cycle Time
	F	15-0 Cycle time in nanoseconds
67		Minimum PIO Transfer Cycle Time Without Flow Control
	F	15-0 Cycle Time in nanoseconds
68		Minimum PIO Transfer Cycle Time With IORDY Flow Control
	F	15-0 Cycle Time in nanoseconds
69-70	R	Reserved (for advanced PIO mode support)
71-127	R	Reserved
128-159	X	Vendor specific
160-255	R	Reserved

If the device has been configured for eight bit transfers, then each word as defined in this table is transferred as described in 3.2.5.

7.15.1 Word 0: General configuration

Devices that conform to this standard shall set bit 15 to zero.

7.15.2 Word 1: Number of cylinders

The number of user-addressable logical cylinders in the default translation mode.

7.15.3 Word 2: Reserved.

7.15.4 Word 3: Number of logical heads

The number of user-addressable logical heads per logical cylinder in the default translation mode.

7.15.5 Word 4: Vendor specific data.

7.15.6 Word 5: Vendor specific data.

7.15.7 Word 6: Number of logical sectors per logical track

The number of user-addressable logical sectors per logical track in the default translation mode.

7.15.8 Words 7-9: Vendor specific data.

7.15.9 Words 10-19: Serial Number

If word 10 of this field is 0000h, then the serial number is not specified and the definition of the remaining words of this field are vendor specific.

If word 10 of this field is not equal to 0000h, then this field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

7.15.10 Word 20: Vendor specific data.

7.15.11 Word 21: Vendor specific data.

7.15.12 Word 22: Number of vendor specific bytes on READ/WRITE LONG commands

The contents of this field specifies the number of vendor specific bytes that are appropriate for the device. If the contents of this field are set to a value other than 4, the SET FEATURES command should be used to switch the length of READ LONG and WRITE LONG commands from 512 plus 4 to 512 plus the value specified in this word.

7.15.13 Word 23-26: Firmware revision

If word 23 of this field is 0000h, then the firmware revision is not specified and the definition of the remaining words of this field are vendor specific.

If word 23 of this field is not equal to 0000h, then this field contains the firmware revision of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

7.15.14 Words 27-46: Model number

If word 27 of this field is 0000h, then the model number is not specified and the definition of the remaining words of this field are vendor specific.

If word 27 of this field is not equal to 0000h, then this field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

7.15.15 Word 47: READ/WRITE MULTIPLE support.

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands. If a device supports the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits contain a non-zero value. If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits shall be zero.

7.15.16 Word 48: Reserved.

7.15.17 Word 49: Capabilities

7.15.17.1 Standby Timer Support

Bit 13 of word 49 is used to determine whether a device utilizes the Standby Timer values defined in this standard. If bit 13 is set to one, then the device utilizes the Standby Timer values as specified in table 13 (see 8.11). If bit 13 is set to zero, the timer values utilized are vendor specific.

7.15.17.2 IORDY Support

Bit 11 of word 49 is used to help determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This insures backward compatibility. If a device supports PIO Mode 3, then this bit shall be set.

7.15.17.3 IORDY Can Be Disabled

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Control of IORDY is accomplished using the SET FEATURES command.

7.15.17.4 LBA supported

Bit 9 of word 49 is used to indicate if the device supports LBA mode addressing. If this bit is set, words 60-61 shall be valid.

7.15.17.5 DMA supported

Bit 8 of word 49 is used to indicate if the device supports the READ/WRITE DMA commands.

7.15.18 Word 50: Reserved.

7.15.19 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 10 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in figure 10, and if it does not, then Mode 0 shall be used to serve as the default timing.

NOTE 21 - For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

7.15.20 Word 52: Single Word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 11 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 11 (i.e. 0, 1, or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

7.15.21 Word 53: Field Validity

If bit 0 of word 53 is set, then the values reported in words 54 through 58 are valid. If this bit is cleared, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set, then the values reported in words 64 through 70 are valid. If this bit is cleared, the values reported in words 64-70 are not valid. Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, shall set bit 1 of word 53 and support the fields contained in words 64 through 70.

7.15.22 Word 54: Number of current logical cylinders

The number of user-addressable logical cylinders in the current translation mode.

NOTE 22 - For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.15.23 Word 55: Number of current logical heads

The number of user-addressable logical heads per logical cylinder in the current translation mode.

NOTE 23 - For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.15.24 Word 56: Number of current logical sectors per logical track

The number of user-addressable logical sectors per logical track in the current translation mode.

NOTE 24 - For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.15.25 Word 57-58: Current capacity in sectors

The current capacity in sectors excludes all sectors used for device-specific purposes. The value reported in this field shall be the product of words 54, 55 and 56.

7.15.26 Word 59: Multiple sector setting

If bit 8 is set, then bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero.

7.15.27 Word 60-61: Total number of user addressable sectors

If the device supports LBA Mode, these words reflect the total number of user addressable sectors. This value does not depend on the current device geometry. If the device does not support LBA mode, these words shall be set to 0.

7.15.28 Word 62: Single word DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g. if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

7.15.29 Word 63: Multiword DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g.; if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

7.15.30 Word 64: Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes are capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3. Bit 1, if set, indicates that the device supports PIO Mode 4.

NOTE 25 - For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

7.15.31 Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time reported by the fastest DMA mode supported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.15.32 Word 66: Manufacturer's Recommended Multiword DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance MAY result.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.15.33 Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer Without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer, without utilization of flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.15.34 Word 68: Minimum PIO Transfer Cycle Time With IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 68 shall not be less than the fastest PIO mode reported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.15.35 Words 69-70: Reserved for future PIO modes.

Words 69 and 70 are reserved for future advanced PIO modes

7.15.36 Words 71-127: Reserved.

7.15.37 Words 128-159: Vendor specific.

7.15.38 Words 160-255: Reserved.

7.16 IDLE

OPCODE - 97h or E3h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby Timer. See table 13.

Table 13 - Automatic standby timer periods

Sector Count Register contents		Corresponding Timeout Period
0	(00h)	Timeout Disabled
1 - 240	(01h-F0h)	(value * 5) seconds
241 - 251	(F1h-FBh)	((value - 240) * 30) minutes
252	(Fch)	21 minutes
253	(FDh)	Vendor unique period between 8 and 12 hours
254	(Feh)	Reserved
255	(Ffh)	21 minutes 15 seconds

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Idle Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

7.17 Idle immediate

OPCODE - 95h or E1h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Idle Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

7.18 Initialize device parameters

OPCODE - 91h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Sector Count register specifies the number of logical sectors per logical track, and the Device/Head register which specifies the number of logical heads minus 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the requested CHS translation.

> NOTE 26 - Previous ATA specifications were unclear about the error conditions that this command may indicate. Some implementations do not indicate any errors for this command even when the command fails. However, most of these implementations do fail media access commands if a valid CHS translation is not in effect.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

Upon receipt of the command, the device sets the BSY bit, saves the parameters, clears the BSY bit, and generates an interrupt.

A device shall support the CHS translation described in words 1, 3 and 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the requested CHS translation is not supported, the device shall set the Error bit in the Status register and set the Aborted Command bit in the Error register before clearing the BSY bit in the Status register.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

> NOTE 27 - Host implementations should use the default CHS translation mode described in words 1, 3 and 6 of the IDENTIFY DEVICE information. Future ATA specifications may restrict the valid input parameters for this command to these values.
>
> NOTE 28 - Some ATA-1 devices require that this command be issued prior to media access.

7.19 Media eject (removable)

OPCODE - EDh

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None required.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - None.

DESCRIPTION - This command completes any pending operations, spins down the device if needed, unlocks the door or media if locked, and initiates a media eject, if required.

7.20 NOP

OPCODE - 00h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None required.

NORMAL OUTPUTS - The Command Block registers, other than the Error and Status registers, are not changed by this command.

ERROR OUTPUTS - This command always fails with an Aborted Command error.

PREREQUISITES - None.

DESCRIPTION - This command enables a host which can only perform 16-bit register accesses, to check device status. The device shall respond, as it does to an unrecognized command, by setting Aborted Command in the Error register, Error in the Status register, clearing Busy in the Status register, and asserting INTRQ.

NOTE 29 - When a 16-bit host writes to the Device/Head Register, one byte contains the Command register, so the device sees a new command when the intended purpose is only to select a device.

Both devices may be Busy but not necessarily Ready, e.g.; Device 0 may be ready, but not device 1. To check this possibility a typical sequence for an 8-bit host would be:

a) Read the Status register (wait until Busy False);

b) Select the device (write to the Device/Head Register);

c) Read the Status register (wait until Busy False and Ready True);

d) Send the command (write to the Command register).

As a 16-bit host executes b and d simultaneously, a problem occurs if the device being selected is Not Ready at the time the command is issued.

7.21 Read buffer

OPCODE - E4h

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - None required.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

PREREQUISITES - None.

NOTE 30 - A WRITE BUFFER command should immediately proceed a READ BUFFER command.

DESCRIPTION - The READ BUFFER command enables the host to read the current contents of the device's sector buffer. When this command is issued, the device sets the BSY bit, sets up the sector buffer for a read operation, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host then reads the data from the buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

7.22 Read DMA (with retries and without retries)

OPCODE - C8h (with retries) or C9h (without retries)

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to the READ SECTOR(S) command except for the following:

- the host initializes the DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the DMA channel

• the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.23 READ LONG (with retries and without retries)

OPCODE - 22h (with retries) or 23h (without retries)

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register shall not specify a value other than 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The SET FEATURES subcommand to enable more than 4 vendor specific bytes shall be executed prior to the READ LONG command if other than 4 vendor specific bytes are to be transferred.

DESCRIPTION - The READ LONG command performs similarly to the READ SECTOR(S) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. During a READ LONG command, the device does not check to determine if there has been a data error. Only single sector READ LONG operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD0-7 only (8-bits wide).

The “with retries” and “without retries” versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

NOTE 31 - Some ATA-1 devices are not capable of delivering the 8 bit ECC immediately after the word sector data. BIOS and driver developers should use PIO mode 0 for 8 bit ECC accesses.

7.24 READ MULTIPLE

OPCODE - C4h

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - A successful SET MULTIPLE MODE command shall precede a READ MULTIPLE command.

DESCRIPTION - The READ MULTIPLE command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command. Command execution is identical to the READ SECTOR(S) operation except that the number of sectors defined by a SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where n = remainder (SECTOR COUNT / block count).

If the READ MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with an Aborted Command error.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

7.25 READ SECTOR(S) (with retries and without retries)

OPCODE - 20h (with retries) or 21h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command reads from 1 to 256 sectors as specified in the Sector Count register. A SECTOR COUNT of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

The DRQ bit is always set prior to data transfer regardless of the presence or absence of an error condition.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.26 READ VERIFY SECTOR(S) (with retries and without retries)

OPCODE - 40h (with retries) or 41h (without retries)

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be verified. The Sector Count register specifies the number of sectors to be verified.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command is identical to the READ SECTOR(S) command, except that the DRQ bit is never set, and no data is transferred to the host.

When the requested sectors have been verified, the device clears the BSY bit and generates an interrupt.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.27 RECALIBRATE

OPCODE - 10h through 1Fh

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None.

NORMAL OUTPUTS - If the command is executed in CHS addressing mode, Cylinder High, Cylinder Low and the head portion of Device/Head shall be zero. The Sector Number register shall be 1. If the command is executed in LBA addressing mode, the Cylinder High, Cylinder Low, the head portion of the Device/Head and the Sector Number register shall be zero.

ERROR OUTPUTS - If the device cannot reach cylinder 0, a Track 0 Not Found error is posted.

PREREQUISITES - None.

DESCRIPTION - The function performed by this command is vendor specific.

7.28 SEEK

OPCODE - 70h through 7Fh

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder High, Cylinder Low, head portion of the Device/Head register and the Sector Number register contain the sector address to which the device should move the read/write heads.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - The function performed by this command is vendor specific.

7.29 SET FEATURES

OPCODE - EFh

TYPE - The command is optional and if implemented each subcommand is optional.

PROTOCOL - Non-data.

INPUTS - The Feature register contains a subcommand code as described in table 14. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

NORMAL OUTPUTS - See the subcommand descriptions.

ERROR OUTPUTS - If the device does not support the command or if any input value is not supported or is invalid, the device posts an Aborted Command error.

PREREQUISITES - None.

DESCRIPTION - This command is used by the host to establish the following parameters which affect the execution of certain device features as shown in table 14.

Table 14 - SET FEATURES register definitions

01h	Enable 8-bit data transfers (see 6.2.5)
02h	Enable write cache *
03h	Set transfer mode based on value in Sector Count register
33h	Disable retry *
44h	Length of vendor specific bytes on READ LONG/WRITE LONG cmds
54h	Set cache segments to Sector Count register value *
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults (see 8.25)
77h	Disable ECC *
81h	Disable 8-bit data transfers (see 6.2.5)
82h	Disable write cache *
88h	Enable ECC *
99h	Enable retries *
AAh	Enable read look-ahead feature
ABh	Set maximum prefetch using Sector Count register value *
BBh	4 bytes of vendor specific byts on READ LONG/WRITE LONG cmds
CCh	Enable reverting to power on defaults (see 8.25)
	*These feature definitions are vendor specific

All values not contained in table 14 are reserved for future definition.

At power on, or after a hardware reset, the default setting of the functions specified by the subcommands are vendor specific.

A setting of 66h allows settings of greater than 80h which may have been modified since power on to remain at the same setting after a software reset.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000 000
PIO Default Transfer Mode, Disable IORDY	0000 001
PIO Flow Control Transfer Mode x	00001 nnn
Single Word DMA Mode x	00010 nnn
Multiword DMA Mode x	00100 nnn
Reserved	01000 nnn
Reserved	10000 nnn

Where “nnn” is a valid mode number in binary and “x” is the mode number in decimal for the associated transfer type.

NOTE: 32 - It is intended that the reserved values be used for future specification of an alternative flow control mechanism.

If a device supports this specification, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000 000”, it shall set its default PIO transfer mode. If the value is “00000 001” and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

See vendor specification for the default mode of the commands which are vendor specific.

Devices reporting support for Multi Word DMA Transfer Mode 1 shall also support Multi Word DMA Transfer Mode 0. Support of IORDY is mandatory when PIO Mode 3 or above is the current mode of operation.

7.30 SET MULTIPLE MODE

OPCODE - C6h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - The Sector Count register contains number of sectors per block to use on all following READ/WRITE MULTIPLE commands.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands or if a block count is not supported, a Aborted Command error is posted, and READ MULTIPLE and WRITE MULTIPLE commands are disabled.

PREREQUISITES - None.

DESCRIPTION - This command enables the device to perform READ AND WRITE MULTIPLE operations and establishes the block count for these commands.

Devices shall support the block size specified in the IDENTIFY DRIVE parameter word 47, bits 7 through 0, and may also support smaller values.

Upon receipt of the command, the device sets the BSY bit equal to one and checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported, the value is used for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and their execution is enabled.

If the Sector Count register contains 0 when the command is issued, READ AND WRITE MULTIPLE commands are disabled.

At power on, or after a hardware reset, the default mode is READ AND WRITE MULTIPLE disabled. Following a software reset, the READ and WRITE MULTIPLE commands may be enabled or disabled. The SET FEATURES command Disable Reverting To Power on Defaults and Enable Reverting To Power on Defaults subcommands, if supported, can be used to control the results of a software reset.

7.31 SLEEP

OPCODE - 99h or E6h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command is the only way to cause the device to enter Sleep Mode.

This command causes the device to set the BSY bit, prepare to enter Sleep mode, clear the BSY bit and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow the device to enter Sleep mode. In Sleep mode the interface becomes inactive without affecting the operation of the ATA interface. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically deassert INTRQ and enter Sleep mode after a vendor specified time period of not less than 2 seconds.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

A device shall not power on in Sleep Mode nor remain in Sleep Mode following a reset sequence.

7.32 STANDBY

OPCODE - 96h or E2h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. See table 13, 8.11.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

7.33 STANDBY IMMEDIATE

OPCODE - 94h or E0h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

7.34 WRITE BUFFER

OPCODE - E8h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to overwrite the contents of one sector in the device's buffer. When this command is issued, the device sets the BSY bit, sets up the buffer for a write operation, sets the DRQ bit, clears the BSY bit, and waits for the host to write the data. Once the host has written the data, the device sets the BSY bit, clears the BSY bit, and generates an interrupt.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

7.35 WRITE DMA (with retries and without retries)

OPCODE - CAh (with retries) or CBh (without retries)

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except for the following:

- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

The “with retries” and “without retries” versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.36 WRITE LONG (with retries and without retries)

OPCODE - 32h (with retries) or 33h (without retries)

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register shall not specify a value other than 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The SET FEATURES subcommand to enable other than 4 vendor specific bytes shall be executed prior to the WRITE LONG command if other than 4 vendor specific bytes are to be transferred.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself. Only single sector WRITE LONG operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD0-7 only (8-bits wide).

The “with retries” and “without retries” versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.37 WRITE MULTIPLE

OPCODE - C5h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - A successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command. interrupts are not generated on every sector, but on the transfer of a block that contains the number of sectors defined by SET MULTIPLE MODE.

Command execution is identical to the WRITE SECTOR(S) operation except that the number of sectors defined by the SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where n = Remainder (SECTOR COUNT / block count).

If the WRITE MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with an Aborted Command error.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

7.38 WRITE SAME

OPCODE - E9h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Feature register contains a subcommand code, either 22H or DDH. If the Feature register contains 22H, the Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be written (not the

number of sectors transferred by the host). If the Feature register contains code DDH, the Cylinder High, Cylinder Low, head portion of the Device/Head, Sector Number and Sector Count registers are not used.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command, if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

NORMAL OUTPUTS - If no error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector written. If the command ends with an error, these registers contain the address of the sector where the first error was detected and the Sector Count register contains the number of sectors remaining to be transferred in order to complete the original request.

ERROR OUTPUTS - If the Feature register contains a value other than 22H or DDH, the command shall be rejected with an aborted command error. Other errors possible are Bad Block, Uncorrectable Data Error, ID Not Found and Address Mark Not Found.

PREREQUISITES - None.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except that only one sector of data is transferred. The contents of the sector are written to the media one or more times.

> NOTE 33 - The WRITE SAME command allows for initialization of part or all of the medium to the specified data with a single command.

If the Features register is 22H, the device shall write that part of the medium specified by the Sector Number and sector address registers.

The support of the Features register value of DDH is optional. If the Features register contains DDH and is supported, the device shall initialize all the user accessible media.

The device issues an interrupt to indicate that the command is complete. Any error encountered during execution results in the termination of the write operation.

It is recommend that system implementations not utilize this command.

7.39 WRITE SECTOR(S) (with retries and without retries)

OPCODE - 30h (with retries) or 31h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command writes from 1 to 256 sectors as specified in the Sector Count register. A SECTOR COUNT of 0 requests 256 sectors.

The “with retries” and “without retries” versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.40 WRITE VERIFY

OPCODE - 3Ch

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command, except that each sector is verified from the media after being written and before the command is completed.

8. Protocol

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if the BSY bit is equal to one, and should proceed no further unless and until the BSY bit is equal to zero. For most commands, the host shall also wait for the DRDY bit to be equal to one before proceeding. The commands shown with DRDY=x can be executed when the DRDY bit is equal to zero.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of ATA devices.

A device shall maintain either the BSY bit equal to one or the DRQ bit equal to one at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while the BSY bit is equal to one or the DRQ bit is equal to one is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding. Host programmers are warned

against setting unrealistically short command timeout periods since this may impact a device's ability to perform device level retry and data recovery activities.

8.1 Power on and hardware resets

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of power on and hardware resets.

The timing assumes the following:

a) DASP- is asserted by Device 1 and received by Device 0 at power-on or hardware reset to indicate the presence of Device 1. At all other times it is asserted by Device 0 or Device 1 to indicate when a device is active;

b) PDIAG- is asserted by Device 1 and detected by Device 0. It is used by Device 1 to indicate to Device 0 that it has completed diagnostics without error and is ready to accept commands from the Host (BSY bit is cleared). This does not indicate that the device is ready, only that it can accept commands.

8.1.1 Power on and hardware resets - device 0

a) Host asserts RESET- for a minimum of 25 usec;
b) Device 0 sets the BSY bit no later than 400 ns after RESET- is negated;
c) Device 0 negates DASP- no later than 1 ms after RESET- is negated;
d) Device 0 samples for at least 450 ms for DASP- to be asserted from Device 1. This sampling starts 1 ms after RESET- is negated;
e) Device 0 performs hardware initialization and diagnostics;
f) Device 0 may revert to its default condition;
g) If Device 0 detected that DASP- was asserted during step d), then Device 0 waits up to 31 seconds for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 seconds, Device 0 sets bit 7 equal to 0 in the Error Register, else Device 0 sets bit 7 equal to 1 in the Error Register. If DASP- assertion was not detected in step d) Device 0 sets bit 7 equal to 0 in the Error Register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h. Device 0 shall store whether or not Device 1 was detected in step d) because this information is need in order to process any Software reset or EXECUTE DEVICE DIAGNOSTIC command later;
h) Device 0 posts diagnostic results to bits 6-0 of the Error Register;
i) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 seconds from the time that RESET- is negated;
j) Device 0 sets the DRDY bit when ready to accept any command.

NOTE 34 - Steps i) and j) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to 1, a host should allow up to 2 minutes for the DRDY bit to become 1. See figure 8.

8.1.2 Power on and hardware resets - device 1

a) Host asserts RESET- for a minimum of 25 us;
b) Device 1 sets the BSY bit no later than 400 ns after RESET- is negated;
c) Device 1 negates DASP- no later than 1 ms after RESET- is negated;
d) Device 1 negates PDIAG- before asserting DASP-;
e) Device 1 asserts DASP- no later than 400 ms after RESET- is negated;
f) Device 1 performs hardware initialization and diagnostics;
g) Device 1 may revert to its default condition;
h) Device 1 posts diagnostic results to the Error Register;

i) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1;
j) If Device 1 passed its diagnostics without error in step f), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step. Device 1 shall clear the BSY bit, and optionally assert PDIAG-, no later than 30 seconds from the time RESET- is negated. The device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h;
k) Device 1 sets the DRDY bit when ready to accept any command;

NOTE 35 - Steps i), j) and k) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to 1, a host should allow up to 2 minutes for the DRDY bit to become 1. See figure 8.

l) Device 1 negates DASP- after the first command is received or negates DASP- if no command is received within 31 seconds after RESET- is asserted.

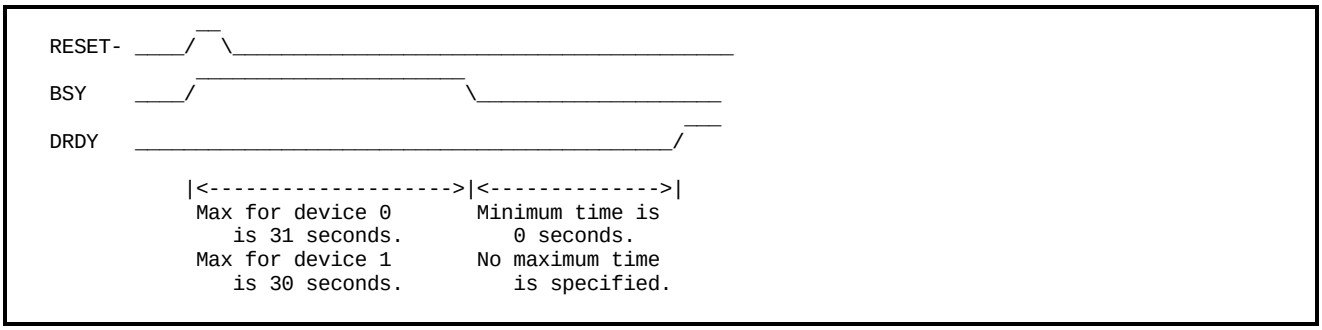


Figure 8 - BSY and DRDY timing for power on and hardware resets

8.2 Software reset

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of software resets.

8.2.1 Software reset - device 0

a) Host sets the SRST bit to 1 in the Device Control register;
b) Device 0 sets BSY bit no later than 400 ns after detecting that the SRST bit is equal to 1;
c) Device 0 performs hardware initialization and diagnostics;
d) Device 0 may revert to its default condition;
e) Device 0 posts diagnostic results to the Error Register;
f) Device 0 waits for the host to set the SRST bit to 0;
g) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 31 seconds from the time that the SRST bit to become 0 for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 seconds, Device 0 sets bit 7 equal to 0 in the Error Register, else Device 0 sets bit 7 equal to 1 in the Error Register. If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 sets bit 7 equal to 0 in the Error register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h;
h) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 seconds from the time that the host sets the SRST bit equal to 0;

NOTE 36 - Steps g) and h) may occur very rapidly.

i) Device 0 sets the DRDY bit when ready to accept any command.

NOTE 35 - Steps h) and i) may occur at the same time. While no maximum time is specified for the DRDY bit to become equal to 1 to occur, a host should allow up to 2 minutes for the DRDY bit to be set to 1. See figure 9.

8.2.2 Software reset - device 1

a) Host sets SRST bit to 1 in the Device Control register;
b) Device 1 set the BSY bit no later than 400 ns after detecting that the SRST bit to equal to 1;
c) Device 1 negates PDIAG- no later than 1 ms after detecting that the SRST bit is 1;
d) Device 1 perform hardware initialization and diagnostics;
e) Device 1 may revert to its default condition;
f) Device 1 posts diagnostic results to the Error Register;
g) Device 1 waits for the host to set the SRST bit equal to 0;
h) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1;
i) If Device 1 passed its diagnostics without error in step d), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step. Device 1 shall clear the BSY bit, optionally assert PDIAG-, no later than 30 seconds from the time the host sets the SRST bit to 0. The device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h;
j) Device 1 sets the DRDY bit when ready to accept any command.

NOTE 38 - Steps h), i) and j) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to 1, a host should allow up to 2 minutes for the DRDY bit to become 1. See figure 9.

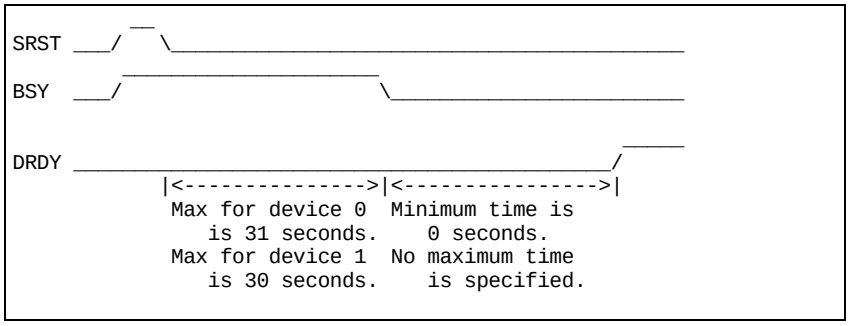


Figure 9 - BSY and DRDY timing for software reset

8.3 PIO data in commands

This class includes:

* IDENTIFY DEVICE
* READ BUFFER
* READ LONG (with and without retry)
* READ SECTOR(S) (with and without retry)
* READ MULTIPLE

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. The following steps describe the processing of a PIO data in command. This description does not include all possible error conditions.

PIO data in protocol:

a) The host reads the Status or Alternate Status register until BSY bit to become equal to 0;

b) The host writes the Device/Head register with the appropriate DEV bit value;

c) The host reads the Status or Alternate Status register until the BSY bit is equal to 0 and the DRDY bit is equal to 1;

d) The host writes any required command parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low and Device/Head registers;

e) The host writes the command code to the Command register;

f) The device sets the BSY bit and prepares to execute the command including preparation to transfer the first block of data to the host;

g) When the block of data is available, the device sets the DRQ bit (setting the DRQ bit is optional if an error condition exists). If there is an error condition, the device sets the appropriate status and error bits as required by that error condition. Finally, the device clears the BSY bit and then asserts INTRQ;

NOTE 39 - There may be times when the BSY bit is set in step f) and then cleared in step g) so quickly, that the host may not be able to detect that the BSY bit had been set.

h) After detecting either BSY bit is equal to 0 by polling the Alternate Status register or INTRQ, the host reads and saves the contents of the Status register;

i) If the DRQ bit is set, the host transfers a block of data by reading the Data register. If any error conditions are present in the status read in step h), the data transfer may not be valid;

j) In response to the Status register being read, the device negates INTRQ. In response to the complete data block being read, one of the following actions is taken:

- If no error status was presented to the host in step h) and if transfer of another block is required, the device sets the BSY bit and the above sequence is repeated from step g).

- If an error status was present in the Status read in step h), the device clears the DRQ bit and the command execution is complete.

- If the last block was transferred, the device clears the DRQ bit and the command execution is complete.

The following diagrams the PIO data in steps:

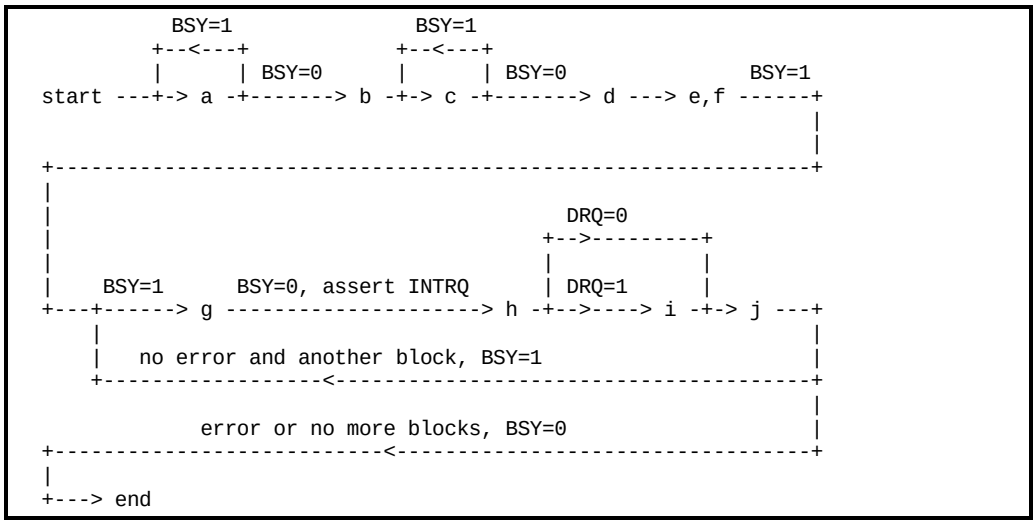


Figure 10 - PIO data in

8.4 PIO data out commands

This class includes:

* DOWNLOAD MICROCODE
* FORMAT TRACK
* WRITE BUFFER
* WRITE LONG (with and without retry)
* WRITE MULTIPLE
* WRITE SAME
* WRITE SECTOR(S) (with and without retry)
* WRITE VERIFY

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. The following steps describe the processing of a PIO data out command. This description does not include all possible error conditions.

PIO data out protocol:

a) The host reads the Status or Alternate Status register until BSY bit is equal to 0;

b) The host writes the Device/Head register with the appropriate DEV bit value;

c) The host reads the Status or Alternate Status register until BSY bit is equal to 0 and the DRDY bit is equal to 1;

d) The host writes any required command parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low and Device/Head registers;

e) The host writes the command code to the Command register;

f) The device sets the BSY bit and prepares to execute the command including preparation to receive the first block of data from the host;

g) When ready to receive the first block of data from the host, the device sets the DRQ bit (setting the DRQ bit is optional if an error condition exists) and any other status or error bits as required and clears the BSY bit;

> NOTE 40 - There may be times when the BSY bit is set in step f) and then cleared in step g) so quickly, that the host may not be able to detect that the BSY bit had been set.

h) The host reads the Status or Alternate Status register until BSY bit is equal to 0;

i) If the DRQ bit is set, the host transfers a complete block of data to the device by writing the Data register;

j) Next, one of the following actions is taken:

> - If any error status was present in the status read in step h), the device clears the DRQ bit, asserts INTRQ and the command execution is complete. The data transferred in step i) is not processed by the device.
>
> - If no error status was presented to the host in step h), the device sets the BSY bit and processing continues with the next step;

k) The device processes the data block just received from the host. When this processing is completed, one of the following actions is taken:

- If no error occurred while processing the data block and if no additional blocks are to be transferred, the device clears the BSY bit and then asserts INTRQ. Command execution is complete;

- If an error occurred while processing the data block the device sets the appropriate status and error bits as required by that error condition. The device clears the BSY bit and then asserts INTRQ. Command execution is complete;

- If no error occurred while processing the data block and if transfer of another block is required, processing continues with the next step;

l) When ready to receive the next data block from the host, the device sets the DRQ bit, clears the BSY bit and then asserts INTRQ;

m) After detecting either the BSY bit is equal to 0 by polling the Alternate Status register or INTRQ, the host reads the contents of the Status register;

n) The host transfers a complete block of data to the device by writing the Data register;

o) The device sets the BSY bit and processing continues at step k).
The following diagrams the PIO data out steps:

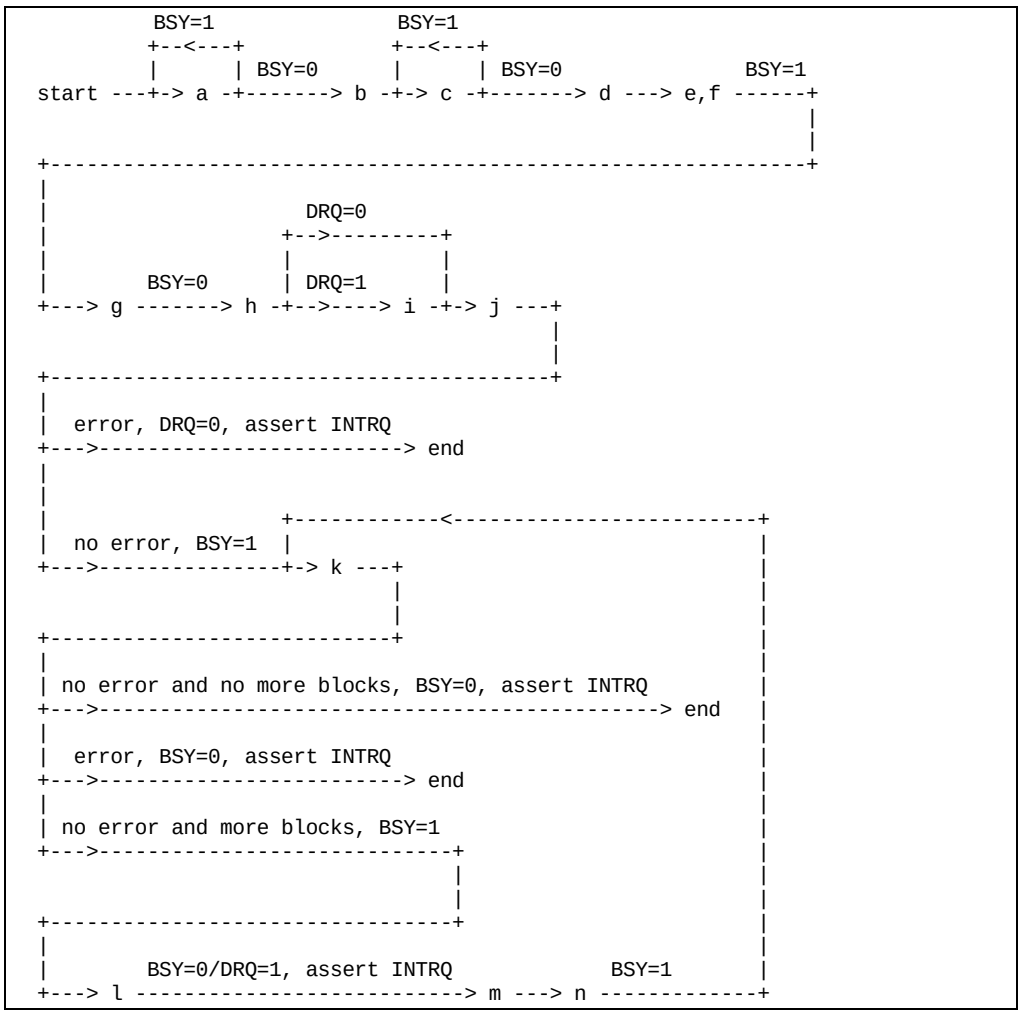


Figure 11 - PIO data out

8.5 Non-data commands

This class includes:

* CHECK POWER MODE
* DOOR LOCK
* DOOR UNLOCK
* EXECUTE DEVICE DIAGNOSTIC (DRDY=x)
* IDLE
* IDLE IMMEDIATE
* INITIALIZE DEVICE PARAMETERS (DRDY=x)
* MEDIA EJECT
* NOP
* READ VERIFY SECTOR(S)
* RECALIBRATE
* SEEK
* SET FEATURES
* SET MULTIPLE MODE
* SLEEP
* STANDBY
* STANDBY IMMEDIATE

Execution of these commands involves no data transfer. The following steps describe the processing of a no data transfer command. This description does not include all possible error conditions. See the EXECUTE DEVICE DIAGNOSTICS command description in 8.8, the NOP command description in 8.15 and the SLEEP command description in 8.26 for additional protocol requirements.

a) The host reads the Status or Alternate Status register until the BSY bit is equal to 0;

b) The host writes the Device/Head register with the appropriate DEV bit value;

c) The host reads the Status or Alternate Status register until the BSY bit is equal to 0 and the DRDY bit is equal to 1;

d) The host writes any required command parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low and Device/Head registers;

e) The host writes the command code to the Command register;

f) The device sets the BSY bit and executes the command. If any error occurs while processing the command, the device set the appropriate status and error bits as required by the error condition;

g) When command processing is completed, the device clears the BSY bit and then asserts INTRQ. Command processing is complete.

Figure 12 shows the no data transfer steps:

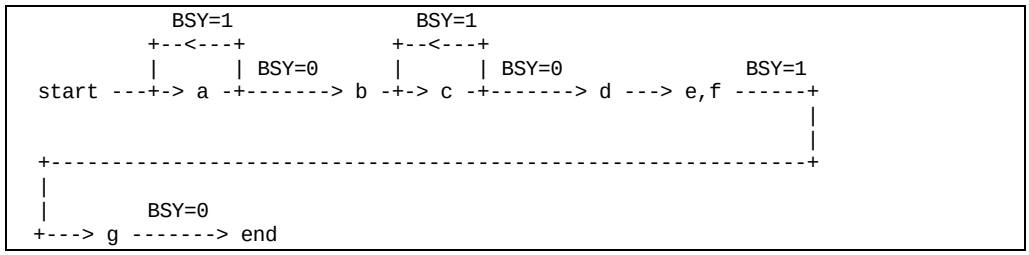


Figure 12 - No data transfer

8.6 DMA data transfer commands (optional)

This class comprises:

* READ DMA (with and without retry)
* WRITE DMA (with and without retry)

Data transfers using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the DMA channel;

- A single interrupt is issued at the completion of the command.

Initiation of the DMA transfer commands is identical to the READ SECTOR(S) or WRITE SECTOR(S) commands except that the host initializes the DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that no intermediate sector interrupts are issued on multi-sector commands.

The following steps describe the execution of a DMA command.

a) The host reads the Status or Alternate Status register until the BSY bit is equal to 0;

b) The host writes the Device/Head register with the appropriate DEV bit value;

c) The host reads the Status or Alternate Status register until the BSY bit is equal to 0 and the DRDY bit is equal to 1;

d) The host writes any required command parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low and Device/Head registers;

e) The host initializes the DMA channel;

NOTE 40 - This step may be performed at anytime after step b) and prior to step f).

f) The host writes the command code to the Command register;

g) The device sets the BSY bit and prepares to execute the command;

h) When the device is ready to transfer data, the device asserts DMARQ. The DMA data transfer may be split into several partial transfers at the discretion of the device or DMA channel. The device shall have either the BSY bit or the DRQ bit in the status registers during the entire DMA data transfer phase. If any error occurs the device set the appropriate status and error bits for the error condition. Data transfer is optional if an error condition exists;

i) When the device has completed processing, it clears both the BSY bit and the DRQ bit and then asserts INTRQ. Command processing is complete;

j) The host resets the DMA channel.

Figure 13 shows the DMA steps:

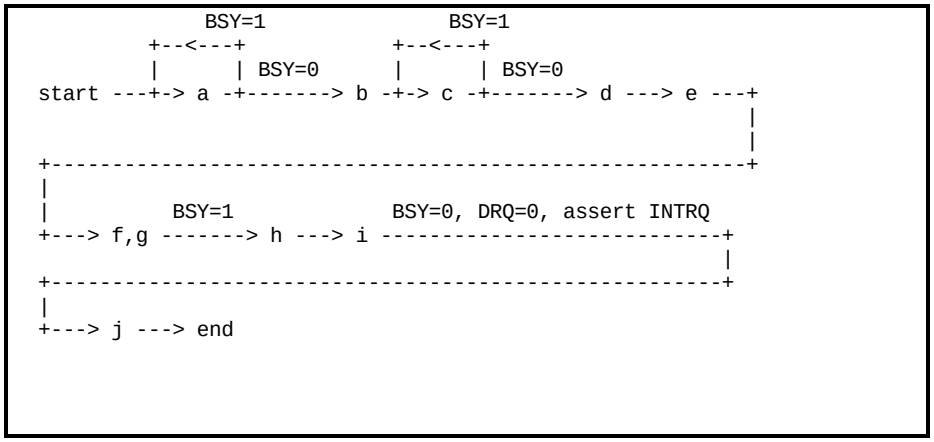


Figure 13 - DMA steps

8.7 Device 0 only configurations

In a single device configuration where device 0 is the only device and the host selects device 1, device 0 may respond to accesses of the Command Block and Control Block registers in one of two methods. These two methods exist because previous versions of the ASCI X3T10 standard did not specify the required behavior for this configuration. The first method is the recommended implementation.

The first method is:

a) A write to the Device Control register shall complete as if device 0 was the selected device;

b) A write to the Command Block register, other than the Command register, shall complete as if device 0 was selected;

c) A write to the Command register is ignored;

d) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if device 0 was selected;

e) A read of the Status or Alternate status register returns the value 00H.

NOTE 41 - IDX is vendor specific and might change following reset or power mode changes resulting in other values for status other than 00H.

The second method requires that device 0 implement an Error, Status and Alternate Status register that is used whenever device 1 is selected.

The second method is:

a) The device 1 Error, Status and Alternate status registers are set to 00H by a reset;

NOTE 42 - IDX is vendor specific and might change following reset or power mode changes resulting in other values for status other than 00H.

b) A write to the Device Control register shall complete as if device 0 was the selected device;

c) A write to the Command Block register, other than the Command register, shall complete as if device 0 was selected;

d) A write to the Command register with a command code other than the INITIALIZE DEVICE PARAMETERS or EXECUTE DEVICE DIAGNOSTICS command causes the device 1 Error, Status and Alternate status registers to be used as follows:

1) the BSY bit is set in the device 1 status register;

2) the ABRT bit is set in the device 1 Error register;

3) the ERR bit is set in the device 1 status registers;

4) the BSY bit is cleared in the device 1 status register;

5) if the nIEN bit in the Device Control Register is cleared, the INTRQ signal is asserted;

e) An EXECUTE DEVICE DIAGNOSTIC command is executed as if it addressed to device 0;

f) An INITIALIZE DEVICE PARAMETERS command is executed as if device 1 is present and is actually executing the command. The command shall have no effect of the device parameters of device 0;

g) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if device 0 was selected;

h) A read of the Error, Status or Alternate status register returns the value in the device 1 copy of these registers. The device 1 status registers shall contain 00H following a reset and the value 01H following an attempt to execute a command, other than EXECUTE DEVICE DIAGNOSTICS or INITIALIZE DEVICE PARAMETERS, on device 1.

9. Timing

9.1 Deskewing

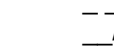
The host shall provide cable deskewing for all signals originating from the controller. The device shall provide cable deskewing for all signals originating at the host.

All timing values and diagrams are shown and measured at the connector of either device connected to the ATA interface. No values are given for measurement at the host interface.

9.2 Symbols

Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

/ or \ - signal transition (asserted or negated) *
< or > - data transition (asserted or negated)
XXXXXX - undefined but not necessarily released
. . . - the "other" condition if a signal is shown with no change
#n - used to number the sequence in which events occur, e.g.; #a, #b


- a degree of uncertainty as to when a signal may be asserted

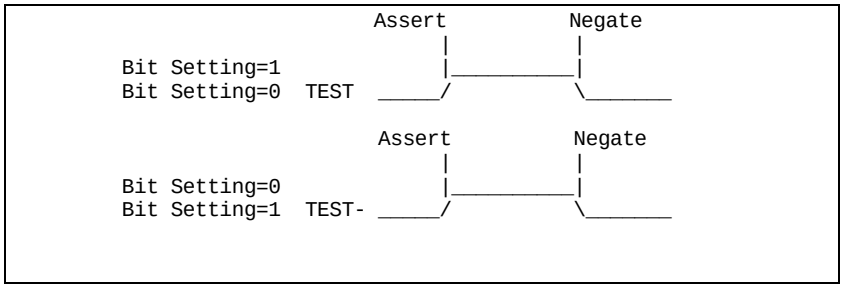

- a degree of uncertainty as to when a signal may be negated

* All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

9.3 Terms

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted e.g. the following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



9.4 Data transfers

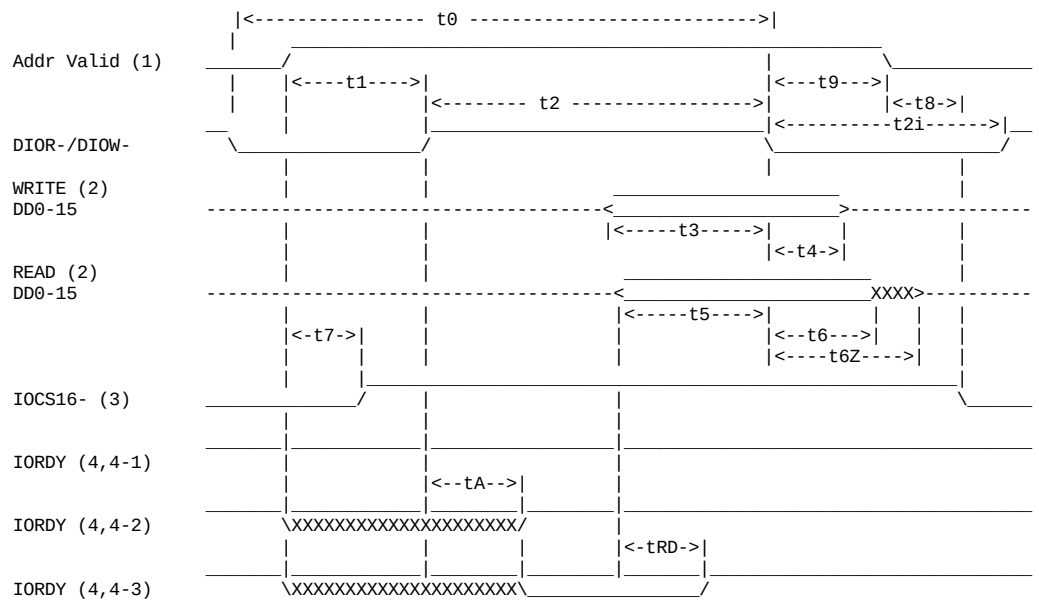
The minimum cycle time supported by the device in PIO Mode 3, 4 and Multiword DMA Mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated Mode e.g.; a drive supporting PIO Mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for Mode 4 PIO Timings.

9.4.1 PIO data transfers

Figure 14 defines the relationships between the interface signals for both 16-bit and 8-bit PIO data transfers. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the Identify Drive parameter list. The value in word 68 shall not be less than the value shown in the table below.

It is mandatory that IORDY be supported when PIO Mode 3 or 4 are the current mode of operation.



NOTES:
(1) Device Address consists of signals CS0-, CS1- and DA2-0
(2) Data consists of DD0-15 (16-bit) or DD0-7 (8-bit)
(3) IOCS16- shown for PIO modes 0,1 and 2. For other modes, this signal is not valid. (See clause 5.2.11)
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
(4-1) Device never negates IORDY: no wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: no wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD0-15 for tRD before causing IORDY to be asserted.

Figure 14 - PIO Data Transfer to/from Device

	PIO timing parameters	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Notes
t0	Cycle time (min)	600 ns	383 ns	240 ns	180 ns	120 ns	(1)
t1	Address valid to DIOR-/DIOW- setup (min)	70 ns	50 ns	30 ns	30 ns	25 ns	
t2	DIOR-/DIOW- 16-bit (min)	165 ns	125 ns	100 ns	80 ns	70 ns	(1)
	Pulse width 8-bit (min)	290 ns	290 ns	290 ns	80	70 ns	(1)
t2i	DIOR-/DIOW- recovery time (min)	-	-	-	70 ns	25 ns	(1)
t3	DIOW- data setup (min)	60 ns	45 ns	30 ns	30 ns	20 ns	
t4	DIOW- data hold (min)	30 ns	20 ns	15 ns	10 ns	10 ns	
t5	DIOR- data setup (min)	50 ns	35 ns	20 ns	20 ns	20 ns	
t6	DIOR- data hold (min)	5 ns	5 ns	5 ns	5 ns	5 ns	
t6Z	DIOR- data tristate (max)	30 ns	30 ns	30 ns	30 ns	30 ns	(2)
t7	Addr valid to IOCS16- assertion (max)	90 ns	50 ns	40 ns	n/a	n/a	(4)
t8	Addr valid to IOCS16- released (max)	60 ns	45 ns	30 ns	n/a	n/a	(4)
t9	DIOR-/DIOW- to address valid hold	20 ns	15 ns	10 ns	10 ns	10 ns	
tRd	Read Data Valid to IORDY active (min)	0 ns	0 ns	0 ns	0 ns	0 ns	
	(if IORDY initially low after tA)						
tA	IORDY Setup time	35 ns	35 ns	35 ns	35 ns	35 ns	(3)
tB	IORDY Pulse Width (max)	1250 ns	1250 ns	1250 ns	1250 ns	1250 ns	

Notes -

(1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

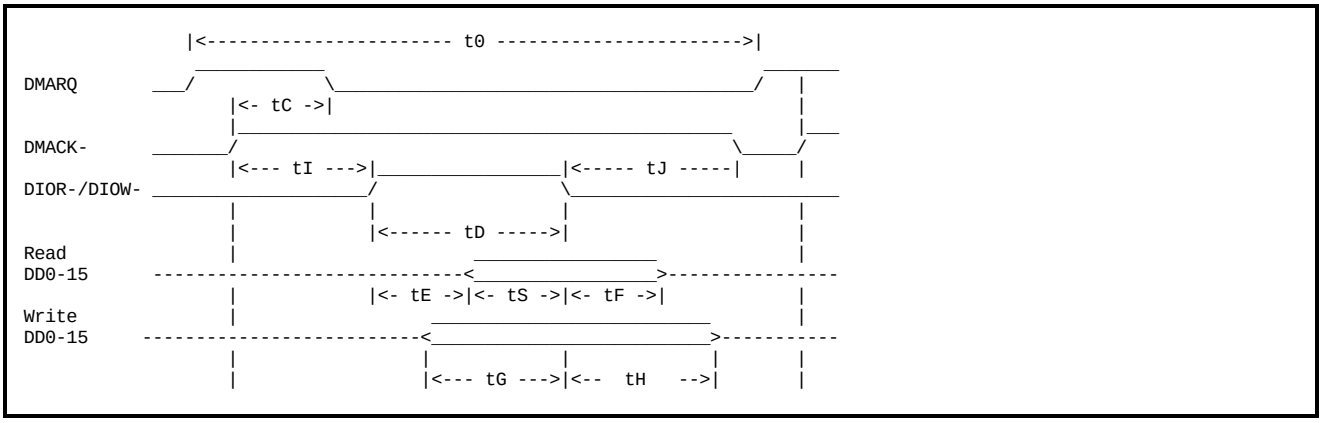
(2) This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

(3) The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

(4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. (See clause 5.2.11)

Figure 14 - PIO Data Transfer to/from Device (concluded)

9.4.2 10.4.2 Single word DMA data transfer



	Single word DMA timing parameters	Mode 0	Mode 1	Mode 2
t0	Cycle time (min)	960 ns	480 ns	240 ns
tC	DMACK to DMARQ delay (max)	200 ns	100 ns	80 ns
tD	DIOR-/DIOW-16-bit (min)	480 ns	240 ns	120 ns
tE	DIOR- data access (max)	250 ns	150 ns	60 ns
tF	DIOR- data hold (min)	5 ns	5 ns	5 ns
tG	DIOW- data setup (min)	250 ns	100 ns	35 ns
tH	DIOW- data hold (min)	50 ns	30 ns	20 ns
tI	DMACK to DIOR-/DIOW- setup (min)	0 ns	0 ns	0 ns
tJ	DIOR-/DIOW- to DMACK hold (min)	0 ns	0 ns	0 ns
tS	DIOR- setup (min)	tD-tE	tD-tE	tD-tE

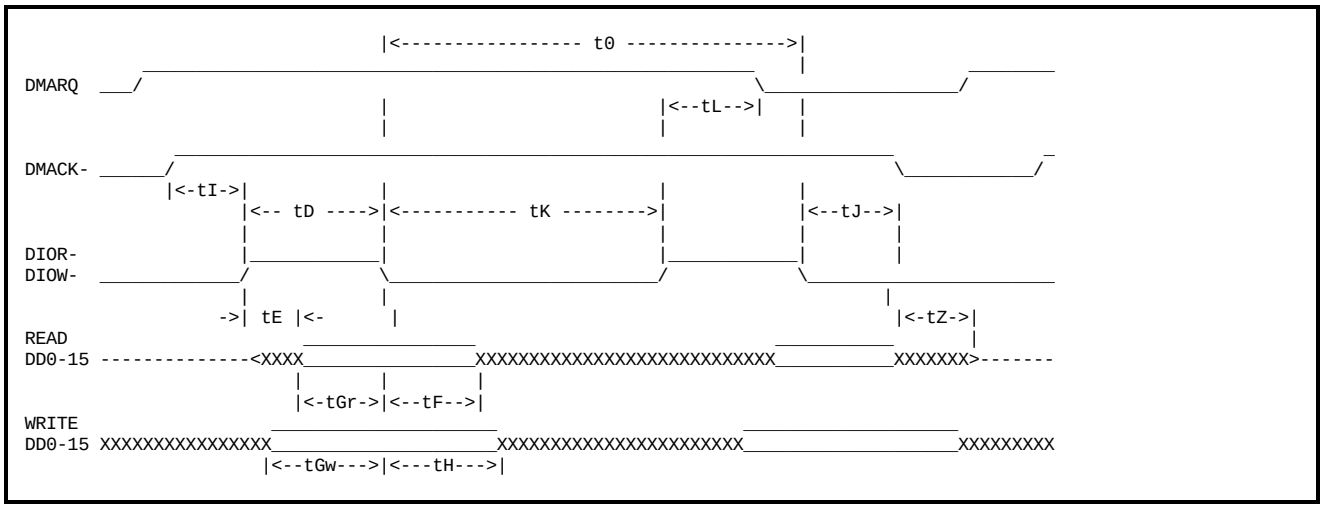
Figure 15 - Single word DMA data transfer

9.4.3 Multiword DMA data transfer

The timings associated with Multiword DMA Transfers are defined in figure 16.

For Multiword DMA modes 1 and above, the minimum value of t0 is specified by word 65 in the Identify Drive parameter list. The value in word 65 shall not be less than the value shown in the table below.

Devices reporting support for Multiword DMA Transfer Mode 2 shall also support Multiword DMA Transfer Mode 0 and 1 and shall power up with Mode 0 as the default Multiword DMA Mode.



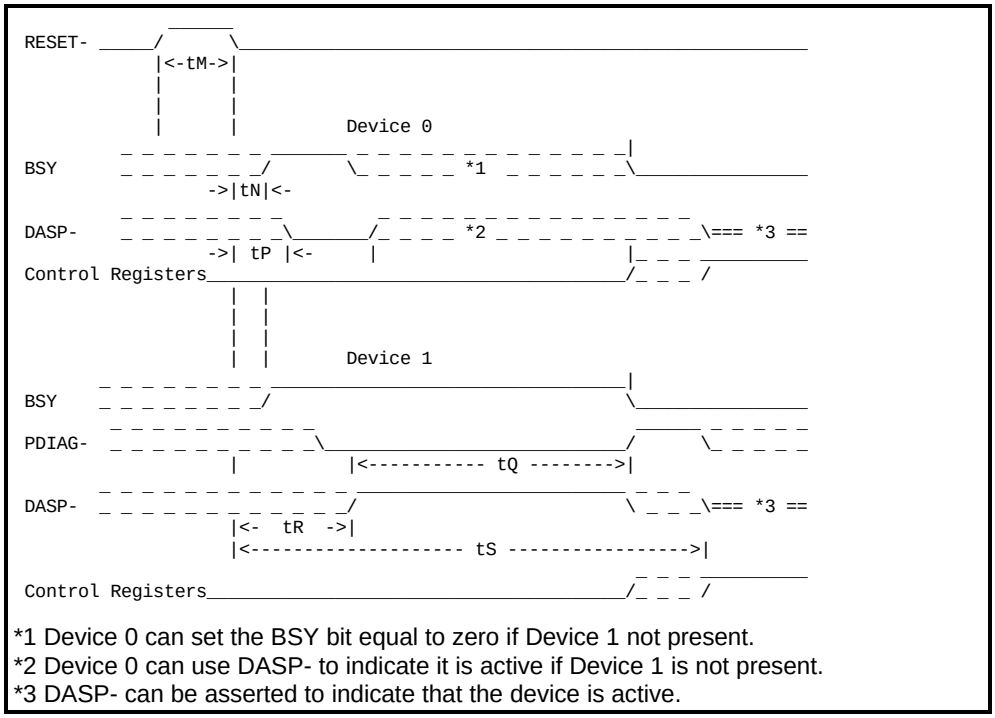
	Multiword DMA	Mode 0		Mode 1		Mode 2		Notes
	timing parameters	Min	Max	Min	Max	Min	Max	
t0	Cycletime	480 ns		150 ns		120 ns		(1)
tC	DMACKtoDMARQdelay		---		---		---	
tD	DIOR-/DIOW-16-bit	215 ns		80 ns		70 ns		(1)
tE	DIOR-dataaccess		150 ns		60 ns		---	
tF	DIOR-datahold	5 ns	(2)	5 ns		5 ns		
tG	DIOW-datasetup	100 ns		30 ns		20 ns	n/a	
tG	DIOW-datasetup	100 ns		30 ns		20 ns		
tH	DIOW-datahold	20 ns		15 ns		10 ns		
tI	DMACKtoDIOR-/DIOW-setup	0 ns		0 ns		0 ns		
tJ	DIOR-/DIOW-toDMACKhold	20 ns		5 ns		5 ns		
tKr	DIOR-negatedpulsewidth	50 ns		50 ns		25 ns		(1)
tKw	DIOW-negatedpulsewidth	215 ns		50 ns		25 ns		(1)
tLr	DIOR-toDMARQdelay		120 ns		40 ns		35 ns	
tLw	DIOW-toDMARQdelay		40 ns		40 ns		35 ns	
tZ	DMACK-totristate		20 ns		25 ns		25 ns	(2)

Notes -
(1) t0 is the minimum total cycle time, tD is the minimum command active time, and tK (tKr or tKw, as appropriate) is the minimum comman recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tK shall be met. The minimum total cycle time requirement, t0, is greater than the sum of tD and tK. This means a host implementation can lengthen either or both tD or tK to ensure that t0 is equal to the value reported in the devices identify drive data.. A device implementation shall support any legal host implementation.
(2) The original ATA standard defined a maximum value for tF. Meaning of this value was not clear. This parameter has been renamed to t and specifies the time from the negation edge of DMACK- to the time the Device Data signals are no longer driven by the device (tristate). The tZ parameter applies only at the end of a Multiword DMA cycle, i.e., when DMACK is negated. The device may actively drive the Devi Data signals, or may tristate the Device Data signals, while DMACK- is active from the first time that DIOR- is asserted until DMACK- is negated as long as tE and tF requirements are met.

Figure16 - Multiword DMA data transfer

9.5 Power-on and hard reset

Figure 17 shows the reset sequence.



*1 Device 0 can set the BSY bit equal to zero if Device 1 not present.
*2 Device 0 can use DASP- to indicate it is active if Device 1 is not present.
*3 DASP- can be asserted to indicate that the device is active.

Label	Units
tM (Min)	25 usec
tN (Max)	400 nsec
tP (Max)	1 msec
tQ (Max)	30 secs
tR Device 0 (Max)	450 msec
tR Device 1 (Max)	400 msec
tS (Max)	31 secs

Figure 17 - Reset sequence

Annex A
(informative)

Diagnostic and reset considerations from a device firmware standpoint

A.1 Power on and hardware reset (RESET-)

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity.

A.2 Software reset

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors, otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

A.3 Device diagnostic command

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command, otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

A.4 Truth table

In all the above cases: Power on, RESET-, software reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register is calculated as shown in the following table:

Device 1 present?	PDIAG- asserted?	Device 0 passed	Error register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Where x indicates the appropriate Diagnostic Code for the Power on, RESET-, software reset, or device diagnostics error.

A.5 Power on or hardware reset algorithm

NOTE 43 - In the following algorithms, the notation 1* refers to the Drive 1 status register copy that Drive 0 keeps when there is no Drive 1 present.

A.5.1 Algorithm for Device 0

1) Power on or hardware reset is detected by the device's hardware.
2) The hardware should automatically do the following within 400 ns of the negation of RESET-:
   a) Set up the hardware to report both Device 0 and Device 1* status registers.
   b) Set the BSY bit to one in the Device 0 Status register.
   c) Set the BSY bit to one in the Device 1* Status register.
3) The device shall determine if it is Device 0 or Device 1. This can be done at least two different ways: by jumper or by using the CSEL signal.
4) Set up PDIAG- and DASP:
   a) Set up PDIAG- as an input.
   b) Release DASP- and set up DASP- as an input.
   c) Monitor DASP- until DASP- is asserted by Device 1 or for 450 ms.
   d) If DASP- is asserted within 450 ms, store the fact that Device 1 is present and set up the hardware so it reports Device 0 status only.
   e) If DASP- is not asserted within 450 ms, store the fact that Device 1 is not present and set up the hardware so it reports both Device 0 and 1* status registers.
   f) Set up DASP- as an output.
   g) Assert DASP-.

   NOTE 42 - Steps 2-4 complete within 450 ms of the negation of RESET-.

5) Perform any remaining time critical hardware initialization including starting the spin up of the device if needed. Complete all the hardware initialization and diagnostic tests needed to get the device ready, including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
6) If Device 1 was detected in step 4:
   a) Monitor PDIAG- until PDIAG- is asserted by Device 1 or for 31 seconds.
   b) If PDIAG- is asserted within 31 seconds, set bit 7 equal to 0 in the Error register.
   c) If PDIAG- is not asserted within 31 seconds, set bit 7 equal to 1 in the Error register.
7) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register to 0000001b.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value other than 0000001b as described in Table 11.
8) Set the BSY bit of the Status register to zero and set Drive 1* Status register to 00H.

   NOTE 45 - Steps 2-8 complete within 31 seconds.

9) Finish initialization and optionally finish spin up.
10) Post Ready status:
   a) Set the DRDY bit to one and the DSC bit to one in the Status register.
   b) Negate DASP-.

A.5.2 Algorithm for Device 1

1) Power on or hardware reset is detected by the device's hardware.
2) The hardware should automatically do the following within 400 ns of the negation of RESET-:
   a) Set up the hardware to report both Device 0 and Device 1* status registers.
   b) Set the BSY bit to one in the Device 0 Status register.
   c) Set the BSY bit to one in the Device 1* Status register.
3) The device shall determine if it is Device 0 or Device 1. This can be done at least two different ways: by jumper or by using the CSEL signal.
4) Set up PDIAG- and DASP:
   a) Negate the PDIAG- signal.
   b) Set up PDIAG- as an output.
   c) Assert the DASP- signal.
   d) Set up DASP- as an output.
   e) Set up the hardware to report Device 1 status only.

NOTE 46 - Steps 2-4 complete within 400 ms of the negation of RESET-.

5) Perform any remaining time critical hardware initialization including starting the spin up of the device if needed. Complete all the hardware initialization and diagnostic tests needed to get the device ready, including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
6) Post Device 1's initialization and diagnostic results:
   a) If Device 1 completed all initialization and diagnostic without error, Set the Error register to 01h and assert PDIAG-.
   b) If Device 1 failed any initialization or diagnostics, set the Error register to a value other than 01h (see Table 11) and do not assert PDIAG-.
7) Set the status register to 00.

NOTE 47 - Steps 2-7 complete within 30 s.

8) Finish initialization and optionally finish spin up.
9) Post Ready status:
   a) Set the DRDY bit to one and, if spin up is also complete, the DSC bit to one in the Status register.
   b) Negate DASP-.
10) If not previously done, wait for spin up to complete and then set the DSC bit in the Status register to one.
11) Negate DASP- when the Command register is written or after 30 s.

A.6 Software Reset Algorithm

A.6.1 Algorithm for Device 0

1) SRST bit set to 1 is detected by the device's hardware.
2) The hardware should set the BSY bit in the Status register to one within 400 ns of the setting of SRST bit to one.

NOTE 46 - Steps 1-2 complete within 1 ms.

3) Assert DASP-.
4) Finish all the hardware initialization needed to place the device in reset including all diagnostics.
5) Wait for SRST bit to be set to 0.
6) Reset the Command Block registers:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
7) If Device 1 is present:
   a) Monitor PDIAG- for 31 seconds or until PDIAG- is asserted by Device 1.
   b) If PDIAG- is asserted within 31 seconds, set bit 7 to 0 in the Error register.
   c) If PDIAG- is not asserted within 31 seconds, set bit 7 to 1 in the Error register.
8) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 0000001b.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value other than 0000001b (see table 11).

NOTE 49 - Steps 6-8 complete within 31 s.

9) Set the DRDY bit in its Status register and set Drive 1* Status register to 00h.

A.6.2 Algorithm for Device 1

1) SRST bit equal to 1 is detected by the device's hardware.
2) The hardware should set 80h in the Status register within 400 ns.
3) Negate the PDIAG- signal.

NOTE 50 - Steps 1-3 complete within 1 ms.

4) Assert DASP-.
5) Finish all the hardware initialization needed to place the device in reset including all diagnostics.
6) Wait for SRST bit to be set to 0.
7) Reset the Command Block registers:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
8) Post Device 1's initialization and diagnostic results:

a) If Device 1 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 01h and assert PDIAG-.
b) If Device 1 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value other than 01h (see table 11) and does not assert PDIAG-.

NOTE 51 - Steps 7-9 complete within 30 s.

9) Set the DRDY bit in the Status register when ready to accept any command.

A.7 Diagnostic command algorithm

A.7.1 Algorithm for Device 0

1) The EXECUTE DEVICE DIAGNOSTIC command is received.
2) The hardware should set 80h in the Status register within 400 ns.
3) The hardware should set 80h in the Device 1* Status register.

NOTE 52 - Steps 1-3 complete within 1 ms.

4) Assert DASP-.
5) Perform all the device diagnostics and note the results.
6) Finish all the hardware initialization needed to get the device ready to receive any type of command from the host including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
7) If Device 1 is present:
   a) Monitor PDIAG- until PDIAG- is asserted by Device 1 or for 6 s.
   b) If PDIAG- is asserted within 6 s, set bit 7 to 0 in the Error register.
   c) If PDIAG- is not asserted within 6 s, set bit 7 to 1 in the Error register.
8) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 0000001b.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value other than 0000001b (see Table 11).

NOTE 53 - Steps 2-8 complete within 6 s.

9) Set the Status register to 50h and set Drive 1* Status register to 00h.
10) Assert INTRQ.

A.7.2 Algorithm for Device 1

1) The EXECUTE DEVICE DIAGNOSTIC command is received.
2) The hardware should set 80h in the Status register within 400 ns.
3) Negate the PDIAG- signal.

NOTE 54 - Steps 1-3 complete within 1 ms.

4) Assert DASP-.
5) Perform all the device diagnostics and note the results.
6) Finish all the hardware initialization needed to get the device ready to receive any type of command from the host including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
7) Post Device 1's initialization and diagnostic results:
   a) If Device 1 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 1 and assert PDIAG-.
   b) If Device 1 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure and do not assert PDIAG-.

   NOTE 55 - Steps 2-7 complete within 5 s.

8) Set the DRDY bit in the Status register when ready to accept any command.

Annex B.
(informative)

44-Pin Small form factor connector

This annex describes a connector alternative often used for 2 1/2" or smaller devices. This alternative was developed by the Small Form Factor (SFF) Committee, an industry ad hoc group.

In an effort to broaden the applications for small form factor devices, a group of companies representing system integrators, device suppliers, and component suppliers decided to address the issues involved.

A primary purpose of the SFF Committee was to define the external dimensions of small form factor devices so that products from different vendors could be used in the same mounting configurations.

The restricted area, and the mating of devices directly to a motherboard required that the number of connectors be reduced, which caused the assignment of additional pins for power. Power is provided to the devices on the same connector as used for the signals, and addresses are set by the receptacle into which the devices are plugged.

The 50-pin connector that has been widely adopted across industry for SFF devices is a low density 2mm connector which has no shroud on the plug which is mounted on the device. A number of suppliers provide intermatable components. The following information has been provided to assist users in specifying components used in an implementation.

Signals Connector Plug	DuPont 86451 or equivalent
Signals Connector Receptacle	DuPont 86455 or equivalent

B.1 44-pin signal assignments

The signals assigned for 44-pin applications are described in table B.1. Although there are 50 pins in the plug, a 44 pin mating receptacle may be used(the removal of pins E and F provides room for the wall of the receptacle).

Some devices may utilize pins A, B, C and D for option selection via physical jumpers. Such implementations may require use of the 44 pin receptacles.

B.2 44-pin signal assignments for ATA

The first four pins of the connector plug located on the device are not to be connected to the host, as they are reserved for manufacturer's use. Pins E, F, and 20 are keys, and are removed.

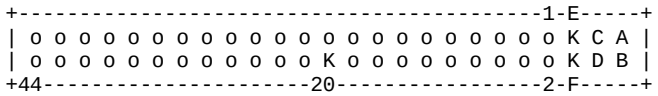


Table B.1 - Signal Assignments for 44-Pin ATA

Signal name	Connector contact	Conductor	Connector contact	Signal name
Vendor specific	A		B	Vendor specific
Vendor specific	C		D	Vendor specific
(keypin)	E		F	(keypin)
RESET-	1	1 | 2	2	Ground
DD7	3	3 | 4	4	DD8
DD6	5	5 | 6	6	DD9
DD5	7	7 | 8	8	DD10
DD4	9	9 | 10	10	DD11
DD3	11	11 | 12	12	DD12
DD2	13	13 | 14	14	DD13
DD1	15	15 | 16	16	DD14
DD0	17	17 | 18	18	DD15
Ground	19	19 | 20	20	(keypin)
DMARQ	21	21 | 22	22	Ground
DIOW-	23	23 | 24	24	Ground
DIOR-	25	25 | 26	26	Ground
IORDY	27	27 | 28	28	SPSYNC:CSEL
DMACK-	29	29 | 30	30	Ground
INTRQ	31	31 | 32	32	IOCS16-
DA1	33	33 | 34	34	PDIAG-
DAO	35	35 | 36	36	DA2
CS0-	37	37 | 38	38	CS1-
DASP-	39	39 | 40	40	Ground
+5v (Logic)	41	41 | 42	42	+5V (Motor)*
*Ground (Return)	43	43 | 44	44	TYPE - (0=ATA)*
* Pins which are additional to those of the 40-pin cable.				

Annex C.
(informative)

68-Pin Small Form Factor Connector

C.1 Overview

This annex defines the pinouts used for the 68-pin alternative connector for the AT Attachment Interface. This connector is the same as the one defined by PCMCIA. This annex defines a pinout alternative that allows a device to function as an AT Attachment Interface compliant device, while also allowing the device to be compliant with PC Card-ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin ATA or PCMCIA.

To simplify the implementation of dual-interface devices, the 68-pin AT Attachment Interface maintains commonality with as many PC Card-ATA signals as possible, while supporting full command and signal compliance with the ATA standard.

The 68-pin ATA pinout does not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the reset signal between the ATA and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

C.2 Signals

This Specification relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card-ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

Unless otherwise noted, all signals and registers with the same names as ATA signals and registers have the same meaning as defined in X3.221-199x, which defines the protocol by which commands are directed to the storage device.

C.3 Signal Descriptions

Any signals not defined below are as described in the ATA, PCMCIA, or the PC Card-ATA documents.

Table C.1 shows the ATA signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table C.1 - Signal Assignments for 68-Pin ATA

Pin	Signal	Hst|Dir|Dev	PCMCIA	Pin	Signal	|Hst|Dir|Dev	PCMCIA
1	Ground	x ---> x	Ground	35	Ground	x ---> x	Ground
2	DD3	x <---> x	D3	36	CD1-	x <--- x	CD1-
3	DD4	x <---> x	D4	37	DD11	x <---> x	D11
4	DD5	x <---> x	D5	38	DD12	x <---> x	D12
5	DD6	x <---> x	D6	39	DD13	x <---> x	D13
6	DD7	x <---> x	D7	40	DD14	x <---> x	D14
7	CS0-	x ---> x	CE1-	41	DD15	x <---> x	D15
8		---> i	A10	42	CS1-	x --->x*1	CE2-
9	SELATA-	x ---> x	OE-	43		<--- i	VS1-
10				44	DIOR-	x ---> x	IORD-
11	CS1-	x --->x[1]	A9	45	DIOW-	x ---> x	IOWR-
12		---> i	A8	46			
13				47			
14				48			
15	---> i		WE-	49			
16	INTRQ	x <--- x	READY/IREQ-	50			
17	VCC	x ---> x	VCC	51	VCC	x ---> x	VCC
18				52			
19				53			
20				54			
21				55	M/S-	x --->x*2	
22		---> i	A7	56	CSEL		x --->x*2
23		---> i	A6	57		<--- i	VS2-
24		---> i	A5	58	RESET-	x ---> x	RESET
25		---> i	A4	59	IORDY	o <--- x*3	WAIT-
26		---> i	A3	60	DMARQ	o <--- x*3	INPACK-
27	DA2	x ---> x	A2	61	DMACK-	o ---> o	REG-
28	DA1	x ---> x	A1	62	DASP-	x <---> x	BVD2/SPKR-
29	DA0	x ---> x	A0	63	PDIAG-	x <---> x	BVD1/STSCHG-
30	DD0	x <---> x	D0	64	DD8	x <---> x	D8
31	DD1	x <---> x	D1	65	DD9	x <---> x	D9
32	DD2	x <---> x	D2	66	DD10	x <---> x	D10
33	IOCS16-	x <--- x	WP/IOIS16-	67	CD2-	x <--- x	CD2-
34	Ground	x ---> x	Ground	68	Ground	x ---> x	Ground

NOTES:
*1 The device shall support only one CS1- signal pin.
*2 The device shall support either M/S- or CSEL but not both.
*3 The device shall hold this signal negated if it does not support the function.

The Dir column indicates the direction of the signal between host and device. An x in the Hst column means this signal shall be supported by the Host. An x in the Dev column means this signal shall be supported by the device. An i in the Dev column means this signal shall be ignored by the device while in 68-pin ATA mode. An o means this signal is Optional. If there is nothing in Dev column for a pin location, then no connection should be made to that pin.

C.3.1 CD1- (Card Detect 1)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

C.3.2 CD2- (Card Detect 2)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

C.3.3 CS1- (Device chip Select 1)

Hosts shall provide CS1- on both the pins identified in table C.1.

Devices are required to recognize only one of the two pins as CS1-.

C.3.4 DMACK- (DMA Acknowledge)

This signal is optional for hosts and devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

C.3.5 DMARQ (DMA Request)

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

C.3.6 IORDY (I/O Channel Ready)

This signal is optional for hosts.

C.3.7 M/S- (Master/Slave)

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying VCC to the connector.

C.3.8 SELATA- (Select 68-pin ATA)

This pin is used by the host to select which mode to use, PC Card-ATA mode or the 68-pin ATA mode. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector, and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a Hard or Soft Reset. The device shall ignore all interface signals for 19 ms after the host supplies Vcc within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card-ATA mode or not respond to further inputs from the host.

C.4 Removability considerations

This standard supports the removability of devices that use the ATA protocol. As removability is a new consideration for ATA devices, several issues need to be considered with regard to the insertion or removal of devices.

C.4.1 Device recommendations

The following are recommendations to device implementors:

– CS0-, CS1-, RESET- and SELATA- should be negated on the device to prevent false selection during hot insertion.

– Ignore all interface signals except SELATA- until 19 ms after the host supplies VCC within the device's voltage tolerance. This time is necessary to de-bounce the device's power on reset sequence. Once in the 68-pin ATA mode, if SELATA- is ever negated following the 19 ms de-bounce delay time, the device should disable itself until VCC is removed.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register should be used to prevent unexpected removal of the device or media.

C.4.2 Host recommendations

The following are recommendations to host implementors:

– Connector pin sequencing should protect the device by making contact to ground before any other signal in the system.

– SELATA- should be asserted at all times.

– All devices should be reset and reconfigured to the same base address each time a device at that address is inserted or removed.

– The removal or insertion of a device at the same address should be detected so as to prevent the corruption of a command.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register should be used to prevent unexpected removal of the device or media.

Annex D.
(informative)

Identify device data for ATA devices below 8 GB

D.1 Definitions and background information

The following abbreviations are used in this annex:

- 528 MB is used to describe a drive that has 1,032,192 sectors or 528,482,304 bytes.

- 8 GB is used to describe a drive that has 16,515,072 sectors or 8,455,716,864 bytes.

The original IBM PC BIOS (Basic Input/Output System) imposed several restrictions on the support of disk drives, and these have been incorporated into many higher level software products. One such restriction limits the capacity of a hard disk drive. Most BIOS software cannot support a disk drive with more than 1,024 cylinders, 16 heads and 63 sectors per track. The maximum addressable capacity of an ATA disk drive under this scheme is 528 MB.

There is growing support of auto-configuration for disk drives on PC systems. The auto-configuration capability usually resides in the BIOS and uses the Identify Drive command data to configure an ATA disk drive.

This annex defines rules for the Identify Drive data of all capacity ATA disk drives and allows BIOS support of ATA drives up to 8 GB using Cylinder/Head/Sector (CHS) addressing.

This specification defines information that newer BIOSs and system software can use to determine the true size of a disk drive and access the full capacity of the drive.

D.2 Cylinder, head and sector addressing

BIOSs and other software that operate an ATA disk drive in CHS (Cylinder, Head and Sector) addressing mode use Identify Drive data words 1, 3, 6 and words 53-58 to ascertain the appropriate translation mode to use and determine the capacity of an ATA disk drive.

Maximum compatibility is achieved if the following rules are obeyed. These rules limit the values placed into words 1, 3, 6, and 53-58. The rules specified here for CHS addressing apply to drives up to 8 GB.

D.2.1 Word 1

For drives less than or equal to 528 MB, Identify Data word 1 (Default Cylinders) shall not specify a value greater than 1,024.

If a drive is greater than 528 MB but less than or equal to 8 GB, the maximum value that shall be placed into this word is determined by the value in Word 3 as shown in the following table.

Value in Word 3	Maximum value in Word 1
1 1h	65,535 FFFFh
2 2h	65,535 FFFFh
3 3h	65,535 FFFFh
4 4h	65,535 FFFFh
5 5h	32,767 7FFFh
6 6h	32,767 7FFFh
7 7h	32,767 7FFFh
8 8h	32,767 7FFFh
9 9h	16,383 3FFFh
10 Ah	16,383 3FFFh
11 Bh	16,383 3FFFh
12 Ch	16,383 3FFFh
13 Dh	16,383 3FFFh
14 Eh	16,383 3FFFh
15 Fh	16,383 3FFFh
16 10h	16,383 3FFFh

The value in this word shall not change.

D.2.2 Word 3

Identify Data word 3 (Default Heads) shall not specify a value greater than 16.

The value in this word shall not change.

D.2.3 Word 6

For drives of 8 GB or less, Identify Data word 6 (Default Sectors) shall not specify a value greater than 63.

The value in this word shall not change.

D.2.4 Use of words 53 through 58

ATA drives that are over 528 MB shall implement words 53-58. Drives not over 528 MB may also implement these words. These words define the addressing for all sectors accessible in CHS mode.

D.2.5 Word 53

Identify Data word 53 bit 0 shall be set to 1 at all times that the drive is in a valid translation mode. Some drives may have translation modes that cannot be supported. An attempt to put a drive into one of these unsupported modes shall cause word 53 bit 0 to be set to 0 with words 54-58 cleared to zero until a valid translation mode is established.

D.2.6 Word 54

Identify Data word 54 (Current Cylinders) shall specify the number of full logical cylinders that can be accessed in the current translation mode. If an Initialize Drive Parameters command has not been executed, the contents of this word shall be the same as word 1. If an Initialize Drive Parameters command has been executed, this word is the integer result of dividing the total number of user sectors (this value may be in words 60-61) by the number of sectors per logical cylinder ([word55] x [word56]), but shall not be a value greater than 65,535.

D.2.7 Word 55

Identify Data word 55 (Current Heads) is the number of heads specified by the last Initialize Drive Parameters command. This word may contain a value of between 1 and 16. If an Initialize Drive Parameters command has not been executed, the contents of this word shall be the same as word 3.

D.2.8 Word 56

Identify Data word 56 (Current Sectors) is the number of sectors specified by the last Initialize Drive Parameters command. This word may contain a value of between 1 and 255. If an Initialize Drive Parameters command has not been executed, the contents of this word shall be the same as word 6.

D.2.9 Words 57-58

Identify Data words 57-58 contain a 32-bit value that shall be equal to [word54] multi [word55] multi [word56]. If words 60-61, LBA sectors, are not zero, words 57-58 shall be less than or equal to the value in words 60-61 at all times.

D.3 Logical block addressing

It is recommended that ATA drives over 528 MB support Logical Block Addressing (LBA).

D.3.11 Words 60-61

Identify Data words 60-61 shall specify the total number of user sectors available in LBA mode at all times. This value shall be equal to or greater than the value in words 57-58 at all times. The contents of these words shall not change.

D.3.2 Orphan Sectors

The sectors, if any, between the last sector addressable in CHS mode and the last sector addressable in LBA mode are known as "orphan" sectors. A drive may or may not allow access to these sectors in CHS addressing mode.

The values in words 1, 3, and 6 should be selected such that the number of orphan sectors is minimized. Normally, the number of orphan sectors should not exceed ([word55] multi [word56] - 1). However, the host system can create conditions where there are a larger number of orphans sectors by issuing the Initialize Drive Parameters command with values other than the values in words 3 and 6.

Annex E.
(informative)

ATA command set summary

The following two tables are provided to facilitate the understanding of the ATA command set. Table 18 provide information on which command codes are currently defined. Table 19 provides a list of all of the ATA commands in order of command code.

Table E.1 - Command Matrix

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
1x	C	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
2x	C	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R
3x	C	C	C	C	R	R	R	R	R	R	R	R	C	R	R	R
4x	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R
5x	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
6x	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
7x	C	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8x	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
9x	C	C	C	R	C	C	C	C	C	C	V	R	R	R	R	R
Ax	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bx	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Cx	V	V	V	V	C	C	C	R	C	C	C	C	R	R	R	R
Dx	R	R	R	R	R	R	R	R	R	R	R	C	C	C	C	C
Ex	C	C	C	C	C	C	C	R	C	C	R	R	C	C	R	C
Fx	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

NOTES:
* - Values 11h through 1Fh are identical to command 10h
Values 71h through 7Fh are identical to command 70h
C - a unique command
R - Reserved, undefined in current specifications
V - Vender Unique commands

Table E.2 - Commands Sorted By Command Value

Command Name	Command Code
NOP	00h
Reserved	01h-0Fh
RECALIBRATE	1xh
READ SECTOR(S) (w/retry)	20h
READ SECTOR(S) (w/o retry)	21h
READ LONG (w/retry)	22h
READ LONG (w/o retry)	23h
Reserved	24h-2Fh
WRITE SECTOR(S) (w/retry)	30h
WRITE SECTOR(S) (w/o retry)	31h
WRITE LONG (w/retry)	32h
WRITE LONG (w/o retry)	33h
Reserved	34h-3Bh
WRITE VERIFY	3Ch
Reserved	3Dh-3Fh
READ VERIFY SECTOR(S) (w/retry)	40h
READ VERIFY SECTOR(S) (w/o retry)	41h
Reserved	42h-4Fh
FORMAT TRACK	50h
Reserved	51h-5Fh
Reserved	60h-6Fh
SEEK	7xh
Vendor specific	8xh
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
Reserved	93h
STANDBY IMMEDIATE	94h*E0h*
IDLE IMMEDIATE	95h*E1h*
STANDBY	96h*E2h*
IDLE	97h*E3h*
CHECK POWER MODE	98h*E5h*
SLEEP	99h*E6h*
Vendor specific	9Ah
Reserved	9Bh-9Fh
Reserved	A0h-AFh
Reserved	B0h-BFh
Vendor specific	C0-C3h
Some commands have two command codes and appear in this table twice, once for each command code.	

Table E.2- Commands Sorted By Command Value (concluded)

Command Name	CommandCode
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
Reserved	C7h
READ DMA (w/retry)	C8h
READ DMA (w/o retry)	C9h
WRITE DMA (w/retry)	CAh
WRITE DMA (w/o retry)	CBh
Reserved	CCh-CFh
Reserved	D0h-DAh
ACKNOWLEDGE MEDIA CHANGE	DBh
BOOT - POST-BOOT	DCh
BOOT - PRE-BOOT	DDh
DOOR LOCK	DEh
DOOR UNLOCK	DFh
STANDBY IMMEDIATE	*94h*E0h
IDLE IMMEDIATE	*95h*E1h
STANDBY	*96h*E2h
IDLE	*97h*E3h
READ BUFFER	E4h
CHECK POWER MODE	*98h*E5h
SLEEP	*99h*E6h
Reserved	E7h
WRITE BUFFER	E8h
WRITE SAME	E9h
Reserved	EAh-EBh
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
Reserved	EEh
SET FEATURES	EFh
Vendor specific	F0h-FFh
Some commands have two command codes and appear in this table twice, once for each command code.	