

Features

- Supports the SignalTap™ embedded logic analyzer in the Quartus™ software
- Allows PC and UNIX users to perform the following functions:
 - Configuring APEX™ 20K, FLEX® 10K, FLEX 8000, and FLEX 6000 devices
 - In-system programming for MAX® 9000, MAX 7000S, and MAX 7000A devices
- Supports operation with V_{CC} at 5.0 V, 3.3 V, or 2.5 V
- Provides a fast, low-cost method for in-system programming
- Downloads data from the Quartus development software and the MAX+PLUS® II software versions 9.3 and higher
- Interfaces with an RS-232 serial or universal serial bus (USB) port
- Uses a 10-pin circuit board connector, which is compatible with the BitBlaster™ serial download cable and the ByteBlasterMV™ parallel port download cable

Functional Description

The MasterBlaster™ communications cable (ordering code: PL-MASTERBLASTER) is a standard PC serial or USB port hardware interface. This cable downloads configuration data to APEX 20K, FLEX 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, and FLEX 6000 devices, as well as programming data to MAX 9000, MAX 7000S, and MAX 7000A (including MAX 7000AE) devices. Because design changes are downloaded directly to the device, prototyping is easy and multiple design iterations can be accomplished in quick succession. The MasterBlaster cable also supports in-circuit debugging with the SignalTap embedded logic analyzer in APEX 20K devices. See [Figure 1](#).

Figure 1. MasterBlaster Serial/USB Communications Cable



Download Modes

The MasterBlaster cable provides two download modes:

- Passive serial (PS) mode—Used for configuring APEX 20K and FLEX devices
- JTAG mode—Industry-standard IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface for programming JTAG-capable MAX and serial configuration devices (i.e., EPC2) in-system or configuring APEX 20K and FLEX devices

SignalTap Logic Analysis

The SignalTap megafunction is an embedded logic analyzer, capturing device data at specified trigger points and storing the data in APEX 20K embedded system blocks (ESBs). This data is then sent to the JTAG IEEE Std. 1149.1 port of an APEX 20K device, uploaded through the MasterBlaster communications cable, and displayed in the Quartus Waveform Editor.



For more information on the SignalTap megafunction, see the *SignalTap Embedded Logic Analyzer Megafunction Data Sheet*.

MasterBlaster Connections

The MasterBlaster cable connects to a computer through a serial or USB port, and connects to the circuit board through a standard 10-pin female connector. Data is downloaded from the serial or USB port through the MasterBlaster cable to the circuit board through the connections discussed in this section.

Header & Plug Connections

The 9-pin male D-type connector connects to an RS-232 port with a standard serial cable. See [Table 1](#).



The USB connector can be used with any standard USB cable.

Table 1. MasterBlaster 9-Pin Serial D-Type Connector Pin-Outs

Pin	Signal Name	Description
2	rx	Receive data
3	tx	Transmit data
4	dtr	Data terminal ready
5	GND	Signal ground
6	dsr	Data set ready
7	rts	Request to send
8	cts	Clear to send



For more information on 9-pin versus 25-pin serial connectors, search for “9-pin or 25-pin serial connectors” in the Altera technical support (AtlasSM) database at <http://www.altera.com>.

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device(s). [Figure 2](#) shows the dimensions of the female plug.

Figure 2. MasterBlaster 10-Pin Female Plug Dimensions

Dimensions are shown in inches. The spacing between pin centers is 0.1 inches.

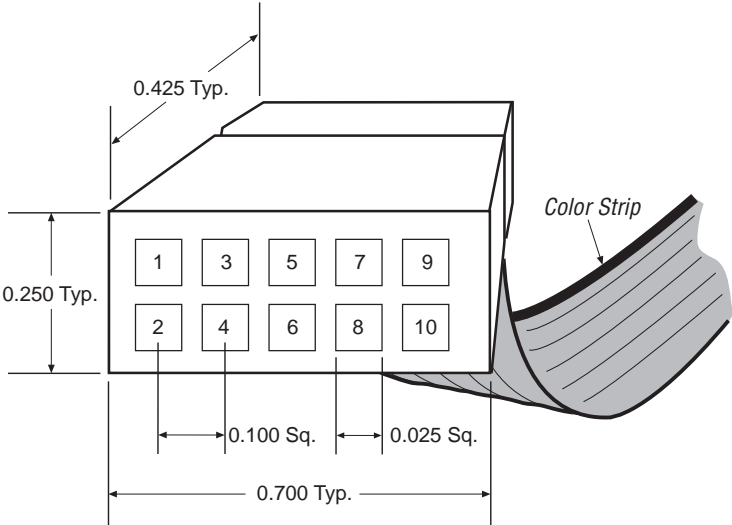


Table 2 identifies the 10-pin female plug’s pin names for the corresponding download mode.

Table 2. MasterBlaster Female Plug’s Pin Names & Download Modes				
Pin	PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description
1	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration control	TDO	Data from device
4	VCC	Power supply	VCC	Power supply
5	nCONFIG	Configuration control	TMS	JTAG state machine control
6	VIO	Reference voltage for MasterBlaster output driver	VIO	Reference voltage for MasterBlaster output driver
7	nSTATUS	Configuration status	—	No connect
8	—	No connect	—	No connect
9	DATA0	Data to device	TDI	Data to device
10	GND	Signal ground	GND	Signal ground

Powering the MasterBlaster Cable

Older download cables received their power from the circuit board only. In contrast, the MasterBlaster cable can receive power from the following sources:

- 5.0-V or 3.3-V circuit boards
- DC power supply
- 5.0 V from the USB cable

When 5.0-V or 3.3-V power is not available on the circuit board, the MasterBlaster cable can be powered by either DC power or the USB cable.



For the MasterBlaster cable's output drivers, connect the circuit board's V_{CC} and ground to the MasterBlaster cable's V_{CC} , V_{IO} , and GND pins.

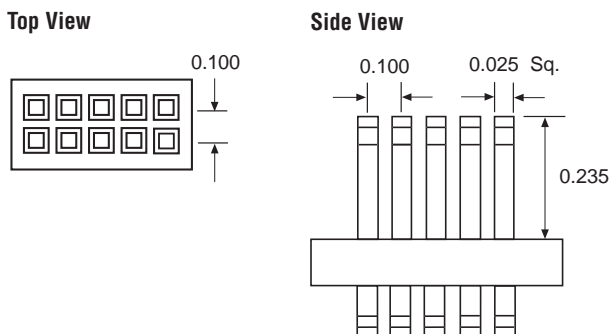
Circuit Board Header Connection

The MasterBlaster 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins, which are connected to the device's programming or configuration pins.

Figure 3 shows the dimensions of a typical 10-pin male header.

Figure 3. 10-Pin Male Header Dimensions

Dimensions are shown in inches.



Operating Conditions

Tables 3 through 5 summarize the absolute maximum ratings, recommended operating conditions, and DC operating conditions for the MasterBlaster cable.

Table 3. MasterBlaster Cable Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	-0.5	7.0	V
V_I	DC input voltage	With respect to ground	-0.5	7.0	V

Table 4. MasterBlaster Cable Recommended Operating Conditions *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Board header supply voltage, 5.0-V operation		4.5	5.5	V
	Board header supply voltage, 3.3-V operation		3.0	3.6	V

Table 5. MasterBlaster Cable DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	$V_{CC} = V_{IO}$	$0.25 \times V_{IO} + 0.3 \text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = V_{IO}$		$0.25 \times V_{IO}$	V
V_{OH}	5.0-V high-level TTL output voltage	TTL load. $V_{CC} = V_{IO} = 4.5 \text{ V}$, $I_{OH} = 8 \text{ mA}$	3.2		V
	3.3-V high-level TTL output voltage	TTL load. $V_{CC} = V_{IO} = 3.0 \text{ V}$, $I_{OH} = 4 \text{ mA}$	2.4		V
	5.0-V high-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 4.5 \text{ V}$, $I_{OH} = 0.1 \text{ mA}$	4.0		V
	3.3-V high-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 3.0 \text{ V}$, $I_{OH} = 0.1 \text{ mA}$	2.7		V
	2.5-V high-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 2.3 \text{ V}$, $I_{OH} = 0.1 \text{ mA}$	2.0		V
V_{OL}	5.0-V low-level TTL output voltage	TTL load. $V_{CC} = V_{IO} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$		0.4	V
	3.3-V low-level TTL output voltage	TTL load. $V_{CC} = V_{IO} = 3.0 \text{ V}$, $I_{OL} = 4 \text{ mA}$		0.4	V
	5.0-V low-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 4.5 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$		0.1	V
	3.3-V low-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 3.0 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$		0.1	V
	2.5-V low-level CMOS output voltage	CMOS load. $V_{CC} = V_{IO} = 2.3 \text{ V}$, $I_{OL} = 0.1 \text{ mA}$		0.1	V
P	Operating power			1.0	W

Notes to tables:

- (1) The DC adapter supply voltage has a minimum value of 3.0 V, a maximum value of 16.0 V, and a power consumption of 1 W (V_{CC} can be at 5.0 V, 3.3 V, or 2.5 V).
- (2) The 5.0-V USB cable supply voltage has a minimum value of 4.5 V and a maximum value of 5.5 V (V_{CC} can be at 5.0 V, 3.3 V, or 2.5 V).

References

For more information on configuration and in-system programmability (ISP), see the following sources:

- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Application Note 95 (In-System Programmability in MAX Devices)*
- *Application Note 100 (In-System Programmability Guidelines)*
- *APEX 20K Programmable Logic Device Family Data Sheet*
- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *FLEX 6000 Programmable Logic Device Family Data Sheet*
- *MAX 9000 Programmable Logic Device Family Data Sheet*
- *MAX 7000 Programmable Logic Device Family Data Sheet*
- *MAX 7000A Programmable Logic Device Family Data Sheet*
- Search for “Configuring a Single Device with the BitBlaster, ByteBlaster, or FLEX Download Cable,” “Setting Up Multi-Device JTAG Chains,” “Configuring Multiple Devices in a JTAG Chain with the BitBlaster or ByteBlasterMV,” and “Programming Multiple Devices in a JTAG Chain with the BitBlaster or ByteBlasterMV” in MAX+PLUS II Help.
- The *Quartus Installation & Licensing* manual for information on how to install the MasterBlaster cable.



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