1999
Intellectual Property Catalog

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Intellectual Property
Catalog

I.S. EN ISO 9001

About this Catalog

September 1999

IP Catalog Contents

This catalog provides information on cores, development boards, and design services from Altera and its partners. The information in this catalog is current as of the printing date, but megafunction specifications and availability are subject to change. For the most current information, refer to the Altera® world-wide web site at **http://www.altera.com/ip-megastore**.

Each megafunction description includes a list of key features, a functional description with information on applicable standards compliance, a block diagram, and a table with utilization and performance specifications. Megafunctions are grouped into the following functional areas:

- Digital Signal Processing (DSP)
- Communications
- PCI & Other Bus Interfaces
- Processor and Peripheral
- Development Boards

Each AMPP partner profile contains contact, background, and product information on the partner company. The partner profile also includes a list of available megafunctions and a description of additional services.

How to Contact Altera

For additional information about Altera products, consult the sources shown in Table 1. For information on how to contact an Altera sales office, see "Altera Sales Offices" in this catalog.

Table 1. Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 544-7850
	Altera Literature Services	(888) 3-ALTERA lit_req@altera.com	(888) 3-ALTERA lit_req@altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-8186	(408) 544-7606
Technical Support	Telephone Hotline (6:00 a.m. to 6:00 p.m. Pacific Time)	(800) 800-EPLD	(408) 544-7000
	Fax	(408) 544-6401	(408) 544-6401
	Electronic Mail	support@altera.com	support@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
General Product Information	Telephone	(408) 544-7104	(408) 544-7104
	World-Wide Web	http://www.altera.com	http://www.altera.com

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Introduction

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Overview

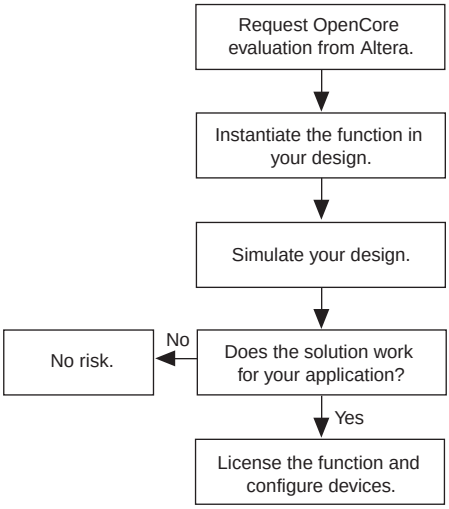
Time-to-market, feature enhancement, and cost reduction have forced the system design community to seek out more efficient design techniques. Their pursuits have produced a breakthrough in traditional design methods by introducing the concept of system level integration. Altera's high-density programmable logic devices (PLDs) offer designers system-on-a-programmable-chip™ (SOPC) hardware solutions for their development activities.

SOPC solutions replace standard components on a board with several functions on a single PLD. These functions are called megafunctions, cores, or intellectual property (IP). Developing a system-on-a-chip differs from traditional hardware design because it requires the presence of a broad spectrum of megafunctions, new tools focused on integration techniques, and design resources capable of implementing these designs with a systems-level perspective.

To help customers attain the benefits of system-level integration, Altera has a portfolio of IP products and resources to facilitate the transition to SOPC solutions. Altera's portfolio includes megafunctions, design resources, development boards, and integration tools. This catalog describes the tools and resources that Altera and its partners provide for designers.

Figure 1 shows the integration flow for megafunctions.

Figure 1. Megafunctions Development Process



Note:
(1) Contact Altera for more information on MegaCore functions; Contact AMPP partners for more information on AMPP megafunctions.

Megafunction Benefits

The following sections describe the faster time-to-market, cost reduction, and increased productivity that megafunctions provide.

Time-to-market

Megafunctions reduce time-to-market by eliminating the need to design standardized functions from scratch. Instead, the designer focuses on those system functions which offer significant differentiation and uses megafunctions to fill in the remaining elements of the target specification.

Cost Reduction

Megafunctions reduce the cost of the target system by eliminating standard components through system-level integration. By integrating several megafunctions onto a single PLD, the total number of components for the complete system is reduced.

Productivity Increase

Because megafunction designs are re-usable, they can be leveraged to satisfy multiple products' specifications. Leveraging megafunction designs earns a return on the initial investment over several products.

AMPP Program

The Altera Megafunction Partners Program (AMPP[SM]), an alliance between Altera and developers of synthesizable megafunctions, brings the advantages of design re-use to Altera PLD users. Through this alliance, AMPP vendors develop megafunctions that are optimized for Altera devices.

Premier AMPP Program

The Premier AMPP Program recognizes the top performing participants in the AMPP program based on feedback from customers. The current Premier AMPP partner is PLD Applications.

MegaCore Functions

MegaCore™ functions are developed, pre-tested, documented, and licensed directly from Altera. These functions are optimized for a specific Altera device architecture, allowing user-specified performance goals to be met. Altera MegaCore functions aid in critical design implementation and help reduce design effort and development cycles.

The Altera Consultants Alliance Program (ACAP) is the first global program of complex programmable logic device (CPLD) consultants. Founded in 1997, ACAP trains and certifies well-established consulting and design organizations around the world. The objective of the program is to help customers achieve design goals by ensuring the presence of third-party engineering resources, which are experienced with Altera products. A listing of ACAP consultants can be found in each chapter of this catalog, as well as an alphabetical listing on page 375.

Risk-Free Evaluation with OpenCore Feature

The OpenCore™ feature allows designers to evaluate megafunctions prior to licensing. Supported by the Quartus™ and MAX+PLUS® II development systems, the OpenCore feature allows designers to compile a megafunction, but prevents the designer from generating programming or configuration files.

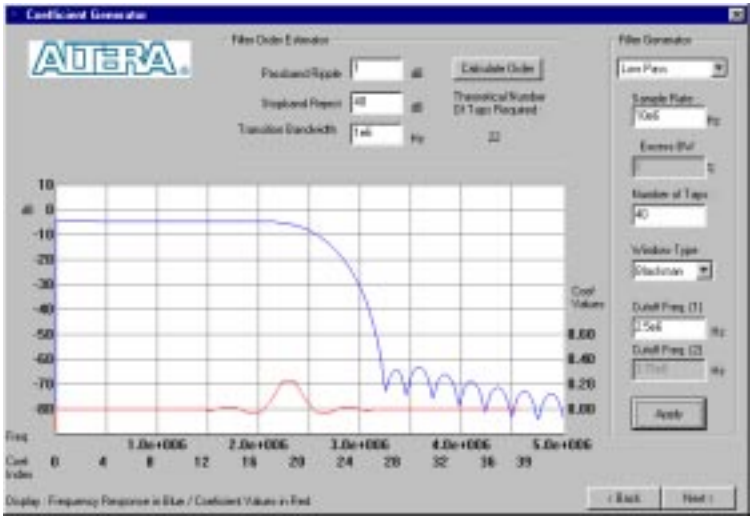
To receive an OpenCore version of a megafunction, contact the AMPP partner directly for an authorization code; the AMPP partner generates this code based on the user's MAX+PLUS II PC or UNIX workstation identification. For Altera MegaCore functions, designers can download OpenCore versions directly from the Altera web site.

MegaWizard™ Plug-In

MegaWizard Plug-Ins

Altera is the first PLD vendor to offer customers the capability to alter megafunction parameters without restricting the end user's design flow. MegaWizard™ Plug-Ins allow users to customize megafunctions to meet specific design objectives, greatly reducing the time spent specifying a custom function. See Figure 2.

Figure 2. MegaWizard Plug-In Feature



Performance & Density Specifications

The performance and density specifications in this catalog apply to megafunctions that are compiled as stand-alone designs. Additional logic synthesis may affect the performance or density of a megafunction, particularly when the function is combined with other megafunctions or logic. Megafunctions shipped as post-synthesis AHDL files have minimal performance or density variations. Megafunctions supplied as source code files may change in performance or density, depending on the design and the target device. Accurate timing cannot be determined until synthesis and place and route of the final design is complete.

Each megafunction description includes a performance metric that profiles the megafunction when compiled as a stand-alone project. The metric is usually a global clock speed or f_{MAX}; in some cases, other metrics such as a t_{PD} or samples/second is given.

In general, a global clock frequency is not affected by the I/O delays that route the signal off-chip, whereas the t_{SU} and t_{CO} parameters are directly affected by on-chip and off-chip routing. If a megafunction is integrated with other logic or megafunctions on the same device, the set-up and clock-to-output delays are reduced because off-chip/on-chip delays are not required.

Subsequent versions of the Quartus and MAX+PLUS II software, megafunction design modifications, or the availability of faster speed-grade devices may affect density or performance characteristics. Contact the megafunction supplier or Altera for the latest performance specifications.

AMPP Megafunction Pricing

To help determine the cost of a megafunction license and to ensure that the megafunction will be successfully integrated, designers need to provide the following information to the megafunction supplier:

- Relevant megafunction parameters (e.g., bus width, resolution)
- License duration requirements (e.g., lifetime, 6 months)
- Target device architecture (e.g., APEX™ 20K, FLEX® 10K devices)
- Netlist-only or source-code license
- Requirements for modifications or feature changes
- Requirements for design migration (e.g., to an application-specific integrated circuit (ASIC))
- Quartus or MAX+PLUS II environment

MegaCore Pricing

For pricing MegaCore functions, contact your local Altera distributor or representative.

MegaCore Licensing

MegaCore functions are licensed directly from Altera Corporation. A copy of the license agreement can be found on the Altera web site at **http://www.altera.com/ipmegastore**.

Technical Support

Altera provides technical support for Altera MegaCores. Technical support for AMPP partner megafunctions is provided by the respective AMPP partner. For more information on technical support, see the Altera web site at **http://www.altera.com/ipmegastore**.

Warranty

The megafunctions in this catalog, as well as other megafunctions and services available from the AMPP partners, are provided without warranty by Altera. Altera expressly disclaims all warranties, express and implied, with respect to the megafunctions supplied by the AMPP partners, including, but not limited to, implied warranties of merchantability, fitness for a particular purpose, title and non-infringement.

The AMPP partners may offer guarantees or warranties for design performance or functionality; contact individual AMPP partners for details.

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Overview

Historically, digital signal processing (DSP) applications have used only DSP processors, application-specific integrated circuits (ASICs), and application-specific standard products (ASSPs). Although DSP processors are flexible, they offer limited real-time performance. ASICs and ASSP devices are capable of real-time processing, but are limited in their adaptability and flexibility. On the other hand, DSP designs implemented in Altera® programmable logic devices (PLDs) combine the flexibility critical for product differentiation with the speed needed for high-performance applications, such as video convolution, radio frequency systems for cable networks, and spread-spectrum filtering. Because Altera APEX™ and FLEX® devices can be reconfigured, the entire DSP implementation flow can be rearranged. Further, algorithms that were traditionally regarded as a sequence of single instructions can be analyzed to determine possible parallelism. Additional deliverables—such as MATLAB Simulink simulation files, hardware description language (HDL) output files, or development boards—further reduce time-to-market.

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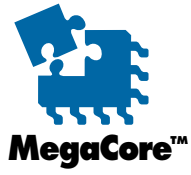
Symbol Interleaver/Deinterleaver

Vendor: Altera
Target Application: Digital, audio and video broadcast, satellite communications, data storage and retrieval systems
Additional Deliverables: Symbol Interleaver/Deinterleaver MegaCore Function User Guide, test vectors
Ordering Code: PLSM-INLV



- High-speed data rates: 120 megasamples per second (MSPS)
- Supports convolutional interleaving algorithm
- Supports block interleaving algorithm
- Parameterized symbol width and codeword length
- Compatible with discrete and streaming Reed-Solomon encoders/decoders
- Optimized for APEX and FLEX architectures
- Internal or external memory architecture
- Parameterized internal or external memory
- Test-vector generation
- Contains a burst error distribution analyzer

General Description

Interleaving is a standard DSP function used in many communications systems. Applications that store or transmit digital data require error correction to reduce the effect of spurious noise that can corrupt data. Digital communications systems designers can choose many types of error-correction codes (ECCs) to reduce the effect of errors in stored or transmitted data. For example, Reed-Solomon encoders/decoders, which are block-encoding algorithms, are used frequently to perform forward error correction (FEC).

Symbol interleaver/deinterleavers can mitigate the effects of burst noise. Typically, these functions are needed for transport channels that require a bit error ratio (BER) on the order of 10^{-6}. Interleaving improves the efficiency of Reed-Solomon encoders/decoders by spreading burst errors across several Reed-Solomon codewords.

The Altera symbol interleaver/deinterleaver function uses internal or external single-port or dual-port RAM. You can implement single-port RAM by using FLEX 10K embedded array blocks (EABs) or an external RAM device; you can implement dual-port RAM using the dual-port RAM capability of APEX 20K embedded system blocks (ESBs) or FLEX 10KE EABs, or an external RAM device. Dual-port RAM provides a faster and smaller implementation than single-port RAM.

The MegaWizard™ Plug-In provided with the symbol interleaver/deinterleaver drastically reduces the design creation and simulation cycles from several weeks to several minutes. The wizard generates a highly optimized instance of a custom interleaver/deinterleaver function as well as a MAX+PLUS® II Vector File (**.vec**) that you can use to simulate the function. For example, by choosing a few simple settings you can build an interleaving function as described in a pre-defined specification such as DVB 802 or UMTS. Additionally, you can implement a custom interleaving function by specifying the parameter values for your specific transmission channel requirements. The flexibility of programmable logic combined with the symbol interleaver/deinterleaver MegaWizard Plug-In allows you to build real-time systems to analyze and improve parameter values determined by theoretical equations.

Functional Description

Interleaving is the process of reordering the symbols in a group of transmitted codewords such that adjacent symbols in the data stream are not from the same codeword. The receiver reassembles the codewords when it processes the data stream. The interleaving process helps reduce the effects of burst errors (i.e., multiple errors in a row), because rearranging the codeword symbols spreads the errors among multiple codewords.

Depending on your application, you may choose to implement a convolutional or a block interleaver/deinterleaver. Convolutional interleaver/deinterleaver functions process data in a continuous stream, which makes them ideal for high-speed applications that require correction for burst errors (e.g., digital video broadcasting). Typically, these functions are used with Reed-Solomon functions. Block interleaver/deinterleavers process data in a discrete stream and are used in applications such as GSM or UMTS (i.e., mobile phones). These functions are often used with Reed-Solomon functions or Turbo Code encoders/decoders. Compared to block interleavers/deinterleavers, convolutional interleavers/deinterleavers provide reduced delay and lower memory usage for the same distribution of errors.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10KE	-1	392	8	110 MHz	`DEPTH` = 12, `UNIT DELAY` = 17, `SYMBOL WIDTH` = 8 bits (digital video broadcast settings) *(1)*
	-1	40	4	120 MHz	`BLOCK LENGTH` = 36, `SPAN DELAY` = 17, `DATA WIDTH` = 8 bits (UTRA) ITU-R RTT *(2)*

Notes:
(1) Convolutional interleaver using FLEX 10KE EABs.
(2) Block interleaver using single-port RAM.

For more information on the symbol interleaver/deinterleaver megafunction, see the *Interleaver/Deinterleaver MegaCore Function User Guide*.

Convolutional Encoder

Vendor: Integrated Silicon Systems
Target Application: Cable modem, wireless communications, satellite communications
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-D479

- High performance
- Highly parameterized
- Bit serial or symbol serial data input
- Complements other FEC megafunctions from ISS

General Description

The convolutional encoder megafunction complements ISS's other FEC megafunctions (Reed-Solomon encoders and decoders, scramblers, descramblers, interleavers and deinterleavers, synchronous insertion and synchronous detection, and Viterbi decoders).

Modifiable Parameters

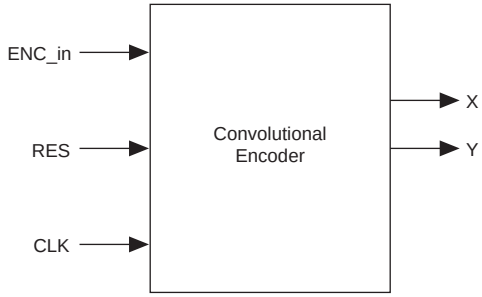
The convolutional encoder megafunction can be configured to use bit rate or symbol rate clocks, to accept the data in bit serial or symbol serial format, and to support a range of international standards. The following megafunction parameters can be modified:

- Performance
- Constraint length
- Code rate
- Generator polynomial
- Puncturing scheme
- Standards compliance

Block Diagram

Figure 1 shows the block diagram for the convolutional encoder megafunction.

Figure 1. Convolutional Encoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-3	39	0	120 MHz	K = 7, R = 1/3, 3/4 (punctured)

Convolutional Interleaver

Vendor: KTech Telecommunications
Target Application: Personal communication systems (PCS), cable modems
Additional Deliverables: Constraint file
ID Code: 52A2-4B52

- Implements a convolutional interleaver function
- Accepts a byte at the input with each clock cycle
- Produces a convolutional-interleaved byte at the output with each clock cycle
- Applications include digital receivers for personal communication systems (PCS) and cable modems

General Description

The convolutional interleaver megafunction implements a convolutional interleaving design that is optimized for PCS and cable modem applications. In FLEX 10K devices, the megafunction uses EABs to support interleaving depth for most convolutional interleaving applications, such as PCS and cable modems. The FLEX 10K EABs support a maximum interleaving size ($N \times M$) of 3,072 bytes, where N is the final index of the interleaving depth and M is the bit memory stage first-in first-out (FIFO) shift register size. For larger interleaving depth, the megafunction requires an external dual-port RAM. A convolutional interleaver megafunction that uses external RAM can be efficiently optimized for FLEX 10K, FLEX 8000, or MAX® 9000 device architectures.

Functional Description

The convolutional interleaver megafunction accepts the input data signal 8 bits at a time. At each byte clock cycle, the `signal_in[7..0]` and `signal_out[7..0]` buses shift to the next row of delay elements. When the maximum depth N is reached, the `signal_in[7..0]` and `signal_out[7..0]` buses go back to the initial index 1 and continue with each cycle of the byte clock. After a delay is introduced by the interleaver, the `signal_out[7..0]` bus produces 8 bits at each byte clock.

Modifiable Parameters

The following megafunction parameters can be modified:

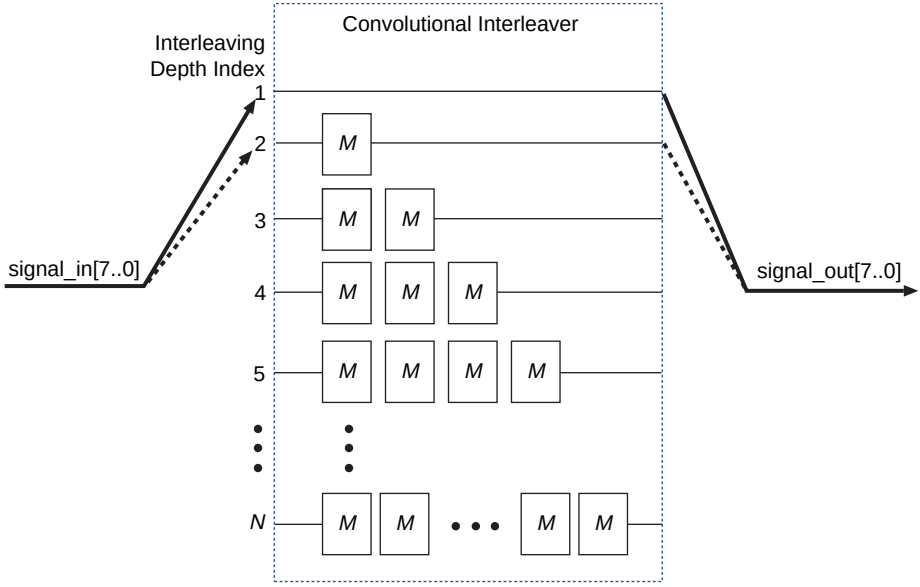
Modifiable Parameters

Parameter	Description
SI	Signal data input size
SO	Signal data output size

Block Diagram

Figure 2 shows the block diagram for the convolutional interleaver megafunction, in which *M* is the bit memory stage FIFO shift register size.

Figure 2. Convolutional Interleaver Megafunction Block Diagram

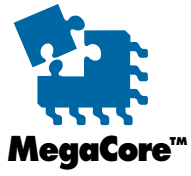


Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	252	0	52 MHz	SI = 8, SO = 8

Reed-Solomon Encoder/Decoder

Vendor: Altera
Target Application: Wireless communications, digital audio and video broadcast, and data storage and retrieval systems
Additional Deliverables: Reed-Solomon Encoder/Decoder MegaCore Function User Guide, test vectors
Ordering Code: PLSM-RSCODEC



- High-performance encoder/decoder for error detection and correction
- Easy-to-use MegaWizard Plug-In
  - Generates parameterized encoders or decoders
  - Generates example test vectors
- Efficient VHDL simulation model
- Fully parameterized Reed-Solomon function including:
  - Number of bits per symbol
  - Number of symbols per codeword
  - Number of check symbols per codeword
  - Field polynomial
  - First root of generator polynomial
- Decoder implementation options:
  - Standard or erasure-supporting
  - Discrete or streaming (pipelined)
  - Fast or small
- Optimized for the APEX 20K and FLEX 10K device architectures

General Description

Reed-Solomon codes are widely used for error detection and correction. To use Reed-Solomon codes, a data stream is first broken into a series of codewords. Each codeword consists of several information symbols followed by several check symbols (also known as parity symbols). Symbols can contain an arbitrary number of bits. The Altera Reed-Solomon MegaCore™ function supports four to eight bits per symbol. In an error correction system, the encoder adds parity symbols to the data stream prior to its transmission over a communications channel. Once the data is received, the decoder checks for and corrects any errors.

Reed-Solomon codes are described as (*N*,*K*), where *N* is the total number of symbols per codeword and *K* is the number of information symbols. Errors are defined on a symbol basis, (i.e., any number of bit errors within a symbol is considered as only one error). A Reed-Solomon decoder can correct one symbol error for every two check symbols in a codeword. However, if a codeword contains many errors, the decoder can only detect up to one symbol error for each check symbol.

Reed-Solomon codes are based on finite-field (i.e., Galois field) arithmetic. All arithmetic operations (i.e., addition, subtraction, multiplication, and division) on field elements give results that are an element of the field. The size of the Galois field is determined by the number of bits per symbol; specifically, the field has 2^m elements, where m is the number of bits per symbol. A specific Galois field is defined by a polynomial, which is user-defined for the Reed-Solomon MegaCore function. The MegaWizard Plug-In only lets the user select valid field polynomials.

The maximum number of symbols in a codeword is limited by the size of the finite field to $2^m - 1$. For example, a code based on 8-bit symbols can have up to 255 symbols per codeword.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10KE	-1	455	6	162 Mbps	speed = full, m = 4 (streaming)
		706	6	273 Mbps	speed = full, m = 5 (streaming)
		844	6	400 Mbps	speed = full, m = 6 (streaming)
		2,543	6	438 Mbps	speed = full, m = 8 (streaming)
		1,988	3	112 Mbps	speed = full, m = 8 (discrete)
		3,265	7	318 Mbps	speed = full, m = 8 (streaming)

For more information on the Reed-Solomon encoder/decoder megafunction, see the *Reed-Solomon MegaCore Function User Guide*.

Reed-Solomon Encoder

Vendor: Integrated Silicon Systems
Target Application: Digital video and audio broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-E479

- Configurable solution for high data rate Reed-Solomon encoding
- Supports a range of standards, including European Telecommunication Standards (ETS) 300-421 and ETS 300-429.
- Single implementation supports any valid block length
- Processes both burst and continuous data
- Supports high-speed applications (up to 400 Mbps)
- Symbol wide input and output, clocked by single symbol rate clock (higher rate clocks, if available, can be used to reduce gate count)
- Low latency implementation: 2 symbol clock cycles
- Simple function interface allows easy integration into larger systems

General Description

The ISS Reed-Solomon encoder megafunction provides compact, high-performance solutions for a wide range of applications.

The European DVB standards provide system requirements for the broadcast of Motion Pictures Expert Group (MPEG)-2 transport packets via, for example, cable or satellite channels. Reed-Solomon error correction coding techniques are employed on the 188-byte MTS packets, with the capability to correct 8 errors per transport packet. This correction requires the use of 16 parity symbols per MTS packet, resulting in a shortened Reed-Solomon codeword of N = 204, K= 188 (N is the number of symbols per codeword, K is the number of information symbols).

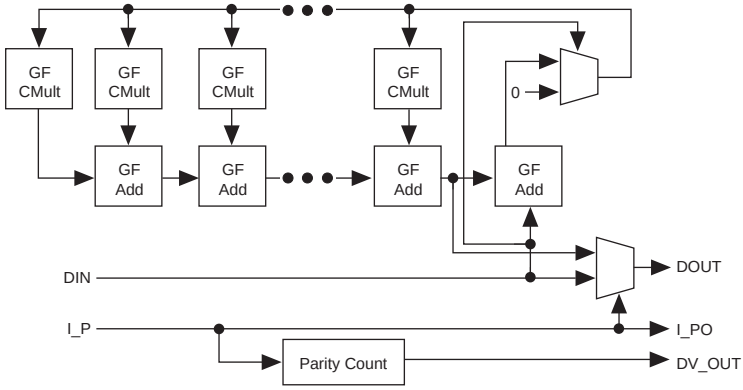
ISS offers a range of Reed-Solomon encoder megafunctions, capable of operating up to 400 Mbps on Altera complex programmable logic devices (CPLDs). This megafunction is designed specifically for the requirements of the DVB standards.

The Reed-Solomon encoder megafunction assumes only the availability of a symbol rate clock and all operations in the encoder are timed with this clock. If a higher rate clock—for example a bit rate clock—is available, the clock can be used to reduce the gate count of the encoder.

Block Diagram

Figure 3 shows the block diagram for the Reed-Solomon encoder megafunction.

Figure 3. Reed-Solomon Encoder Megafunction Block Diagram



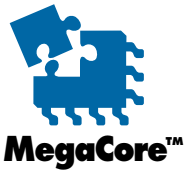
Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	199	0	88 Mbps	N = 204, K = 188, 8-bit symbols

Reed-Solomon Variable (N,K) Encoder

Vendor: Altera
Target Application:
Data communications, digital video broadcast

- High performance (up to 500 Mbps)
- Supports multiple standards
- Fully user parameterized



Preliminary Information

General Description

The Reed-Solomon variable encoder operates like the standard Reed-Solomon encoder, except that the values of N and R can be changed at runtime without reconfiguring the device. The function is compiled for the maximum values of N and R, which can be set by a register write to the function at run time.

The Reed-Solomon variable encoder is a compact, high performance function that can be completely parameterized by the user. The encoder uses the following generator polynomial:

$$g(x) = \prod_{i = \mathrm{GENSTART}}^{\mathrm{GENSTART}+R-1} (x - \alpha^{i})$$

Codewords are generated with no latency, at the symbol clock rate.

The Reed-Solomon variable encoder is optimized for Altera FLEX 6000 and FLEX 10K devices.

Modifiable Parameters

The following megafunction parameters can be modified:

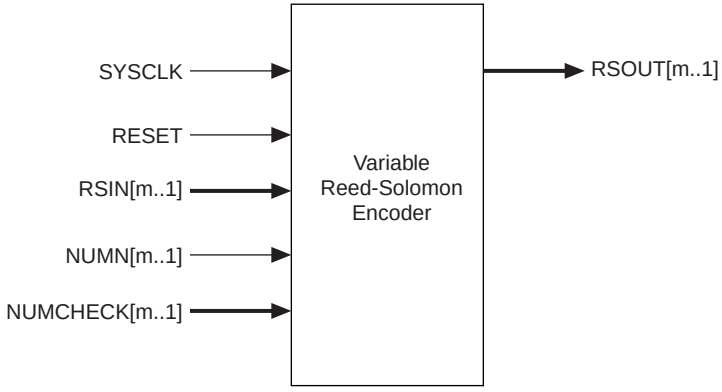
Modifiable Parameters

Parameter	Description
N	The total number of symbols per codeword can range from 3 to $2^m - 1$.
R	The number of check symbols per codeword can range from 4 to (N-1), with a maximum of 40.
M	The number of bits per codeword can range from 4 to 10.
FIELD	The polynomial defining the Galois field for the Reed Solomon decoder may be found using the included **FIELD.EXE** utility, if not defined by a standard.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 4 shows the block diagram for the Reed-Solomon variable encoder megafunction.

Figure 4. Reed-Solomon Variable Encoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	148	0	55 Mbps	N = 30, R = 6, M = 5, FIELD = 55, GENSTART = 0
		953	0	50 Mbps	N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		553	0	40 Mbps	N = 255, R = 10, M = 8, FIELD = 391, GENSTART = 120

Reed-Solomon Decoder

Vendor: Integrated Silicon Systems
Target Application: Digital video and audio broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-E479

- Configurable solution for high data rate Reed-Solomon decoding
- Supports a range of standards, including European Telecommunication Standards (ETS) 300-421 and ETS 300-429
- Single implementation supports any valid block length
- Processes both burst and continuous data
- Supports high-speed applications (up to 400 Mbps)
- Symbol wide input and output, clock by single symbol rate clock (higher rate clock, if available, can be used to reduce gate count)
- Simple function interface allows easy integration into larger systems

General Description

The ISS Reed-Solomon decoder megafunction provides compact, high-performance solutions for a wide range of applications, and is consistent with the requirements of the European digital video broadcast (DVB) standards.

The European DVB standards provide system requirements for the broadcast of MPEG2 transport packets via, for example, cable or satellite channels. Reed-Solomon error correction coding techniques are employed on the 188-byte MTS packets, with the capability to correct 8 errors per transport packet being required. This process requires 16 parity symbols per MTS packet resulting in a shortened Reed-Solomon codeword of N = 204, K= 188.

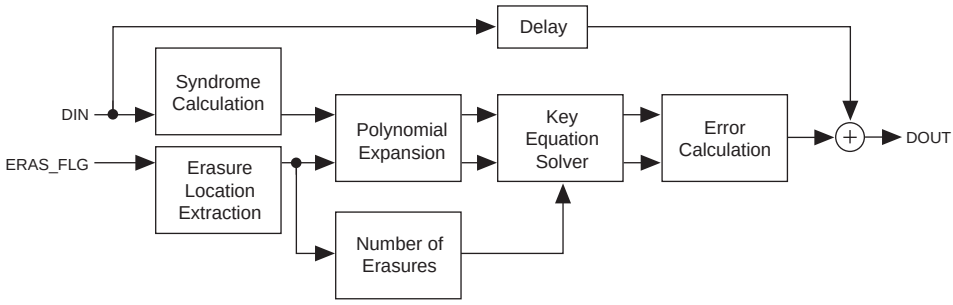
ISS has developed a range of Reed-Solomon decoder megafunctions, capable of operation up to 100 Mbps in Altera CPLDs. This Reed-Solomon decoder megafunction is designed specifically for the requirements of DVB standards.

The megafunction assumes only the availability of a symbol rate clock and all operations in the decoder are timed with this clock. If a higher rate clock, for example a bit rate clock, is available, the clock can be used to reduce the gate count of the decoder.

Block Diagram

Figure 5 shows the block diagram for the Reed-Solomon decoder megafunction.

Figure 5. Reed-Solomon Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,605	6	320 Mbps	N = 204, K = 188, 8-bit symbols

Reed-Solomon Discrete & Streaming Decoders

Vendor: Altera
Target Application: Telecommunications and data communications
Additional Deliverables: DECRELV2.exe (an executable that automatically generates test vectors based on parameters)

MegaCore™

Preliminary Information

- High-speed decoder (up to 500 Mbps)
- Supports multiple standards
- Fully user parameterized

General Description

The Reed-Solomon decoder megafunctions are high-performance, fully parameterized Reed-Solomon functions for Altera APEX 20K and FLEX 10K PLDs. The user can select any combination of parameters that define a Reed-Solomon code, to create a synthesized and routed function within minutes. Data throughput, even with automatically generated and routed functions, is typically in the range of 500 Mbps.

When selecting between discrete and streaming decoders, the following differences will impact the design:

- The discrete function receives a codeword, operates on it, and writes out a corrected codeword. Because the function only operates on one codeword at a time, the discrete decoder has the most flexible interface, but the lowest throughput.
- The streaming decoder receives codewords continuously with short gaps in between. After a system latency, the function writes out codewords at the same rate. Because the streaming decoder operates on three codewords at a time, it provides much higher throughput.
- The function's generator utility, **DECRELV2.EXE**, generates both the function description and test bench, which allows immediate verification.

Reed-Solomon Variable (N,K) Streaming Decoders

The variable Reed-Solomon decoder operates like standard Reed-Solomon decoders, except that the values of N and R may be changed during runtime without reconfiguring the device. The function is compiled with the maximum N and R values to be supported, and then may be configured by a register specifying the current values.

Modifiable Parameters

The following megafunction parameters can be modified:

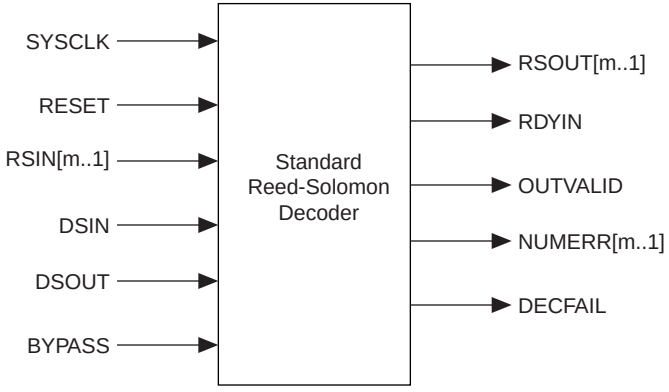
Modifiable Parameters

Parameter	Description
N	The total number of symbols per codeword can range from 3 to $2^m - 1$.
R	The number of check symbols per codeword can range from 4 to (N – 1), with a maximum of 40.
M	The number of bits per codeword can range from 4 to 10.
FIELD	The polynomial defining the Galois field for the Reed Solomon decoder may be found using the included **FIELD.EXE** utility, if not defined by a standard.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 6 shows the block diagram for the Reed-Solomon decoder megafunction.

Figure 6. Reed-Solomon Discrete & Streaming Decoder Megafunction Block Diagram

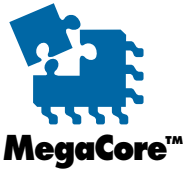


Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	517	3	66 MHz (60 Mbps)	Discrete mode: N = 30, R = 6, M = 5, FIELD = 55, GENSTART = 0
		735	6	66 MHz (220 Mbps)	Streaming mode: N = 30, R = 6, M = 5, FIELD = 55, GENSTART = 0
EPF10K50E	-1	1,988	3	55 MHz (120 Mbps)	Discrete mode: N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		2,502	6	55 MHz (420 Mbps)	Streaming mode: N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		1,410	3	53 MHz (130 Mbps)	Discrete mode: N = 255, R = 10, M = 8, FIELD = 391, GENSTART = 120

Reed-Solomon Continuous Decoder

Vendor: Altera
Target Application: Telecommunications and data communications
Additional Deliverables: DECRSV3.exe (an executable that automatically generates test vectors based on parameters)



Preliminary Information

- High performance (up to 500 Mbps)
- Supports multiple standards
- Fully user parameterized

General Description

The continuous Reed-Solomon decoder function is designed to handle continuously burst codeword inputs and outputs, without any gaps between the codewords. It is slightly more restricted in parameter range than the standard decoder or variable decoder functions.

The generator utility, **DECRSV4.EXE**, generates both the functions description, and a test bench for the function, allowing the user to verify the function almost immediately.

Modifiable Parameters

The following megafunction parameters can be modified:

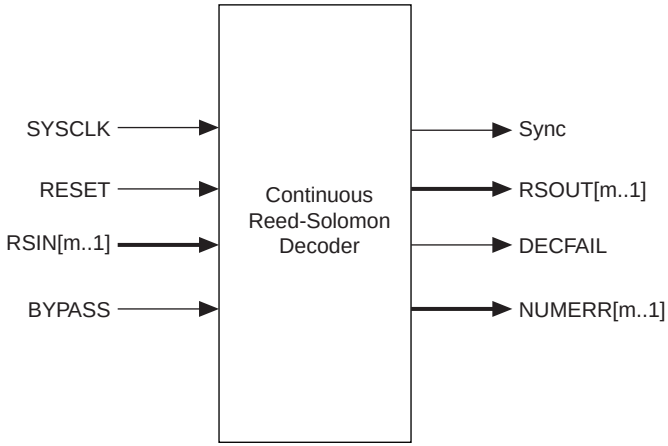
Modifiable Parameters

Parameter	Description
N	The total number of symbols per codeword can range from 3 to $2^m - 1$, with a maximum of 7R.
R	The number of check symbols per codeword can range from 8 to 20.
M	The number of bits per codeword can range from 7 to 10.
FIELD	The polynomial defining the Galois field for the Reed Solomon decoder may be found using the included **FIELD.EXE** utility, if not defined by a standard.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 7 shows the block diagram for the Reed-Solomon continuous decoder megafunction.

Figure 7. Reed-Solomon Continuous Decoder Megafunction Block Diagram

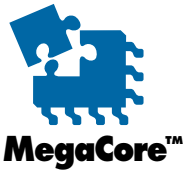


Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	1,282	6	55 MHz (440 Mbps)	N = 255, R = 8, M = 8, FIELD = 285, GENSTART = 0
EPF10K50E	-1	2,485	6	55 MHz (440 Mbps)	N = 204, R = 8, M = 8, FIELD = 285, GENSTART = 0
		1,807	7	50 MHz (400 Mbps)	N = 85, R = 10, M = 8, FIELD = 391, GENSTART = 120

Reed-Solomon Decoder with Erasures Option

Vendor: Altera
Target Application: Telecommunications and data communications



Preliminary Information

- Adds erasure support to standard decoders
- Available in both discrete and streaming modes
- High performance without additional latency
- Supports multiple standards
- Fully user parameterized

General Description

The Reed-Solomon decoder with erasures operates in an identical manner to the decoders without the erasures option. No additional latency is incurred by the use of erasures. Erasures are only used on the decoding side. The standard Reed-Solomon encoder is still used on the encoding side.

Erasures can double the error correcting capability of a Reed-Solomon code. For random errors, a Reed-Solomon code requires two check symbols to find and correct the error. If the location of the error is known, only one check symbol is required to correct the error with an erasures algorithm. With the erasures option, up to R (see "Modifiable Parameters" below) erasure locations can be handled per codeword.

As Reed-Solomon codes find and correct errors by the polynomial evaluation, the polynomial lengths have to be doubled if the error correction capability of the code is to be doubled. For this reason, the logic resources required for a decoder with the erasures option is almost doubled (typically 7/4) over standard decoders.

Modifiable Parameters

The following megafunction parameters can be modified:

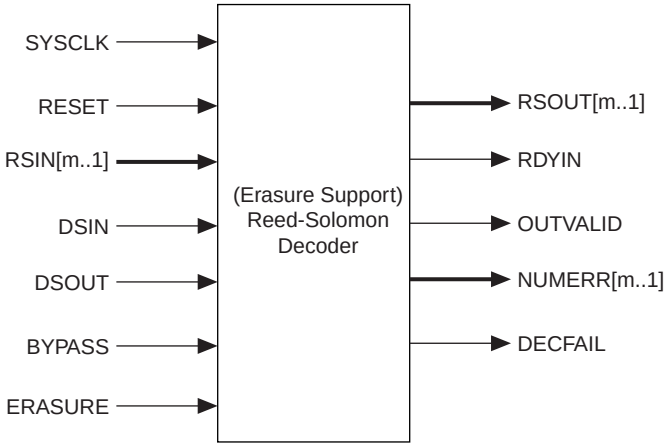
Modifiable Parameters

Parameter	Description
N	The total number of symbols per codeword can range from 3 to $2^m - 1$.
R	The number of check symbols per codeword can range from 4 to (N –1), with a maximum of 40.
M	The number of bits per codeword can range from 4 to 10.
FIELD	The polynomial defining the Galois field for the Reed Solomon decoder may be found using the included **FIELD.EXE** utility, if not defined by a standard.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 8 shows the block diagram for the Reed-Solomon erasures option decoder megafunction.

Figure 8. Reed-Solomon Erasures Option Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50E	-1	1617	7	53 MHz (408 Mbps)	Streaming mode: N = 128, R = 4, M = 8, FIELD = 391, GENSTART = 120
EPF10K100	-1	3334	6	51 MHz (120 Mbps)	Discrete mode: N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)

Dual-Constraint-Length Viterbi Decoder

Vendor: Nova Engineering
Target Application: Communications, Satellite Communications, MIL-STD-188-181, MIL-STD-188-182, MIL-STD-188-183
Additional Deliverables: Simulation files
ID Code: 66A3-F801

- Dual constraint lengths (K = 7, and K = 9)
- Multiple rates (R = 1/2, 3/4, 7/8)
- Hard or soft decision
- Built-in BER monitor

General Description

The performance of modern digital communications systems are often restricted due to power limitations and the presence of Additive White Gaussian Noise (AWGN). The addition of FEC to transmitted digital waveforms overcomes these limitations. One of the most efficient FEC techniques employs a combination of convolutional encoding and Viterbi decoding. The dual-constraint-length Viterbi decoder megafunction provides a decoder for the following modes:

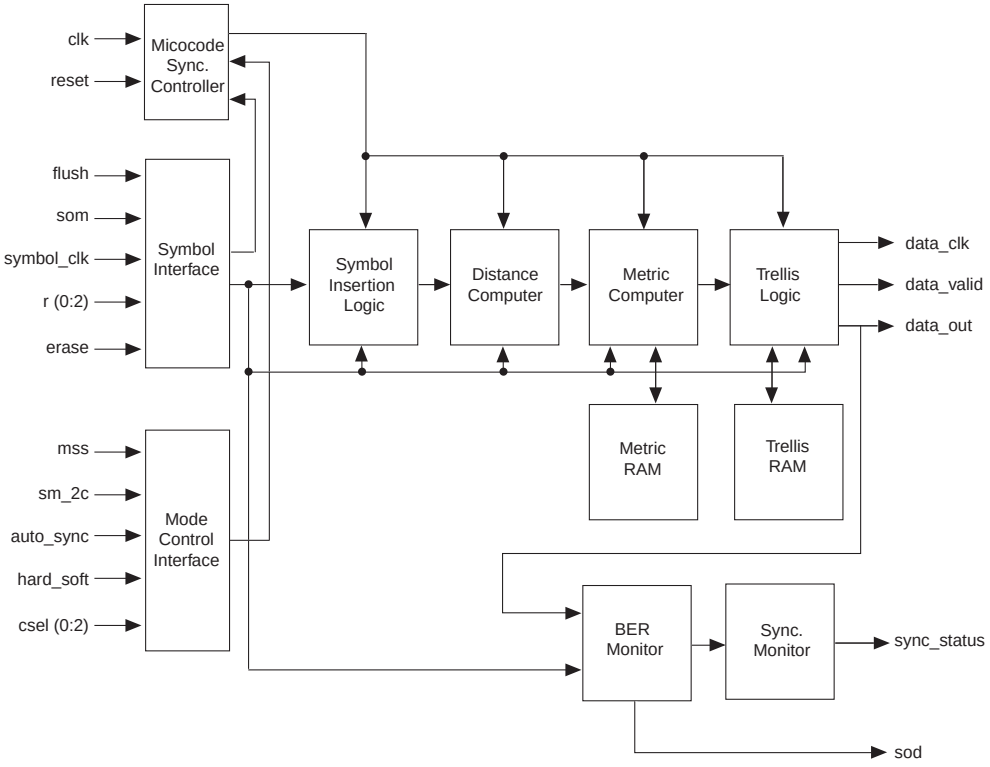
- K = 7, rate 1/2
- Punctured K = 7, rate 3/4
- Punctured K = 7, rate 7/8
- K = 9, rate 3/4

Both soft decision and hard decision decoding are supported in either sign/magnitude or two's complement format. The decoder can be operated in a synchronous manner using the `start-of-message` signal, or it can self-synchronize by selecting the `auto_sync` feature.

Block Diagram

Figure 9 shows the block diagram for the dual-constraint-length Viterbi decoder megafunction.

Figure 9. Dual-Constraint-Length Viterbi Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K250A	-2	2,327	15	20 MHz	Contact Nova Engineering

Viterbi Decoder

Vendor: CAST
Target Application:
Forward error correction, wireless telecommunications, consumer electronics
Additional Deliverables:
VHDL test bench
ID Code: 2AA5-C014

- Hard decision decoder
- Trace-back method for survivor memory
- Branch metric computations can be added for different applications

General Description

The Viterbi decoder megafunction decodes convolutional codes. The megafunction can also be used to produce the best estimate of a transmitted sequence over a channel with inter-symbol interference (ISI).

The megafunction finds the most likely path of the incoming data. The path is calculated so that the data is compared to the data in the branch metric table (this table shows the allowed data symbols, which are dependent on the encoder), and the error between received symbol and the symbol in table is calculated. The path with the smallest error is selected.

Viterbi_AcsUnit Module

The Viterbi_AcsUnit module calculates the path metrics to find the minimum path. The number of add-compare-select (ACS) units is parameterizable.

Viterbi_SmuCtrl Module

The Viterbi_SmuCtrl module manages the survivor memory. The state machine controls the alternate reading of new branch metrics and the trace-back. During trace-back, the megafunction reads the decision values from memory and outputs the decoded bits. The megafunction reconstructs the encoder's actions in reverse order by updating the state register with a decision value pointed by the former state value. As a result, the decoded bits are also output in reverse order.

Viterbi_Memory Module

The Viterbi_Memory module is an optional RAM memory that stores the trace-back values during calculation.

Modifiable Parameters

The following megafunction parameters can be modified:

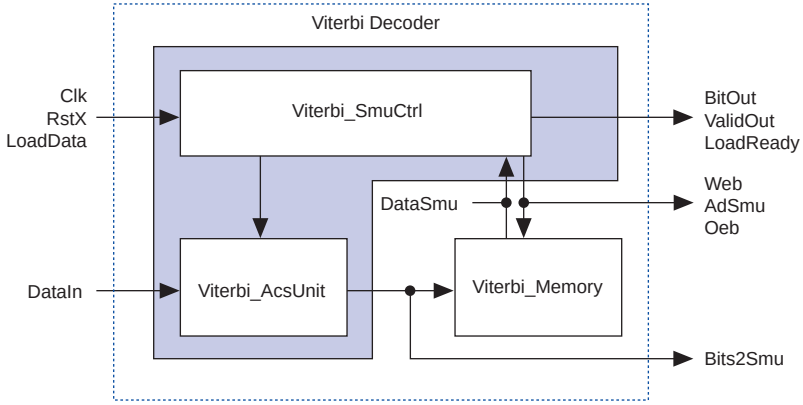
Modifiable Parameters

Parameter	Description
N	Number of states in the trellis
NB	Number of bits to represent transition values
ACS	ACS cells
LTB	Length of the trace-back
LRB	Length of the received burst
IP	Initial path metric for state 0
MWL	Survivor memory (RAM) word length

Block Diagram

Figure 10 shows a block diagram of the Viterbi decoder megafunction.

Figure 10. Viterbi Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	960	0	31 MHz	N = 16, NB = 8, ACS = 4, LTB = 30, LRB = 5, IP = –4, MWL = 8
EPF6016	-2	954	–	17 MHz	

Viterbi Decoder

Vendor: Integrated Silicon Systems
Target Application: Digital video broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Behavioral VHDL testbench, documentation
ID Code: C38B-DC41

- Soft decision decoder
- High-speed applications, typically 45 millions of samples per second (MSPS) on continuous data stream
- Compatible with other ISS FEC megafunctions
- Dynamic support of R = 1/2 and R = 3/4
- May be configured in terms of constraint length K, rate R, soft or hard decision
- Simple interface allows easy integration into larger systems

General Description

The ISS Viterbi decoder megafunction is a high-performance implementation suitable for a range of FEC applications. The megafunction may be used in conjunction with other FEC-related megafunctions available from ISS to rapidly construct complete FEC solutions.

The megafunction has been developed in HDL and has been tailored specifically for Altera APEX and FLEX architectures to obtain compact, high-performance implementations.

The basic megafunction assumes only the provision of a symbol rate clock. If a higher rate clock is available in the system, some of the hardware may be reused multiple times per data symbol period, reducing the overall hardware requirements. If the latency of the first sample is approximately 960 Clk × 4 cycles, a continuous data stream could be processed at 47 MSPS typically.

The ISS Viterbi decoder megafunction can be rapidly configured for a wide range of specifications. The megafunctions have been developed using HDLs, in a modular and parameterizable fashion. This design gives ISS the capability to quickly configure a specific implementation to a user's specification by adding specific modules, such as the interleaver/deinterleaver and scrambler/descrambler.

Modifiable Parameters

The following megafunction parameters can be modified:

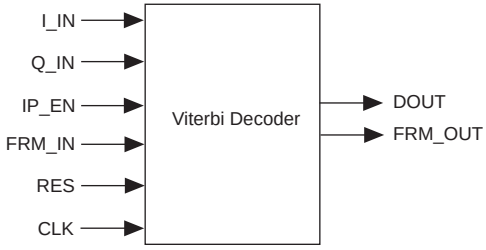
Modifiable Parameters

Parameter	Description
K	Constraint length
R	Decoder rate
P	Puncturing scheme
D	Soft or hard decision decoder

Block Diagram

Figure 11 shows a block diagram of the Viterbi decoder megafunction.

Figure 11. Viterbi Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K200E	-1	2,846	4	19.5 ns, 51.28 MHz	K = 7, R = 1/2, soft decision decoder

DVB FEC Codec

Vendor: Integrated Silicon Systems
Target Application: Digital video broadcast
Additional Deliverables: Verilog test files to support simulation and verification
ID Code: C38B-DC42

- Complete DVB FEC solution, which includes:
  - Scrambler/descrambler
  - Reed-Solomon encoder/decoder
  - Interleaver/deinterleaver
- 8-bit parallel data symbol input and output
- Bit-rate and symbol-rate clock required
- Reed-Solomon code generator polynomial according to ETS 300-429
- Reed-Solomon field generator polynomial according to ETS 300-429
- Reed-Solomon codeword format (204,188)
- Two input control signals provided to both transmit (Tx) and receive (Rx)
  - Low to high transition at the start of the codeword and high to low transition at the end of the codeword
  - Low to high transition at the start of the codeword and high to low transition at the start of the parity
  - Rx function also has input for external synchronizing signal for Descrambler block
- Statistics reporting
- Interleave depth = 12
- Constant latency regardless of mode of operation, except when external RAM removed
- Encoder and decoder supplied as separate functions

General Description

A top level block diagram for the FEC Tx and Rx modules is provided in Figure 12 on page 40.

Functional Description

The following sections discuss the functional description of the transmitter and receiver.

Transmitter

Each block in the transmit function has a fixed latency, and when disabled will pass the data unmodified with the same latency.

The scrambler block is known as the Mux Adaptation and Energy Dispersal block in the ETS DVB specification. This block contains Pseudo Random Binary Sequence (PRBS) generators to ensure an even 1-to-0 ratio in the transmitted data stream. To ensure that transmitter and receiver synchronize their PRBS generators, the first byte in every 8 packets is inverted. In the normal MPEG-2 scheme, this byte will be a 47 hex value.

The scrambler block waits for the first byte of the first packet immediately after Reset is de-asserted, by monitoring the state of the `TxIPIn` and `TxDVIn` signals. The first byte after reset for which these signals are asserted is assumed to be the synchronous byte, and is inverted. Thereafter the first byte in every eighth packet is also inverted.

The Reed-Solomon encoder block generates parity symbols and inserts these in the data stream when `RxDVIn` is asserted and `RxIPIn` is de-asserted. The value of the input data (`RxDIn`) at this time is ignored.

The convolutional interleaver has an interleave depth of 12 and requires the use of an external DPRAM to perform this function. It passes bytes through the block with varying latency. The sync bytes always pass with minimum latency. The total transmit function latency for invalid bytes, sync bytes, and every 12th byte—or for all bytes when the interleaver is disabled—is 4 ticks.

RECEIVER

Each block in the receiver function has a fixed latency, and when disabled will pass the data unmodified with the same latency.

The convolutional deinterleaver assumes that the first valid byte after reset (first byte with `RxDVIn` asserted) is a sync byte and delays this byte by the maximum fixed delay (11 packets). Thereafter, every twelfth byte will have the same delay. Bytes are delayed by successively smaller amounts until the eleventh byte, which has zero delay applied. Invalid bytes are not delayed, and when the deinterleaver is disabled, all bytes are passed though with no delay.

The Reed-Solomon decoder holds a packet until it has been either completely corrected, or the number of errors is too great. In the latter case the packet is passed out with the RxUncOut signal asserted for the entire packet. This makes it easier for downstream hardware to discard uncorrectable packets. The decoder also maintains a count of the number of corrected bytes in the 0-to-8 range. This value is held after the end of a packet until the first byte of the next packet, when it is cleared (or set to 1 if the first byte was corrected). The function asserts RxCorOut and updates the count at the same time as it outputs each corrected byte.

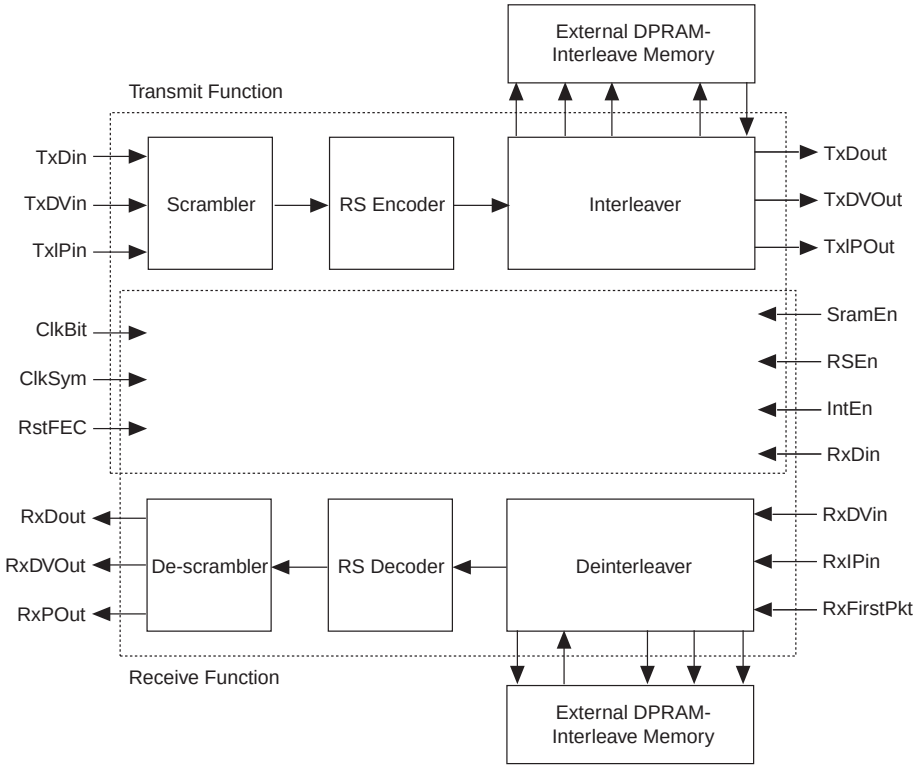
The descrambler block needs knowledge of which synchronous byte is the eighth packet to reset its PRBS. Since the data stream in this application may not be MPEG-2 compliant, the Rx function must be told by external hardware when this synchronous byte arrives. The RxFirstPkt signal should be asserted when the synchronous byte is driven on the RxDIn pins. This signal is delayed appropriately to match the delay through the convolutional deinterleaver and the Reed-Solomon decoder. There is no synchronization mechanism for a PRBS generator for non-valid bytes; therefore, only bytes with RxDVOut asserted will be correct.

The total delay through the Rx function is 610 clock ticks for invalid bytes and for bytes which are 11 bytes after the synchronous byte, and every twelfth byte thereafter, or all bytes when the deinterleaver is disabled. The combination of the Tx function interleaver and Rx function deinterleaver delays results in an additional overall delay of 11 packets when interleaving is enabled.

Block Diagram

Figure 12 shows the block diagram of the DVB FEC Codec megafunction.

Figure 12. DVB FEC Codec Megafunction Block Diagram



Device Utilization Example

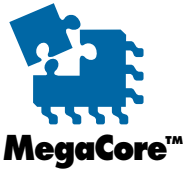
Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50RC240	-3	1,915	6	44.376 MHz	Maximum symbol rate 5.547 MHz

Although the functions are illustrated combined, they are supplied separately with necessary control signals duplicated.

µ-Law & A-Law Companders

Vendor: Altera
Target Application:
Voice applications

- G.711 Compliant
- High performance
- Area efficient



Preliminary Information

General Description

The µ-Law and A-Law compander megafunctions consist of separate compression and expansion components. For the µ-Law megafunction, the standard of 14 bits to 8 bits to 14 bits is implemented. For the A-Law megafunction, the standard of 13 bits to 8 bits to 13 bits is implemented. Both megafunctions are purely combinatorial and very compact.

Because of the high performance of the megafunctions, many voice channels can be supported by a single instance.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	57	0	30 ns	µ-Law compressor
		29	0	20 ns	µ-Law expander
		30	0	18 ns	A-Law compressor
		26	0	18 ns	A-Law expander

Linear Feedback Shift Register

Vendor: Nova Engineering
Target Application: Direct sequence spread spectrum (DSSS), pseudo-random number (PN) generation, wireless communications, encryption and decryption, error detection
Additional Deliverables: Simulation file
ID Code: 66A3-F401

- Programmable pattern length
- Automatic resizing and feedback selection
- Programmable initial value (IV)
- Optimized for the Altera APEX 20K, FLEX 10K, and FLEX 8000 device architectures
- Applications
  - Encryption/decryption
  - Direct sequence spread spectrum
  - Pseudo-random number (PN) generation
  - Scrambler/de-scrambler
  - Built-in self test

General Description

A linear feedback shift register (LFSR) megafunction is based on linear XOR or XNOR feedback logic in which the initial value of the shift register, shift register taps, and feedback logic determines the output sequence. This scheme allows the user to load the shift register with an initialization sequence. The shift register taps are combined with XOR or XNOR logic and then fed back into the shift register input.

Functional Description

The shift register size (m) is equal to `length` + 1, where `length` is an integer between 1 and 31. The shift register produces a sequence of $2^m - 1$ bits. For example, a shift register size of 32 produces a shift register sequence of $2^{32} - 1$ bits and is specified by setting the `length` input to 31. The `length` input is synchronous to the rising edge of the `clock`. When a `clock` edge loads the `length` input, the megafunction will automatically reconfigure the shift register's size.

The `load` input initializes the contents of the shift register. Whenever `load` is asserted, the megafunction configures itself to a normal shift register size of 32. The desired initial value will be loaded through the `shift_in` input using 32 clock cycles. Because the `length` value is ignored when `load` is asserted, `length` can be asserted any time before `load` de-asserts. The `load` input can be de-asserted after the 32nd rising clock edge. The next rising edge of the `clock` would then configure the shift register size and feedback logic and initialize the length sequence.

The following table describes the LFSR parameters.

LFSR Megafunction Parameters		
Name	**Typical Values**	**Description**
Shift register size(s)	2 to 32 bits	Specified by user.
Feedback logic configuration	XOR	Can be customized for either XOR or XNOR applications.

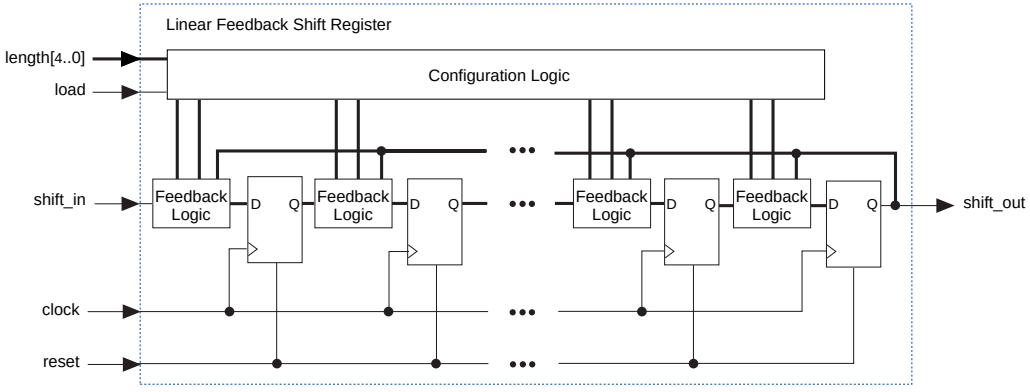
Modifiable Parameters

Nova Engineering will customize the LFSR megafunction's shift register size and the feedback configuration to meet user specifications at no additional cost. This customization reduces logic usage and optimizes area and performance.

Block Diagram

Figure 13 shows the block diagram for the LFSR megafunction.

Figure 13. Linear Feedback Shift Register Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	338	0	103 MHz	Contact Nova Engineering
EPF6016	-2	318	0	95 MHz	Contact Nova Engineering
EPM7128E	-7	103	0	113 MHz	Contact Nova Engineering

Parameterized CRC Generator/Checker

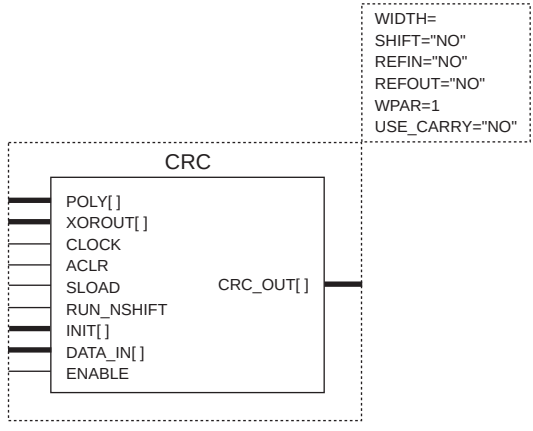
Vendor: Altera
Target Application: DSP
Additional Deliverables: crc MegaCore Function Parameterized CRC Generator/Checker Data Sheet
Ordering Code: PLSM-CRC

- crc MegaCore function, general-purpose cyclic redundancy code (CRC) generator and checker
- Optimized for the APEX and FLEX device architectures
- Supported by the Quartus™ and MAX+PLUS® II development system
- High-speed operation, over 100 MHz for many configurations
- Fully parameterized, including:
  - Any length generator polynomial
  - Input data width, from 1 bit to the width of the polynomial
  - Any initial value
- Built-in support for:
  - Inverting output data
- Reflecting (reversing bit order) input and output data

General Description

The crc MegaCore function is a general-purpose CRC generator and checker that validates data frames and ensures that data corruption during transmission is detected. The crc function is fully parameterized, and therefore can be used in virtually any design that requires a CRC checker. See Figure 14.

Figure 14. crc Symbol



Functional Description

The `crc` function validates data streams via redundant encoding. CRCs are a preferred type of redundant encoding, where redundant bits are spread over more bits than the original data stream. Similar to parity checking, CRC encoding is a method of generating a code to verify the integrity of the data stream. However, while parity checking uses one bit to indicate even or odd parity, CRC encoding uses multiple bits, and therefore catches more errors in the data stream.

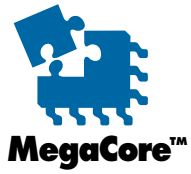
CRCs are particularly effective for two reasons:

- CRCs provide excellent protection against common errors such as burst errors, in which consecutive bits in a data stream are corrupted during transmission.
- The original data is the first part of the transmission, which makes systems that use CRCs easy to understand and implement.

The `crc` function is fully parameterized. Thus, virtually any CRC algorithm can be defined using the parameters described in this data sheet. To maximize flexibility, the `crc` function also allows designers to set port values, e.g., initial register values can be set via the `init[WIDTH-1..0]` input.

FIR Compiler

Vendor: Altera
Target Application: DSP, video imaging, HDTV, set-top boxes
Additional Deliverables: FIR Compiler MegaCore User Guide
Ordering Code: PLSM-FIR



- First system-level, programmable logic solution for DSP designs, including:
  - Automatic interpolation filters
  - Automatic decimation filters
- Fully integrated finite impulse response (FIR) filter development environment
- Optimized for the APEX 20K and FLEX 10K device architectures
- Fully parallel or serial arithmetic architectures
- Uses any number of taps
- Includes a built-in coefficient generator
- Imports coefficients from third-party tools
- Imports floating-point or integer coefficients from third-party tools
- Uses multiple coefficient scaling algorithms
- Provides floating-point to fixed-point coefficient analysis
- Supports coefficient widths from 4 to 32 bits of precision
- Supports signed or unsigned input data widths, from 4 to 32 bits wide
- User-selectable output precision via rounding and saturation
- Creates MATLAB Simulink, VHDL, and Verilog HDL simulation models
- Generates MAX+PLUS II and Quartus vector files
- Includes an impulse, step function, and random input testbed
- Provides resource estimates dynamically

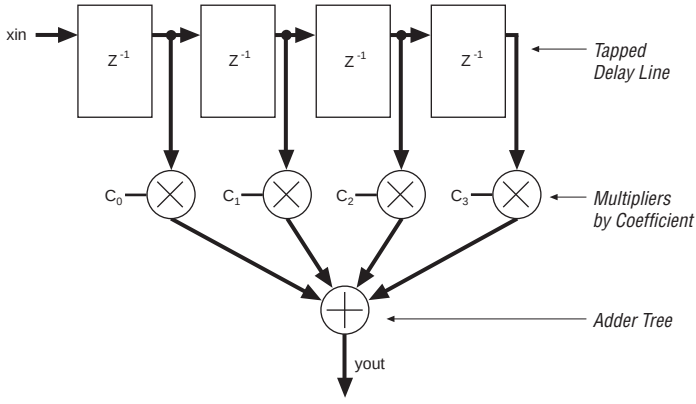
General Description

Many digital systems use signal filtering to remove unwanted noise, provide spectral shaping, or to perform signal detection or analysis. Two types of filters that provide these functions are finite impulse response (FIR) filters and infinite impulse response (IIR) filters. FIR filters are used in systems that require a linear phase and have inherently stable structure. IIR filters are used in systems that can tolerate phase distortion. Typical filter applications include signal preconditioning, band selection, and low-pass filtering.

In contrast to IIR filters, FIR filters have a linear phase and inherent stability. This benefit filter makes FIR filter usually attractive enough that they are designed into a large number of systems. However, for a given frequency response, FIR filters are a higher order than IIR filters, making FIR filters more expensive computationally.

The structure of a FIR filter is a weighted, tapped delay line (see Figure 15). The filter design process involves identifying coefficients that match the frequency response specified for the system. The coefficients determine the structure of the filter. You can change which signal frequencies are passed through the filter by changing the coefficient values or adding more coefficients.

Figure 15. Basic FIR Filter



DSP processors with a limited number of multiplier-accumulators (MACs) require many clock cycles to compute each output value because the number of cycles is directly related to the order of the filter. A dedicated hardware solution can achieve one output per clock cycle. In contrast, a fully parallel, pipelined FIR filter implemented in a PLD can operate at data rates above 100 MSPS, making PLDs ideal for high-speed filtering applications.

The FIR compiler speeds up the design cycle by:

- Finding the coefficients needed to design a particular type of FIR filter with a particular set of characteristics.
- Generating clock-cycle-accurate FIR filter models (also known as bit-true models) in the Verilog HDL and VHDL languages, and for the MATLAB environment (Model Files and M-Files).
- Automatically generating the code required for the MAX+PLUS II or Quartus software to synthesize high-speed, area-efficient FIR filters of various architectures.
- Creating standard test vectors (i.e., impulse, step, and random input) to test the response of the FIR filter.

Functional Description

The FIR compiler has an interactive wizard-driven interface that allows you to create custom FIR filters easily. The wizard outputs simulation files for use with third-party tools, including MATLAB. The FIR compiler supports 3 to 256 taps.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10KE	-1	879	0	82 MHz	17-tap, fully parallel
		1,260	0	101 MHz	19-tap, full parallel
		761	5	69 MHz	79-tap, serial

For more information on the FIR compiler megafunction, see the *FIR Compiler MegaCore Function User Guide*.

Cascadable Adaptive FIR Filter

Vendor: Integrated Silicon Systems
Target Application: 1-D and 2-D adaptive filtering, image and video processing, pulse shaping correlation and equalization, voice processing
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C38B-1126

- Ultra-fast "on-the-fly" coefficient programmability
- High-level specification up to 75 MSPS
- Optimized for the Altera APEX and FLEX architectures
- One-dimensional (1-D) and two-dimensional (2-D) versions available

General Description

The 7-tap, 9-bit data and coefficient finite impulse response (FIR) megafunction with "on-the-fly" coefficient programmability performs the following operation:

$$\texttt{Result[19..0]}_n = \sum_{K=1}^{7} \texttt{DataIn[8..0]}_{(n-K)} \times \texttt{W}_{(K)}\,\texttt{In[8..0]}$$

The variable $\texttt{DataIn[8..0]}_n$ refers to the nth input sample. The variable $\texttt{W}_{(K)}\texttt{In[8..0]}$ refers to the Kth coefficient of the FIR filter.

Data Input Interface

The 9- bit input data word, `DataIn[8..0]`, can be represented by either two's complement or straight binary format. The input data format is defined by the `Sel` signal. When the `Sel` signal is tied to logic 0 during the operation of the 7-tap FIR filter, the data is assumed to be in two's complement format. When the `Sel` signal is tied to logic 1, the data is assumed to be in straight binary format. The data is latched into the filter on the falling edge of the `ClkInput` signal.

Coefficient Loading

The coefficients are in sign plus absolute value representation and are latched into the filter on the falling edge of the `Clk_Load` signal when the `En_Load` signal is asserted high.

Tapped Delay Outputs

The data-tap outputs, `D1Out[8..0]` to `D7Out[8..0]`, are in two's complement format, regardless of the format used by `DataIn[8..0]`. The data-tap outputs are clocked out on the falling edge of the `ClkInput`.

Cascade Data Output

The input data delayed output, `DataOut[8..0]`, is in the same representation as the input data. The input data delayed output is clocked out on the falling edge of the `ClkInput` signal.

Result Output

The two's complement result, `Result[19..0]`, from the filter is clocked out on the falling edge of the `ClkInput` signal.

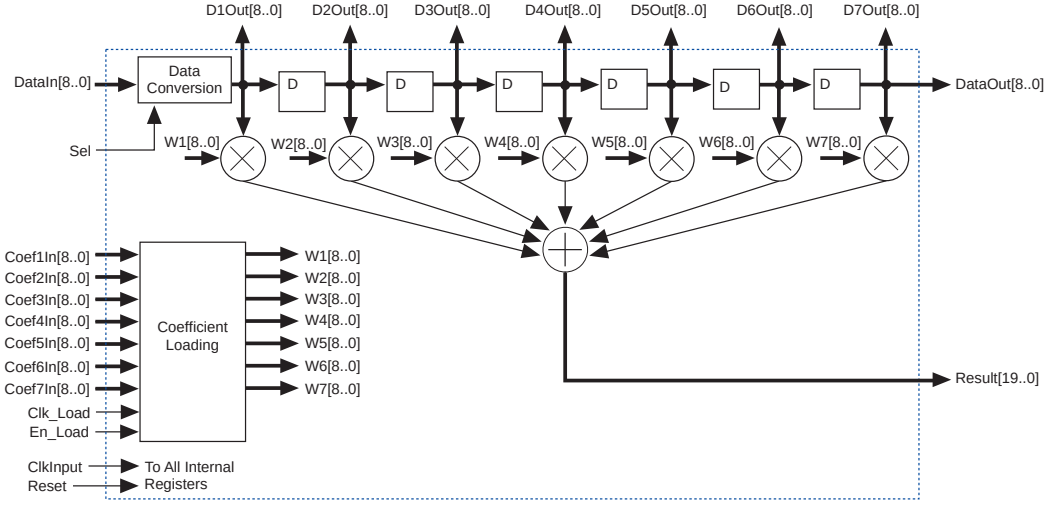
Latency

From the perspective of data entering the megafunction (`DataIn[8..0]`) the latency of the 7 tap FIR filter function is 11 `ClkInput` cycles. `D1Out[8..0]` has a latency of 3 `ClkInput` cycles, `D4Out[8..0]` has a latency of 4 `ClkInput` cycles, `D7Out[8..0]` has a latency of 9 `ClkInput` cycles, and `DataOut[8..0]` has a latency of 9 `ClkInput` cycles.

Block Diagram

Figure 16 shows the block diagram for the cascadable adaptive FIR filter megafunction.

Figure 16. Cascadable Adaptive FIR Filter Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,070	0	75 MSPS	T = 7, W = 9, P = 0

Note:
(1) Contact ISS for design optimization and highest performance results.

FIR Filter Library

Vendor: Integrated Silicon Systems
Target Application: DSP, video imaging, set top boxes, HDTV
ID Code: C38B-70E4

- Sample rates ranging from 2 kHz to over 75 MHz
- Fully parameterized FIR filters
- Both 1-D and 2-D variants available
- Optimized to provide desired functionality with minimum silicon
- "On-the-fly" coefficient adaptation available
- Applications include:
  - 1-D and 2-D FIR filtering
  - Matched filtering
  - Adaptive filtering
  - Image and video processing
  - Pulse shaping
  - Correlation and equalization

General Description

The megafunctions in the FIR filter library, with sample rates ranging from 2 kHz to over 75 MHz, are ideal for solving filtering problems. By cascading the megafunctions, the designer can construct large high-speed FIR filters. The megafunctions can also be replicated to construct a range of FIR filters, which are all covered by the same FIR filter library license.

ISS can customize the number of filter taps, filter dimensions (e.g., 1-D or 2-D), performance (pipelining), and data word lengths and formats. ISS provides test vectors, full documentation, and technical assistance to help designers integrate the megafunction into their projects.

Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40 *(2)*	-3	1,827	0	60.6 MHz	*(2)*
EPF10K30A	-2	701	0	100 MHz	*(3)*

Notes:
(1) Specifications are subject to change.
(2) This example has an 8-bit input data, 8-bit coefficients, full internal accuracy, "on-the-fly" coefficient adaptation, and is cascadable to create larger filters. Contact ISS for design optimization and highest performance results.
(3) 104-tap, 1-bit input data, 10-bit coefficient data, 19-bit output data, dual-bank coefficients, interpolate factor of 4.

IIR Filter Library

Vendor: Integrated Silicon Systems
Target Application: Digital audio processing, digital video processing, signal conditioning, channel selection filtering
Additional Deliverables: User guide
ID Code: C38B-704E

- Cascadable
- High performance
- "On-the-fly" coefficient adaptation available

General Description

The megafunctions in the infinite impulse response (IIR) filter library are used in a broad spectrum of signal bandwidths. The megafunctions are basic building blocks for many IIR filter implementations. A second-order IIR filter, such as a biquad IIR filter, can be used to construct higher orders of filters by cascading the required number of biquad sections. A complete range of high-performance IIR filters can be constructed from a single IIR filter megafunction, which is covered under the same IIR filter library license. The megafunctions can process data at rates in excess of 50 MSPS.

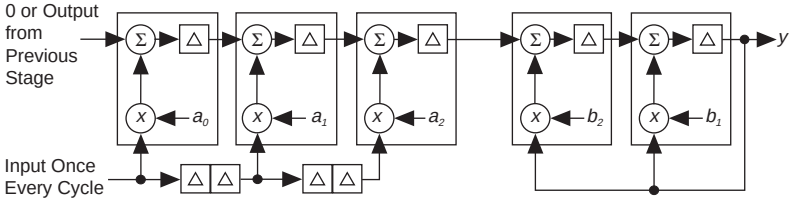
Modifiable Parameters

ISS can customize the data sample rate, coefficient loading strategy, filter order, and data word lengths and formats. Contact ISS for the best parameter settings to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 17 shows the block diagram for the IIR filter library.

Figure 17. IIR Filter Library Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	430	6	17 MHz	Biquad IIR filter with 8-bit input data, 8-bit coefficients, and 11-bit internal accuracy

Rank Order Filter

Vendor: Integrated Silicon Systems
Target Application: Signal processing systems
Additional Deliverables: Simulation files, testbench
ID Code: C38B-1115

- User-defined filter length
- Two-dimensional (2-D) operation available (e.g., 1 × 3, 3 × 3)
- 12-bit two's complement data word length
- 20 MSPS operation

General Description

The rank order filter megafunction enables any rank from a user-defined input data sequence to be selected. Designers can choose both 1-D and 2-D data windows and the length of the window.

Data Configuration Registers

Data is clocked to the function on the rising edge of the clock signal, `clk`. For 1-D operation, only the `data1` input is used, and the `data2` and `data3` inputs are tied low by the user. For 2-D operation, all three data inputs are used.

A range of further configurations are possible, including 1-D filters from 3 to 15 bits, as well as 1 × 3, 3 × 3 2-D filters. The `length` and `D1_D2` inputs configures the filter. The `length` input determines the data length, and it is used with the `D1_D2` input to configure the filter for 2-D operation. The data configuration register block formats the input data for sorting by the next stage in the filter, the shuffle array.

Shuffle Array

The shuffle array processes the data elements of each "window" in parallel. When the data emerges from the shuffle network, it is fully sorted.

Rank Selection

The desired rank value output is selected by input rank under user control.

Latency

A new data sample, or samples in 2-D operation, is loaded into the megafunction on every clock cycle. After the filter is completely filled with data, a result is produced every clock cycle.

The latency in clock cycles from a data series being loaded into the filter to getting the result is 12 clock cycles (i.e., as a new data sample is loaded into the filter, the first result is output 12 clock cycles later). Because the megafunction operates as a sliding window, each data sample contributes to several consecutive results (e.g., 15 results for a 15 × 1 filter). The filter was designed so the latency for all modes of operation are equivalent. A delay is also associated with the loading of the first set of data series (e.g., 15 clock cycles for a 15 × 1 filter).

Modifiable Parameters

The following megafunction parameters can be modified:

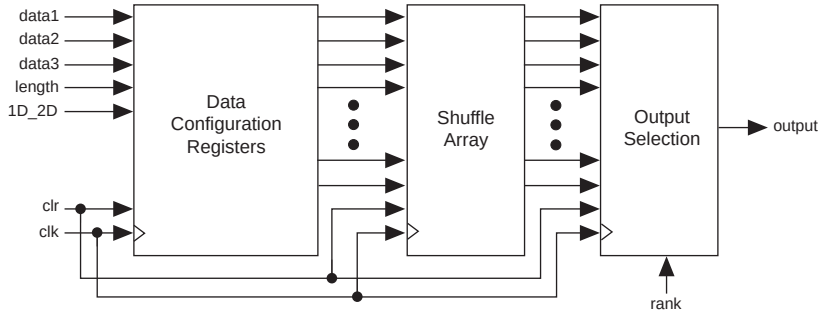
Modifiable Parameters

Parameter	Description
W	Window size
L	Data word length (bits)

Block Diagram

Figure 18 shows the block diagram for the rank order filter megafunction.

Figure 18. Rank Order Filter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	3,852	0	30 MHz	W = 15 × 1, L = 12

Laplacian Edge Detector

Vendor: Integrated Silicon Systems
Target Application: Video, broadcast systems
Additional Deliverables: Simulation files, VHDL template
ID Code: C38B-A264

- Bit parallel input and output data
- Unsigned binary input data format
- Parameterizable input data word lengths, which must be specified by the customer before delivery
- Two output data formats are available (two's complement or signed binary)
- Variants of the megafunction, which can handle input sample rates of up to 90 MHz, are available
- Asynchronous clear input signal

General Description

The Laplacian edge detector megafunction is a two-dimensional (2-D) filter targeted towards real-time front-end image processing applications. The input data words are bit-parallel unsigned binary format to suit the output of most video analog-to-digital converters (ADCs). To use the laplacian edge detector megafunction, the input data must be made available three vertically adjacent pixels at a time.

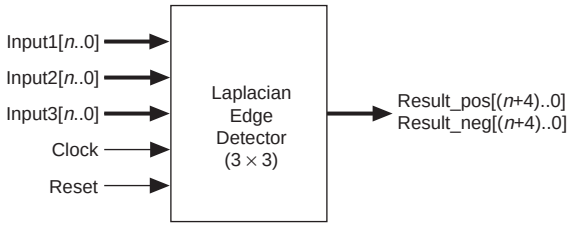
Modifiable Parameters

ISS can customize the input data word length (W) to meet user specifications.

Block Diagram

Figure 19 shows the block diagram for the Laplacian edge detector megafunction.

Figure 19. Laplacian Edge Detector Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	260	0	56 MHz	W = 8, 12

Binary Pattern Correlator

Vendor: Nova Engineering
Target Application: Spread spectrum communications, pattern recognition, error correction, frame synchronization
Additional Deliverables: Simulation file
ID Code: 66A3-F501

- Optimized for the APEX 20K, FLEX 10K, and FLEX 6000 device architectures
- Parallel correlation summing network for maximum speed
- Programmable reference pattern and mask registers
- Cascadable in length and depth
- Applications include:
  - Frame synchronization
  - Spread-spectrum receivers
  - Error correction
  - Pattern matching

General Description

The binary pattern correlator megafunction is a digital correlator that compares the digital pattern stored in the reference pattern register with the data samples stored in the correlator shift register. The megafunction contains the following components: a data shift register, a reference pattern register, a mask register, the correlation array, and the correlation summing network.

Functional Description

To determine the number of matches in a data stream, the megafunction shifts the data samples into the data shift register, where they are compared with the data stored in the reference pattern register. The number of matches is calculated on each rising edge of the clock, and the final sum is referred to as the correlation sum.

Typically, the correlation sum is compared to a programmable threshold. The threshold determines the probability of detection and the false alarm rate. A lower threshold increases the probability of a detection, but it can also increase the probability of a false alarm. For example, if the shift register and reference pattern are 32 bits in length, then a threshold setting of 32 requires a perfect match with no false alarms. However, a threshold of 32 does not permit a single bit error. Most systems are required to be tolerant of a small number of errors. Therefore, a threshold of 31 provides a bit error tolerance of about 3%. Although the probability of detection increases, the probability of a false alarm increases as well.

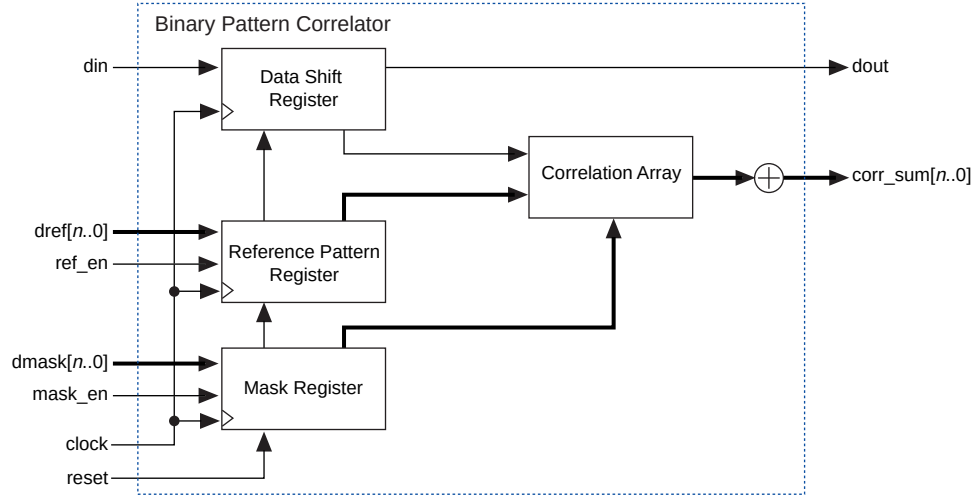
Modifiable Parameters

Nova Engineering will customize the megafunction's length and width at no additional cost. Customizing the data widths optimizes the megafunction for specific applications.

Block Diagram

Figure 20 shows the block diagram for the binary pattern correlator megafunction.

Figure 20. Binary Pattern Correlator Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	236	0	68 MHz	Contact Nova Engineering
EPF6016	-2	236	–	32 MHz	Contact Nova Engineering

Numerically Controlled Oscillator

Vendor: Altera
Target Application: Demodulation, frequency synthesis, cable communications

- Real or complex outputs
- Direct or calculated outputs
- Optimized for FLEX 10K devices
- User parameterized

MegaCore™

Preliminary Information

General Description

Numerically controlled oscillators (NCOs) are found in many applications, such as demodulation, frequency synthesis, and up/down conversion. The NCO function is fully parameterized, allowing the user to optimize the NCO for their system requirements. The NCO uses very few logic resources and memory blocks, depending on the parameters selected. Because the function uses memory, it is specific to the Altera APEX 20K and FLEX 10K devices.

The NCO function is capable of high-speed operation—over 130 MHz input frequency—supporting a bandwidth of 65 MHz. It can calculate up to 2,048 points per component, with up to a 17-bit output amplitude. Any size of phase accumulator can be specified. A 1/4 wave mode allows the NCO function's ROM to represent a larger number of points than would typically be supported by memory found on board the PLD.

Modifiable Parameters

The following megafunction parameters can be modified:

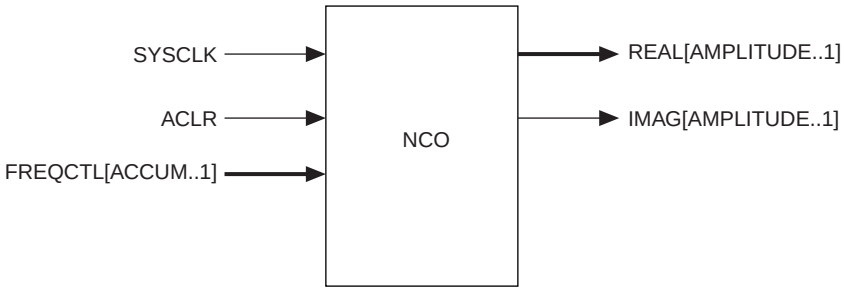
Modifiable Parameters

Parameter	Description
TYPE	Direct (full wave table), CALCULATED (1/4 wave table).
OUTTYPE	REAL or COMPLEX.
PIPELINED	YES – Pipelined memory access.
ACCUMULATOR	Phase accumulator precision.
PHASE	2^{PHASE} – Number of points in component.
AMPLITUDE	Output precision of each component.

Block Diagram

Figure 21 shows the block diagram for the NCO megafunction.

Figure 21. NCO Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	10	1	110 MHz	DIRECT, REAL, ACCUMULATOR = 8, PHASE = 8, AMPLITUDE = 8
		20	2	88 MHz	DIRECT, REAL, ACCUMULATOR = 20, PHASE = 9, AMPLITUDE = 12
		16	2	108 MHz	DIRECT, REAL, ACCUMULATOR = 8, PHASE = 8, AMPLITUDE = 8
		24	4	130 MHz	CALCULATED, REAL, ACCUMULATOR = 24, PHASE = 10, AMPLITUDE = 9
		32	1	88 MHz	DIRECT, REAL, ACCUMULATOR = 22, PHASE = 11, AMPLITUDE = 14
		33	2	134 MHz	CALCULATED, REAL, ACCUMULATOR = 24, PHASE = 10, AMPLITUDE = 12
		32	2	87 MHz	CALCULATED, REAL, ACCUMULATOR = 24, PHASE = 10, AMPLITUDE = 12
		44	4	98 MHz	CALCULATED, REAL, ACCUMULATOR = 32, PHASE = 11, AMPLITUDE = 17

Numerically Controlled Oscillator

Vendor: Nova Engineering
Target Application:
DDS for up/down frequency conversion, frequency hopping systems, DFTs, polar to rectangular conversion, digital modulation/ demodulation
Additional Deliverables:
Simulation files
ID Code: 66A3-F201

- Simultaneous quadrature outputs
- Parameterized phase accumulator width and output data width
- Optimized for the APEX 20K and FLEX 10K device architectures
- Ideal for the following functions:
  - Direct digital synthesizers
  - Frequency hopping systems
  - Discrete Fourier transforms
  - Modulators/demodulators
  - Polar-to-rectangular conversion

General Description

The NCO megafunction from Nova Engineering generates digital sine and cosine waveforms at a programmable periodic rate. The sine and cosine outputs can be adjusted over a wide range of frequencies with a high degree of resolution. Nova Engineering can customize the input and output data width to meet user specifications.

Functional Description

The NCO megafunction contains sine and cosine look-up tables (LUTs) that perform the following functions:

$$\sin(n) = \sin(2\pi n/N)$$
$$\cos(n) = \cos(2\pi n/N)$$

where: n = Address input to the LUT
N = Number of samples in the LUT
$\sin(n)$ = Amplitude of sine wave at $(2\pi n/N)$
$\cos(n)$ = Amplitude of cosine wave at $(2\pi n/N)$

Incrementing n from 0 to N causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The value $2\pi n/N$ represents a fractional phase angle between 0 and 2π. The time (t) required to increment n from 0 to N is the period of the sine and cosine waveforms produced by the NCO megafunction.

The LUT address is incremented once each system clock cycle by an amount equal to the `phase[`*m*`..0]` input. The phase angle data is accumulated and stored in the phase accumulator register. The output of the phase accumulator register is used to address the LUTs.

The frequency (f) of the system clock (f_{CLK}) is fixed. Therefore, the frequency of the sine and cosine waves is:

$$f = 1/t = f_{CLK} \times \texttt{phase}[m..0]/2^{(m+1)}$$

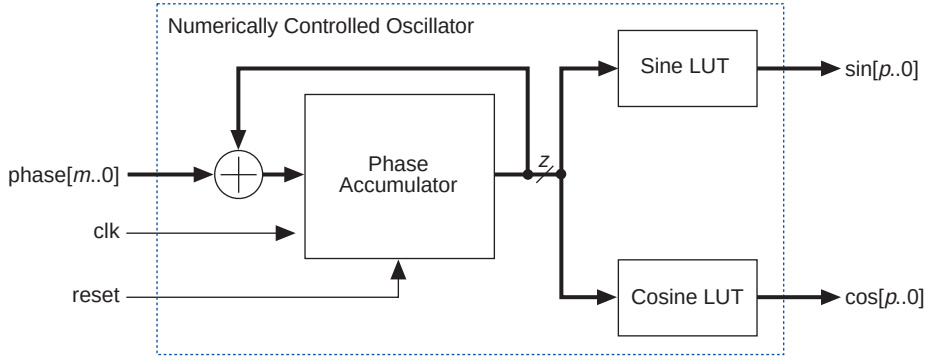
Modifiable Parameters

Nova Engineering will customize the phase accumulator and output data widths to user specifications at no additional charge. Customizing the width optimizes the megafunction for specific applications.

Block Diagram

Figure 22 shows the block diagram for the NCO megafunction.

Figure 22. NCO Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-1	60	2	97 MHz	Phase accumulator width = 24 bits, output data width of 8 bits

QPSK Equalizer

Vendor: Integrated Silicon Systems
Target Application: Satellite communications
Additional Deliverables: VHDL testbench, MATLAB files
ID Code: C38B-1123

- Fast speed 61 MHz
- Easy to use
- Parameterizable

General Description

The QPSK equalizer megafunction is composed of two channels (I and Q), with one channel per device. Each channel has been implemented as a 7-tap FIR filter, where the coefficients are updated using the LMS algorithm. All operations perform at the symbol rate, except the coefficient update, which is performed every 12 clock cycles.

All the input and output words for the 7-tap LMS FIR filter megafunction are bit-parallel and all the signals are active high.

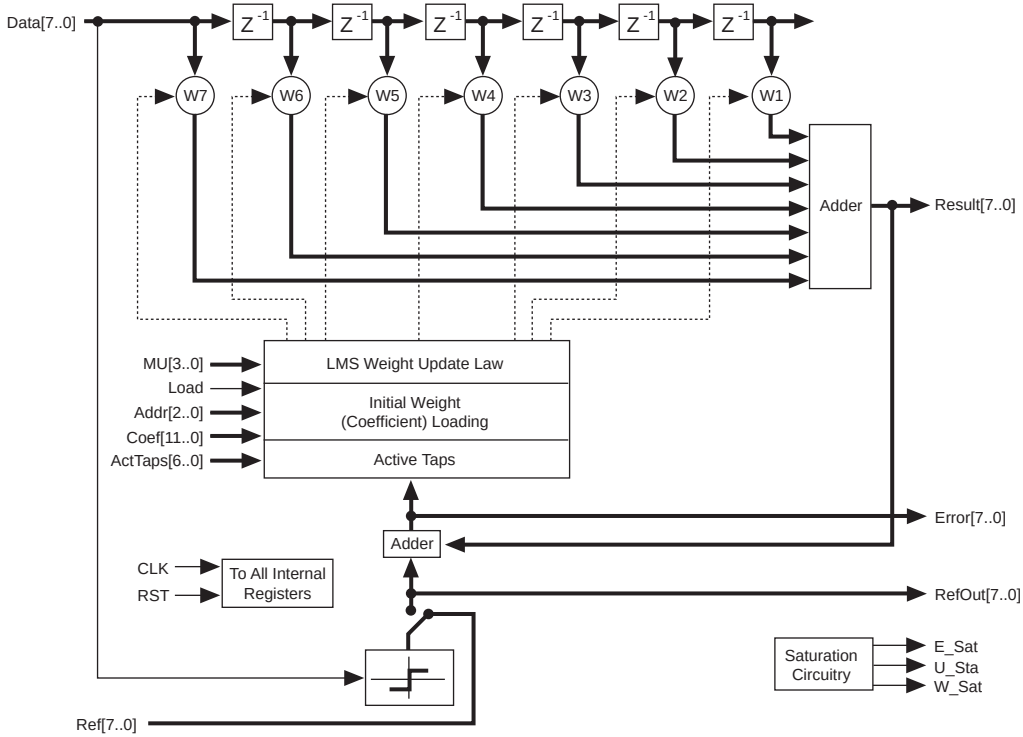
The update operation is based on the LMS algorithm shown below:

$$W_{k+1} = W_k + \mu e_k x_k$$

Block Diagram

Figure 23 shows the block diagram for one 7-tap LMS filter megafunction.

Figure 23. QPSK Equalizer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,500	0	61 MHz	Contact ISS

Digital Modulator

Vendor: Nova Engineering
Target Application: Amplitude modulators, frequency modulators, phase modulators, and up/down frequency conversion
Additional Deliverables: Simulation files
ID Code: 66A3-F301

- Optimized for the Altera APEX 20K and FLEX 10K device architectures
- Parameterized complex multiplier/mixer
- Parameterized quadrature output NCO
- Configurable phase accumulator within the NCO
- Configurable phase offset input port
- Applications:
  - Amplitude modulation (AM)
  - Frequency modulation (FM)
  - Phase modulation (PM)
  - Down converters
  - Direct digital synthesis

General Description

The digital modulator megafunction from Nova Engineering contains a parameterized complex multiplier/mixer and quadrature output NCO. The NCO is a LUT that has a quadrature output, phase accumulator, and phase offset input port. The complex multiplier/mixer multiplies two user-defined inputs with the NCO outputs for amplitude modulation or frequency down conversion.

Functional Description

The NCO contains sine and cosine LUTs that generate digital sine and cosine waveforms at a periodic rate. The LUTs perform the following functions:

$F_1[n] = \sin[2\pi n/N]$
$F_2[n] = \cos[2\pi n/N]$

where: n = Address input to the LUT
N = Number of samples in the LUT
$F_1[n]$ = Amplitude of sine wave at $[2\pi n/N]$
$F_2[n]$ = Amplitude of cosine wave at $[2\pi n/N]$

Incrementing n from 0 to N causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The value $2\pi n/N$ represents a fractional phase angle between 0 ($n = 0$) and 2π ($n = N$). The time (t) required to increment n from 0 to N, is the period of the sine and cosine waveforms produced by the NCO. Moreover, an m-bit `phase` input generates the addresses for the quadrature NCO. The LUT address increments once each system clock cycle by an amount equal to the `phase` input. The LUT address, or phase angle, is accumulated and stored in the phase accumulator register. The register's output is used to address the sine and cosine LUTs.

The frequency (f) of the system clock (f_{CLOCK}) is fixed. Therefore, the frequency of the sine and cosine waves produced by the NCO is:

$$f = 1/T = (f_{CLOCK} \times \texttt{phase}) \ / \ 2^{(m+1)}$$

where: `phase` = Input phase angle

The `phase_offset` input modulates the NCO phase angle. The value from the `phase_offset` input is summed with the phase accumulator output. Both values, as well as the sum, are represented in two's complement format.

The complex multiplier/mixer can multiply two complex numbers represented in two's complement format. It uses a parallel-pipelined architecture that provides maximum speed. The complex multiplier/mixer performs the following function:

$$\texttt{real} + j\texttt{imag} = (\texttt{a} + j\texttt{b}) \times (\texttt{c} + j\texttt{d})$$

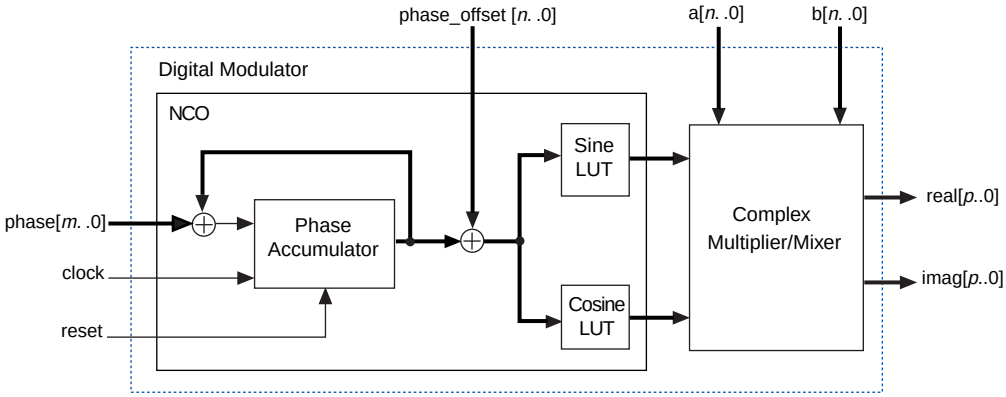
where: $j = \sqrt{(-1)}$
$\texttt{real} = (\texttt{a} \times \texttt{c}) - (\texttt{b} \times \texttt{d})$
$\texttt{imag} = (\texttt{a} \times \texttt{d}) + (\texttt{b} \times \texttt{c})$

The total latency of the modulator from the `phase` input to the `real` output is 6 clock cycles. The output of the complex multiplier/mixer is registered to improve speed without increasing the number of logic cells used.

Block Diagram

Figure 24 shows the block diagram for the digital modulator megafunction.

Figure 24. Digital Modulator Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	674	2	71 MHz	24-bit accumulator, 10-bit phase offset, 8-bit complex multiplier, and 8-bit quadrature outputs

Complex Multiplier/Mixer

Vendor: Nova Engineering
Target Application: Digital mixers, modulators/demodulators, discrete Fourier transforms (DFT), complex arithmetic, wireless communications systems
Additional Deliverables: Prototype board, simulation files
ID Code: 66A3-F101

- Parallel implementation for maximum speed
- Parameterized data width
- Optimized for the Altera FLEX 10K and FLEX 8000 device architectures
- Ideal for the following applications:
  - Digital mixers
  - Discrete Fourier transforms
  - Modulators/demodulators
  - Complex arithmetic
  - Wireless telecommunication systems

General Description

The complex multiplier/mixer megafunction from Nova Engineering can multiply two complex numbers or mix two complex signals. This function can be used for vector cross products, vector dot products, up/down frequency conversion, differential phase detection, digital amplitude modulation (AM), and quadrature amplitude modulation (QAM). Nova Engineering will customize the input width, output width, and processing latency of the complex multiplier/mixer megafunction at no additional cost.

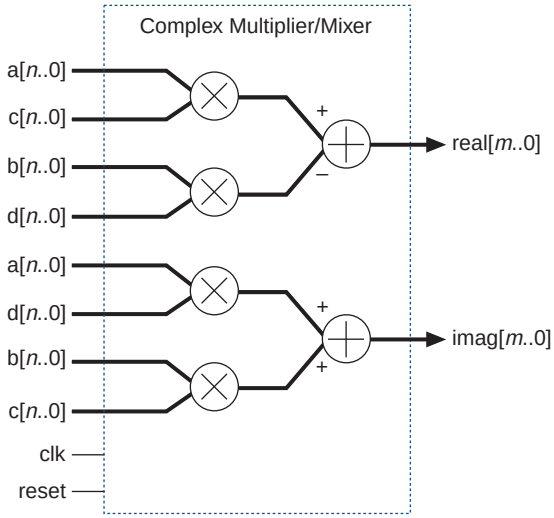
Functional Description

The complex multiplier/mixer megafunction is a parallel and pipelined architecture that provides maximum speed. The function's internal and external operations are synchronized to the rising clock edge, and an asynchronous `reset` input is provided for initializing all internal registers.

Block Diagram

Figure 25 shows the block diagram for the complex multiplier/mixer megafunction.

Figure 25. Complex Multiplier/Mixer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	604	0	83 MHz	8 × 8 complex multiplier with a three-clock latency
EPF6016	-2	608	0	47 MHz	

Early/Late-Gate Symbol Synchronizer

Vendor: Nova Engineering
Target Application:
Digital receivers,
synchronous data interfaces
Additional Deliverables:
Simulation files
ID Code: 66A3-F601

- Complete closed-loop synchronizer
- Variable loop filter bandwidth
- Balanced gate/dual integrator design
- Optimized for the Altera APEX 20K, FLEX 10K, and FLEX 8000 device architectures
- Applications
  - Digital receivers
  - PLLs

General Description

The early/late gate synchronizer megafunction contains all the functions necessary for a complete, first-order, closed-loop synchronizer. The synchronizer includes a phase detector, an up-down counter loop filter, and a digitally controlled oscillator (DCO). The phase detector is a balanced early/late gate, dual integrator design. The output of the phase detector is the difference, or phase error, between the data clock and the input data stream. The phase error (θ_e) output from the phase detector is accumulated in an up-down counter, which increments and decrements according to the sign and magnitude of the phase error.

The DCO advances or retards the phase of the locally generated data clock whenever the error accumulator exceeds a specified error threshold. The error threshold is programmable and is used to control the bandwidth of the loop filter. The loop bandwidth can be narrowed by increasing the error threshold and widened by decreasing the error threshold. Small error thresholds allow the filter to respond to rapid changes in the phase error.

The DCO also adjusts the phase of the locally generated data clock in programmable step sizes. The step size, or magnitude, of the phase adjustment determines the loop acquisition time and data clock jitter. Large step sizes can be used to minimize acquisition times, since large phase steps can quickly correct large phase errors. Small step sizes can be used to minimize clock jitter when the loop is locked.

Functional Description

The phase detector requires a high-speed clock to sample the input binary data stream. The sampling clock must be an even multiple of the data rate and is typically 16 times the data rate (i.e., `ratio[7..0]` = 16).

The relationship between the data and sampling clocks is described below:

$$T_{data\_clk} = \texttt{ratio[7..0]} \times T_{sample\_clk}$$

where: T_{sample_clk} = Period of the sample clock
T_{data_clk} = Period of the data clock
`ratio[7..0]` = Even integer between 4 and 254

A master counter generates the data clock and the early and late gate timing pulses. The early timing gate enables one accumulator to integrate the energy in the incoming signal during the first half of the symbol period. The late timing gate enables a second accumulator to integrate the signal energy during the second half of the symbol period. The total accumulator integrates the signal energy during the entire symbol period. The total accumulator determines whether the data bit was a binary one or zero, and adjusts the sign of the phase error appropriately. Assuming transitions in the data, the difference between the early and late gate integrators is proportional to the receiver phase error (θ_e). The phase detector output is defined as follows:

$$\theta_e = |S_{early}| - |S_{late}|$$

where: $|\Sigma_{early}| \leq \frac{ratio[7..0]}{2}$ and $|\Sigma_{late}| \leq \frac{ratio[7..0]}{2}$

The phase error is accumulated until:

$$|\Sigma\theta_e| > \texttt{error\_thresh[15..0]}$$

The DCO advances or retards the phase of the data clock whenever the accumulated error exceeds the programmed error threshold. The direction of the phase adjustment is determined by the sign of the accumulated phase error, while the magnitude of the correction is determined by the value programmed into `step_size[7..0]`.

Phase corrections, or phase steps, by the DCO can be represented in degrees or fractional cycles of the data clock. The following equation demonstrates how to calculate the phase step in degrees:

$$\text{phase step} = \frac{\text{step - size}[7..0]}{ratio[7..0]} \times 360^{\circ}$$

The step_size[7..0] value should always be very small in relation to the ratio[7..0] value. Phase corrections greater than the ratio[7..0] value will make the loop unstable. The step_size[7..0] value should also be greater than zero, except when no phase corrections are desired. Setting the step_size[7..0] value to zero is equivalent to disabling the synchronizer.

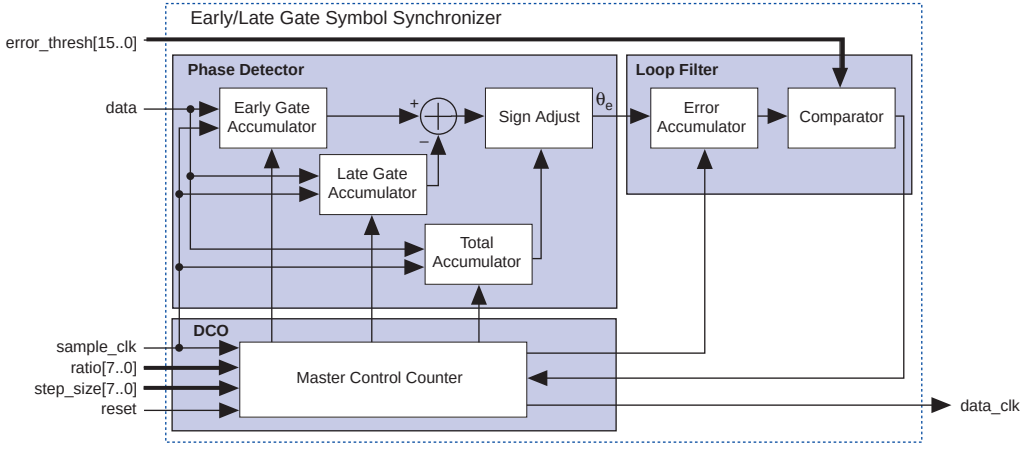
The timing jitter, caused by phase adjustments to the data clock, can be calculated with the following equation:

timing jitter = step_size[7..0] × T_{sample_clk}

Block Diagram

Figure 26 shows the block diagram for the early/late-gate symbol synchronizer megafunction.

Figure 26. Early/Late-Gate Symbol Synchronizer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	260	0	71 MHz	Contact Nova Engineering

fft Fast Fourier Transform

Vendor: Altera
Target Application: DSP systems
Additional Deliverables: fft Fast Fourier Transform Data Sheet
Ordering Code: PLSM-FFT

MegaCore™

- Optimized for the Altera APEX 20K and FLEX 10K device architectures
- Complex data in and data out decimation-in-frequency (DIF) fast Fourier transform (FFT)
- Dual memory architecture
- Flexible memory interface—data and twiddle memory elements can be implemented in internal and/or external RAM
- Significantly faster than DSP processor solutions
- Parameterized data width, twiddle width, and number of points
- Block-floating point notation to provide optimal accuracy

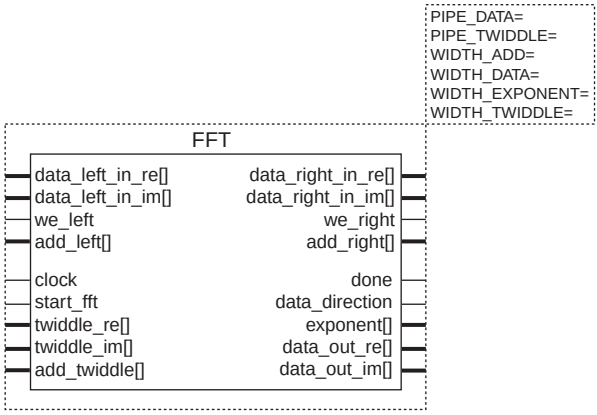
General Description

The Altera `fft` MegaCore function implements a DIF algorithm, and contains all the logic functions necessary to implement an FFT algorithm. The memory configuration and I/O interface can be configured by the designer for optimum flexibility.

To optimize throughput, the `fft` MegaCore function uses a dual memory architecture that consists of the right and left memory banks. The dual memory architecture allows data to be read from one memory bank and written to another memory bank.

The `fft` MegaCore function also uses a third memory, known as the twiddle memory bank, that is kept separate from the right and left memory banks to maximize throughput. Figure 27 shows the symbol for the `fft` MegaCore function.

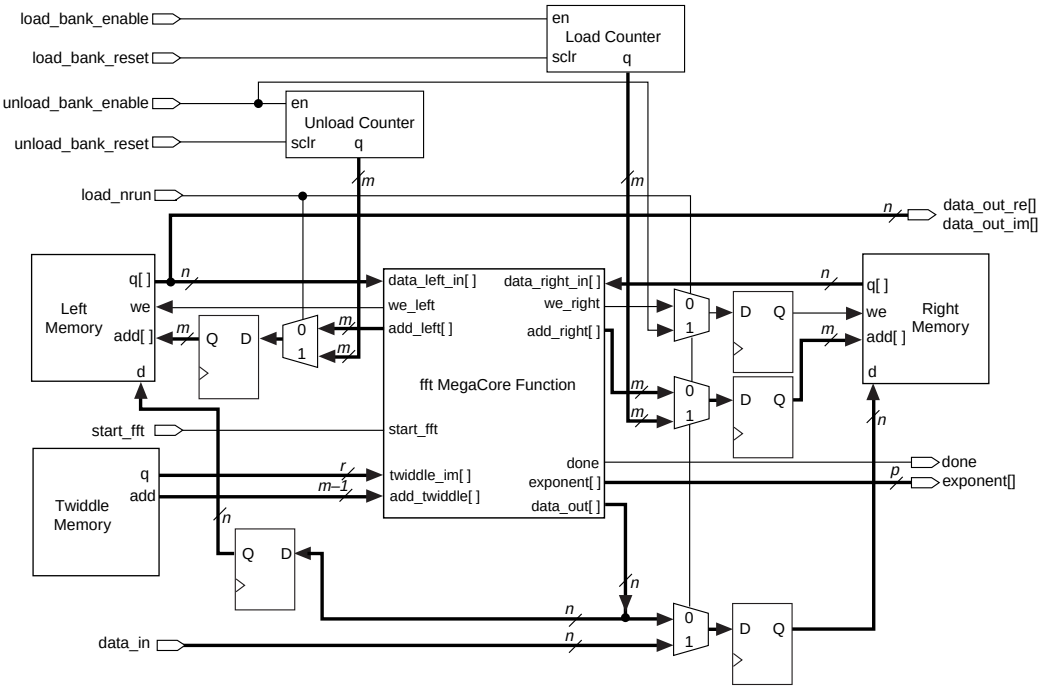
Figure 27. fft Symbol



Functional Description

Figure 28 shows a block diagram of an example system implementation that uses the `fft` MegaCore function and additional logic in a FLEX 10K device. The designer can choose from a variety of memory and I/O interface options. The implementation shown in Figure 28 has on-chip RAM, an odd number of passes (i.e., an odd number of address bits), and no data buffering. The right, left, and twiddle memory elements are all implemented in FLEX 10K embedded array blocks (EABs). After new data is loaded into the right memory bank, the `fft` function can sequentially process data. The `fft` function cannot process data while new data is being loaded into the right memory bank. When the `fft` function is not processing data, new data can be loaded and unloaded simultaneously from both the right and left memory banks.

Figure 28. Block Diagram of a System Implementation with an fft MegaCore Function



where: $n = 2 \times$ WIDTH_DATA
$m =$ WIDTH_ADD
$p =$ WIDTH_EXPONENT
$r =$ WIDTH_TWIDDLE

FFT/IFFT High Performance 64-Point

Vendor: Integrated Silicon Systems
Target Application: Signal processing systems
Additional Deliverables: VHDL testbench, test vector generation files, functional VHDL simulation model
ID Code: C38B-1114

- High performance
- No external memory required
- Easy to use

General Description

The ISS high performance 64-point FFT/IFFT megafunction, FFT64HP, performs forward or inverse fast Fourier transform (FFT) functions on complex data containing 64 points according to the equations below:

$$\text{FFT:} \quad Y(k) = \frac{1}{16}\sum_{n=0}^{63} X(n) W_{64}^{-nk} \quad , k = 0, 1, 2, \ldots 63 \qquad [1]$$

$$\text{IFFT:} \quad Y(k) = \frac{1}{16}\sum_{n=0}^{63} X(n) W_{64}^{nk} \quad , k = 0, 1, 2, \ldots 63 \qquad [2]$$

Data is loaded into the workspace RAM in normal sequential order. The transformed data comes out from the function in radix-4 digitally-reversed order with the index indicated by output `QIX`.

Functional Description

The FFT64HP megafunction is based on the radix-4 decimation in frequency (DIF) algorithm. It performs the computation concurrently in three highly pipelined cascaded stages, as illustrated in Figure 29. The FFT64P megafunction is capable of processing continuous input data and contains all the necessary circuits to support this continuous processing.

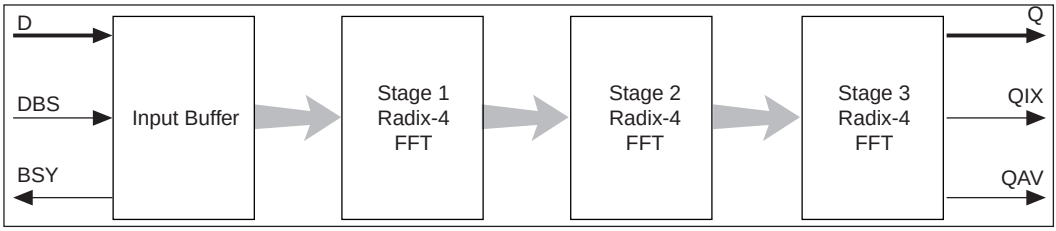
The internal complex programmable logic device (CPLD) memory is utilized and the whole circuit is on a single device. Both the input and output are complex numbers in the two's complement format. The input wordlength is 9 bits and the output wordlength is 12 bits. The twiddle factors and internal commutation data wordlengths are 12 bits.

The function can accept continuous input data, i.e., a 64-point data block every 64 clock cycles. When clocked at 54 MHz, the function achieves continuous computation speed of approximately 1.19 ms. The computation has a latency of 174 clock cycles.

Block Diagram

Figure 29 shows the block diagram for the FFT64HP megafunction.

Figure 29. FFT64HP Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100ARC	-1	3,963	12	13.88 ns, 72 MHz	Contact ISS

FFT/IFFT Low Latency 64-Point

Vendor: Integrated Silicon Systems
Target Application: Signal processing systems
Additional Deliverables: VHDL testbench, test vector generation files, functional VHDL simulation model
ID Code: C38B-9001

- Low latency
- No external memory required
- Easy to use

General Description

The ISS low latency 64-point FFT megafunction, FFT64LL, performs forward or inverse fast Fourier transform (FFT) functions on complex data containing 64 points according to the equations below.

$$\text{FFT:} \quad Y(k) = \frac{1}{16}\sum_{n=0}^{63} X(n) W_{64}^{-nk} \quad , k = 0, 1, 2, \ldots 63 \qquad [1]$$

$$\text{IFFT:} \quad Y(k) = \frac{1}{16}\sum_{n=0}^{63} X(n) W_{64}^{nk} \quad , k = 0, 1, 2, \ldots 63 \qquad [2]$$

Functional Description

The FFT64LL megafuntion performs decimation in frequency (DIF), radix-4 digitally reversed order, and forward or inverse FFT on complex data. Data is loaded into the its workspace RAM in normal sequential (natural) order. The transformed data comes out from the function in radix-4 digitally-reversed order with the index indicated by output `QIX`.

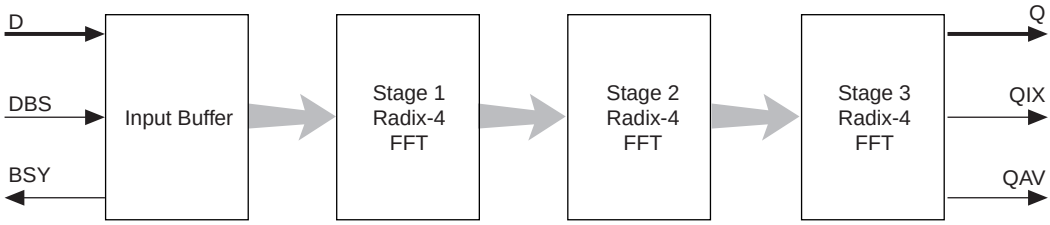
The internal CPLD memory is utilized and the whole circuit is on a single device. Both the input and output are complex numbers in the two's complement format. The input wordlength is 9 bits and the output wordlength is 12 bits. The twiddle factors and internal commutation data wordlengths are 12 bits.

The function can accept a 64-point data block every 112 clock cycles. When clocked at 54 MHz with a data block fed every 112 clock cycles, the function achieves a computation speed of approximately 2.08 ms. The computation has a latency of 88 clock cycles. See Figure 30.

Block Diagram

Figure 30 shows the block diagram for the FFT64LL megafunction.

Figure 30. FFT64LL Megafunction Block Diagram

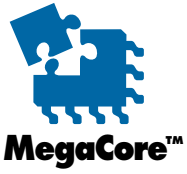


Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-1	3,674	12	15.62 ns, 64 MHz	Contact ISS

FFT Processor

Vendor: Altera
Target Application: Wireless communications, voice recognition, spectrum analysis, noise analysis
Additional Deliverables: FFTCHIPA and FFTCHIPB reference designs



Preliminary Information

- High performance
- High accuracy
- FFT and IFFT processing
- User parameterized

General Description

The FFT processor is a high performance, parameterized complex in/complex out megafunction for programmable logic. The megafunction implements a mixed radix (4 and 2) processing function, along with an automatically generated control unit. Any Radix-2 length FFT can be chosen.

Two reference designs are also included: FFTCHIPA and FFTCHIPB. These reference designs detail the memory and user interface for the FFT processor, for on-board or off-board memory, respectively. As the FFT processor can be interfaced to memory off of the device, the function can be compiled to both Altera FLEX 10K and FLEX 6000 devices.

For maximum accuracy, wordgrowth and precision are carefully managed during processing. Full internal precision is maintained during butterfly operations. The block floating point section is used to maximize dynamic range. For a random complex input to a 8,192-point, 16-bit FFT, the average error is about 1.5 bits.

The maximum clock frequency of the FFT is dependent on precision and device speed grade. For 12-bit precision, 50 MHz can be expected in FLEX 10KA-3 devices, and up to 80 MHz in FLEX 10KE-1 devices.

A set of MATLAB programs is included to transfer MATLAB vectors to and from the Altera MAX+PLUS II simulation environment. This transfer allows the accuracy of the megafunction to be precisely tested.

Modifiable Parameters

The following megafunction parameters can be modified:

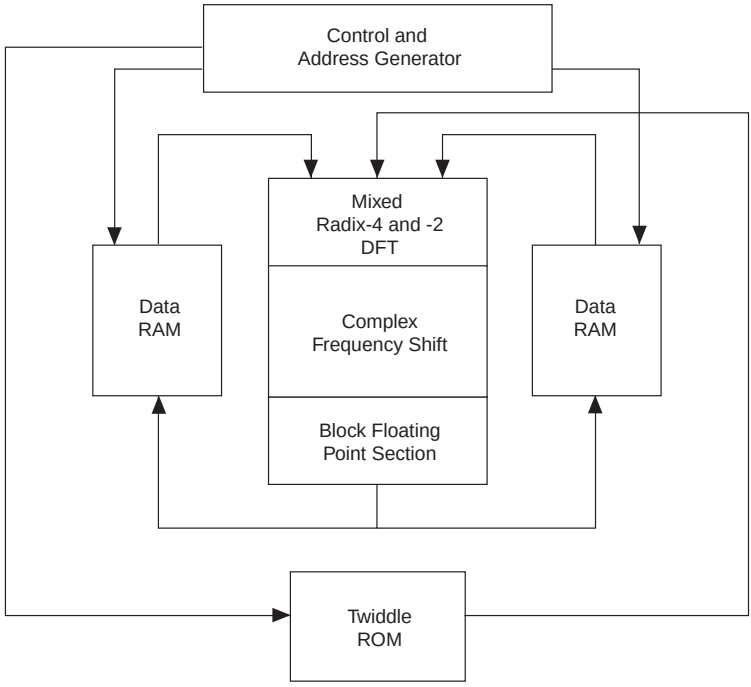
Modifiable Parameters

Parameter	Description
POINTS	Number of points in the FFT.
DATAWIDTH	Precision of the input and result data.
TWIDDLEWIDTH	Precision of the twiddle factors.
FLOATWIDTH	Precision of the block floating foint exponent.
INTERFACE	Modifies processing pipeline for internal and external memory accesses.

Block Diagram

Figure 31 shows the block diagram for the FFT processor megafunction.

Figure 31. FFT Processor Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	1,101	0	80 MHz	DATAWIDTH = 8, TWIDDLEWIDTH = 8
		1,950	0	75 MHz	DATAWIDTH = 12, TWIDDLEWIDTH = 12
		2,900	0	65 MHz	DATAWIDTH = 12, TWIDDLEWIDTH = 12

RGB2YCrCb & YCrCb2RGB Color Space Converters

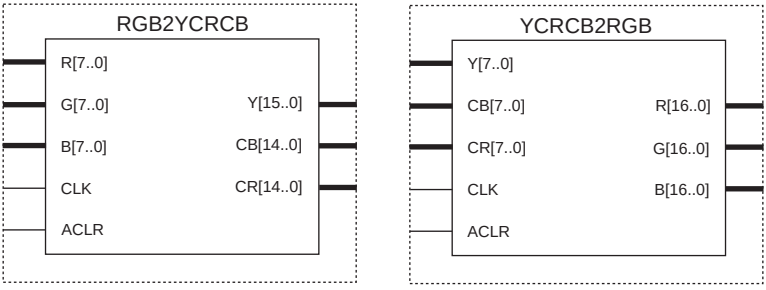
Vendor: Altera
Target Application: DSP, video imaging, HDTV, set-top boxes
Additional Deliverables: RGB2YCrCb & YCrCb2RGB Color Space Converters Data Sheet
Ordering Code: PLSM-CSC

- 24-bit RGB2YCrCb and YCrCb2RGB color space conversion
- High-speed operation (100 MHz)
- Full precision outputs: rounding and saturation can be performed with the `round` and `saturate` reference designs
- Useful for a variety of applications, including image filtering, machine vision, and digital video
- Optimized for APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 device architectures

General Description

The `RGB2YCrCb` and `YCrCb2RGB` color space converter MegaCore functions convert digital video colors to television broadcast signal colors and vice-versa. The functions are useful for a number of image processing and filtering operations. The `RGB2YCrCb` function converts red-green-blue (RGB) color space to the YCrCb (intensity-color red-color blue) color space; the `YCrCb2RGB` function performs the inverse operation. Figure 32 shows the symbols for the `RGB2YCrCb` and `YCrCb2RGB` functions.

Figure 32. RGB2YCrCb & YCrCb2RGB Symbols



Functional Description

The `RGB2YCrCb` function uses the following equations when converting gamma-corrected RGB data to YCrCb data:

$$Y' = 0.257R' + 0.504G' + 0.098B' + 16$$
$$Cr = 0.439R' - 0.368G' - 0.071B' + 128$$
$$Cb = -0.148R' - 0.291G' + 0.439B' + 128$$

The `YCrCb2RGB` function uses the following equations when converting YCrCb data to RGB data:

$$R' = 1.164(Y' - 16) + 1.596(Cr - 128)$$
$$G' = 1.164(Y' - 16) - 0.813(Cr - 128) - 0.392(Cb - 128)$$
$$B' = 1.164(Y' - 16) + 2.017(Cb - 128)$$

Because the inputs are multiplied by constant values, the LUT architecture of FLEX 10K and FLEX 8000 devices is ideal for efficiently performing the conversion equations.

Discrete Cosine Transform

Vendor: Integrated Silicon Systems
Target Application: Multimedia systems, set-top boxes, video telephony systems, broadcast systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-A263

- Fully parameterized megafunction
- Discrete cosine transform (DCT), inverse discrete cosine transform (IDCT), and combined DCT/IDCT variants available
- High performance
- Implements an 8 × 8 two-dimensional (2-D) DCT conforming to many image compression standards

General Description

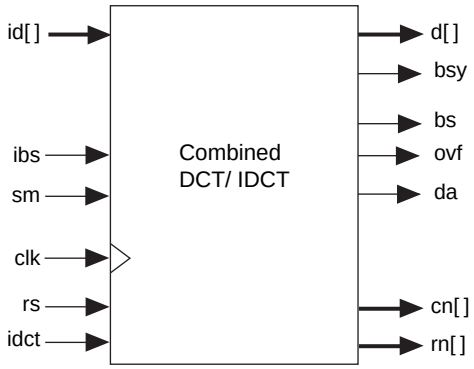
The DCT and IDCT megafunctions operate at sample rates of up to 50 MHz, and are fundamental building blocks for many image and video compression systems. Additional functionality ensures that the megafunctions are easy to use and reduces the need for extra circuitry. Parameter selection enables the megafunctions to comply with the following standards: H.261, H.263, Joint Photographic Experts Group (JPEG), MPEG-1, MPEG-2, and MPEG-4.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 33 shows the block diagram for the DCT megafunction.

Figure 33. DCT Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-3	4,386	0	17.45 MHz	8 × 8, 2-D DCT with 8-bit inputs, 8-bit outputs, 8-bit coefficient word lengths, and 12-bit internal precision

Multi-Standard ADPCM

Vendor: Integrated Silicon Systems
Target Application: Overload voice channels in digital circuit multiplication equipment (DCME), data modems for DCME, packetized voice protocol (PVP) systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-AD4E

- Compliant with G.721, G.723, G.726, G.726a, G.727, and G.727a ITU standards
- Coding 64 Kbits/second to and from 40, 32, 24, and 16 kbits/second
- Support for both A- and Mu-law pulse-code modulation (PCM) coding
- Support for up to 20 full duplex channels, and 40 encode or decode channels
- Optimized for FLEX 10K device architectures

General Description

The adaptive pulse code modulation (ADPCM) megafunction performs multi-channel duplex ADPCM coding in telecommunications applications. Most of the applications of the G.726 standard are in overload channel communication, i.e., carrying voice and data modem signals in DCME, particularly for modems operating in excess of 4,800 kbits per second. Most of the applications of the G.727 standard are in converting A- and µ-law PCM channels to and from variable-rate embedded ADPCM channels. The primary use of the megafunction in the G.727 and G.726 standard is for packetized speech systems, operating in accordance with the packetized voice protocol (PVP).

The ADPCM megafunction, which is optimized for the Altera FLEX 10K architecture, combines the algorithm and architecture research of ISS with the performance and implementation advantages of the FLEX 10K family. The ADPCM megafunction is designed in a hierarchical manner to enable the high-quality implementation achieved in the lower-level blocks, such as multipliers and adders, to be carried through to the higher-level encoder and decoder blocks.

The megafunction ensures that products incorporating ADPCM can be delivered to market quickly and efficiently, and is parameterized to meet the target application operating requirements. The megafunction can be utilized for multi-channel encoding, multi-channel decoding, and multi-channel duplex coding.

The multi-standard ADPCM megafunction's functionality and timing are verified using ITU standard test sequences. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 34 shows the block diagram for the multi-standard ADPCM encoder megafunction.

Figure 34. Multi-Standard ADPCM Encoder Megafunction Block Diagram

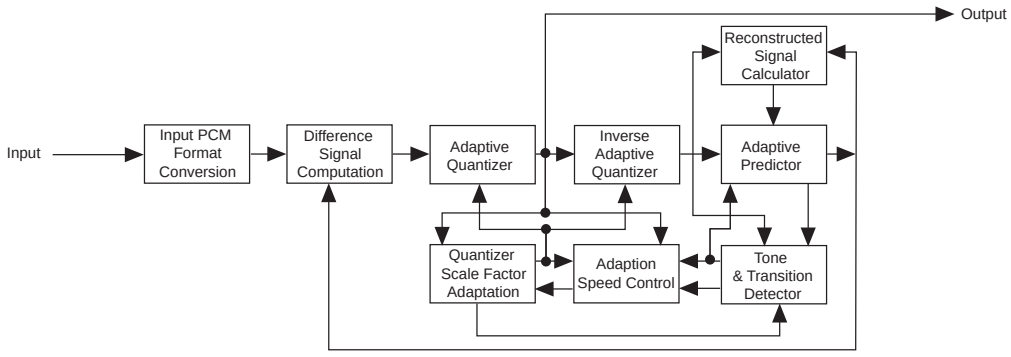
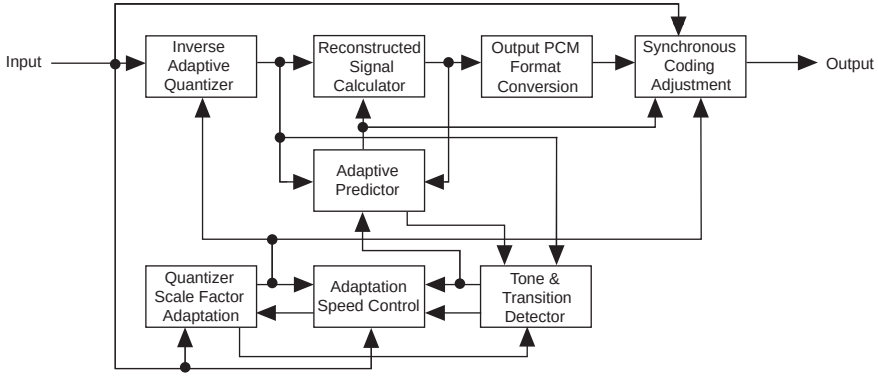


Figure 35 shows the block diagram for the multi-standard ADPCM decoder megafunction.

Figure 35. ADPCM Decoder Block Diagram



When instantiating the ADPCM megafunction, the control bits can be used to select the desired coding rate. Depending on the coding rate selected, the function may use less logic. The Altera software automatically minimizes the design, removing any unused logic.

The G.726 standard is a fixed ADPCM algorithm for conversion to and from 64 kbits per second and 40, 32, 24, and 16 kbits per second. The algorithms of the G.727 standard quantize the signal into function and enhancement bits. The function bits are used for precision while the enhancement bits are used to reduce the quantization noise in the reconstructed signal. The function bits must reach the decoder, but the enhancement bits can be discarded to alleviate congestion. (The G.726a and G.727a represent modifications to the standards.)

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	3,942	9	9 MHz	16 channels, full duplex coding with all standards and coding rates, and PCM laws

Image Processing Library

Vendor: Integrated Silicon Systems
Target Application: DSP for imaging, DSP for communications
ID Code: C38B-FFF2

- Wide range of front-end video and image processing megafunctions
- Parameterized level of pipelining, window sizes, and data word lengths and formats
- Option to use FLEX 10K embedded array blocks (EABs) as pixel line delays
- Real-time operation with pixel rates up to and including HDTV standard rate of 54 MHz

General Description

The image processing library includes the following front-end video and image processing megafunctions: edge detectors, image enhancement filters, matched filters, video convolvers, contrast enhancement filters, and median filters. These image processing megafunctions have been simplified to reduce the interface requirements and to enable the rapid generation of high quality, high functionality, real-time processing designs.

An image processing megafunction can use FLEX 10K embedded array blocks (EABs) to implement the required line delays for 2-D filtering applications. Also, several front-end image processing megafunctions can be incorporated in a single design, allowing developers to perform multiple processing tasks in real-time and to switch instantaneously between them. Contact ISS for the best parameter settings to meet specific application requirements.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	231	0	90 MHz	Contact ISS

Floating-Point Operator Library

Vendor: Integrated Silicon Systems
Target Application: Adaptive systems, safety-critical systems, flight control, flight guidance, scientific processing, overflow indicator
Additional Deliverables: VHDL testbench, OpenCore feature, VHDL RTL source code
ID Code: C38B-1112, C38B-1122, C38B-1121

- Programmable register length and initial value
- Automatic resizing and feedback selection (2 to 32 bits)
- Feedback architecture designed for maximum speed
- Multiple user-selectable configurations

General Description

Floating-point operation implementation in programmable logic is now easy with the ISS floating-point operator library, which consists of the following:

- *Floating-point adder*—Registrable output and optional pipeline cuts, both addends have the same exponent size.
- *Floating-point divider*—Using radix-2 SR 0 array. Default quotient value when in operation = 0/0.
- *Floating-point multiplier*—BooWtMult is used to achieve the fastest possible speed without introducing pipelining in mantissa processing.

Modifiable Parameters

The following megafunction parameters can be modified:

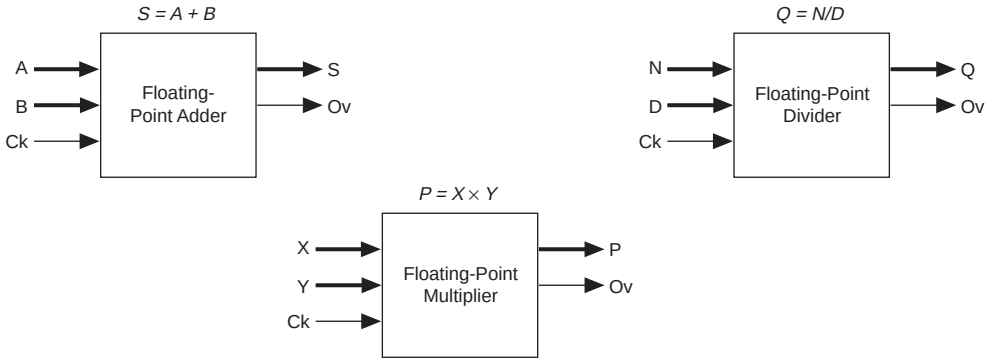
Parameter	Description
M	Mantissa size
E	Exponent size
P	Number of pipeline levels

Contact ISS directly for any required modifications.

Block Diagram

Figure 36 shows the block diagram for the floating-point operator library.

Figure 36. Floating-Point Operator Library Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	618	0	35 MHz	Floating-point adder (M = 16, E = 6, P = 3)
		785	0	37 MHz	Floating-point multiplier (M = 16, E = 6, P = 2)
		2,051	0	41 MHz	Floating-point divider (M = 16, E = 6, P = 6)

Digital IF Receiver

Vendor: Nova Engineering
Target Application: Narrowband and Wideband Digital Receivers
Additional Deliverables: Simulation files
ID Code: 66A3-F901

- Complete digital IF receiver
- Quadrature NCO and digital mixer translate intermediate frequency (IF) signal to baseband
- CIC and FIR filters provide decimation and filtering
- Standard processor bus interface supports programmable features
- High speed serial interface supports industry standard DSP processors

General Description

The digital IF receiver megafunction combines a quadrature NCO and a digital mixer to translate the input IF signal down to baseband. Multiple Cascaded Integrator Comb (CIC) filters and a FIR filter provide bandlimiting, decimation, and interpolation to accommodate a variety of signal bandwidths. The digital IF receiver is designed to accommodate 12-bit complex data including a total of six, 4th order CIC filters, two 64-tap programmable coefficient FIR filters, a quadrature NCO, and two digital mixers to process both the in-phase and quadrature signal components.

The digital IF receiver can reduce the bandwidth and sampling rate of DSP-based receivers by pre-selecting the signals of interest. The reduction in bandwidth and sampling rate can dramatically reduce the cost and complexity of the DSP system used for downstream demodulation or other signal processing.

The Digital IF Receiver megafunction allows the designer to lower the sampling rate of the system A/D converter and still directly sample a 70MHz IF. Through a signal processing technique known as IF under sampling, images of the desired signal are created at the sampling frequency. The digital IF receiver allows the bandwidth of interest to be selectively passed while other sampling artifacts are discarded.

The digital signal processing techniques, used in the digital IF receiver, avoid many of the undesirable effects associated with classic analog implementations. For example, digital filters do not require initial component tolerances, calibration, or preventive maintenance and do not suffer from temperature variations, or aging characteristics. Digital mixers also eliminate common analog degradations such as I/Q phase mismatch, amplitude imbalance, and DC offsets.

The FIR filters can store up to 8 different sets of coefficients. The coefficient set used by the FIR filters can be dynamically changed through the processor interface. In addition, the decimation and interpolation rates of the CIC filters can be controlled by through the processor interface.

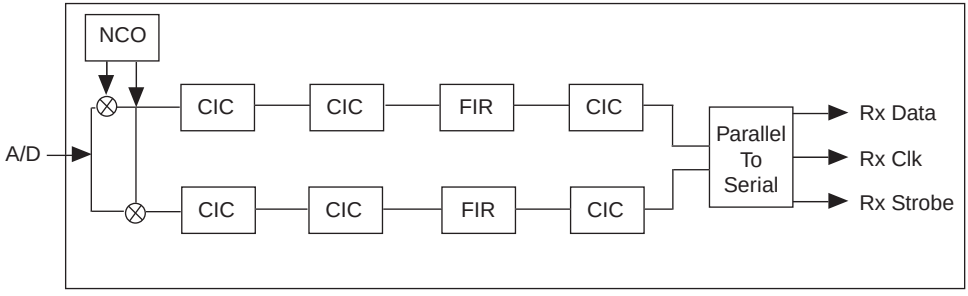
Modifiable Parameters

Nova Engineering will customize the FIR coefficients and the CIC decimation/interpolation rates at no additional charge. Custom coefficients and CIC rates optimize the performance of the digital IF receiver.

Block Diagram

Figure 37 shows the block diagram for the digital IF receiver megafunction.

Figure 37. Digital IF Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100E	-1	2,400	11	75 MHz, 25 MSPS	Input sampling rate

DSP Design Services (ACAP Partners)

The following table lists the ACAP partners who offer design services for DSP.

Partner	Expertise						Services						
	Error Detection & Correction	Filtering	Modulation/Demodulation	Control Loops	Signal Analysis/Transform	Imaging & Compression	IP Integration	Algorithm Optimization	Hardware Optimization	Software Development	Board Design	Prototype Development	Board Products
Advanced Logical Design, Inc. 12280 Saratoga-Sunnyvale Rd.#201 Saratoga, CA 95070 Tel. (408) 446-1004	✓			✓		✓	✓		✓	✓	✓	✓	
Applied Computing Technology, Inc. 1020F Commerce Park Drive Oak Ridge, TN 37830 Tel. (423) 220-0777	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	
Applied Microelectronics Inc. 1046 Barrington Street, Halifax Nova Scotia, Canada, B3H 2R1 Tel. (902) 421-1250 **Offering:** Experienced in algorithm, hardware, and embedded processor DSP developments.	✓	✓			✓		✓	✓	✓	✓	✓	✓	✓
BARCO SILEX Rue du Bosquet 7 1348 Louvain La Neuve Belgium Tel. (32) 10-45 49 04		✓	✓	✓		✓							
Bright Design Services 10436 NE 112th Street Seattle, WA 98033 Tel. (425) 576-1524	✓			✓		✓	✓		✓	✓	✓	✓	

Partner	Expertise						Services						
	Error Detection & Correction	Filtering	Modulation/Demodulation	Control Loops	Signal Analysis/Transform	Imaging & Compression	IP Integration	Algorithm Optimization	Hardware Optimization	Software Development	Board Design	Prototype Development	Board Products
Coded Solutions Pty Ltd 65 Johnston Street Annandale, NSW 2038 Australia Tel. (61) 2 9518 7011 **Offering:** Active developing JPEG modules.							✓		✓			✓	
Digital Design Solutions 6696 Fossil Creek Dr. Memphis, TN 38120 Tel. (901) 759-1802		✓							✓		✓	✓	✓
DMC Manufacturing, Inc. 7025 Central Highway Pennsauken, NJ 08109 Tel. (609) 665-5400 **Offering:** Experienced with design optimization and integration of the Altera design with the PCB design for performance, manufacturing, and testing.									✓		✓	✓	✓
Eberwein & Associates, Inc. 9449 Briar Forest, #507 Houston, TX 77063 Tel. (713) 784-1226	✓	✓		✓		✓		✓	✓	✓	✓	✓	✓
Gid'el Ltd. 14 Ein Ayyala ISRAEL 30825 Tel. (972)-6639-1708	✓			✓		✓	✓		✓	✓	✓	✓	

Partner	Expertise						Services						
	Error Detection & Correction	Filtering	Modulation/Demodulation	Control Loops	Signal Analysis/Transform	Imaging & Compression	IP Integration	Algorithm Optimization	Hardware Optimization	Software Development	Board Design	Prototype Development	Board Products
Innovative Configuration, Inc. (ICI) 712 via Palo Alto Aptos, CA 95003 Tel. (831) 688-6917 **Offering:** Multimedia oriented DSP.	✓	✓	✓	✓		✓	✓		✓	✓	✓	✓	
Intrinsix 33 Lyman St. Westboro, MA 01581 Tel. (508) 836-4100		✓			✓	✓	✓	✓	✓	✓	✓	✓	
I/O Consulting A/S Gaaseagervej 6 DK-8250 Egaa Tel. (45) 87 43 80 74					✓		✓	✓	✓	✓	✓	✓	✓
Locke's Digital Developments Ltd. New Street, Marnhull, Dorset, England. DT10 1PY Tel. (44) 0 1258 821 222	✓	✓			✓		✓		✓	✓	✓	✓	
Northwest Logic Design, Inc. 1905 NW 169th Place, Suite 121 Beaverton, OR 97006 Tel. (503) 533-5800	✓	✓	✓	✓			✓		✓	✓	✓	✓	
Plandscapes, Inc. 101 Kingland Dr. Stow, MA 01775 Tel. (978) 562-6462	✓							✓				✓	

Partner	Expertise						Services						
	Error Detection & Correction	Filtering	Modulation/Demodulation	Control Loops	Signal Analysis/Transform	Imaging & Compression	IP Integration	Algorithm Optimization	Hardware Optimization	Software Development	Board Design	Prototype Development	Board Products
RPA Electronics Design 1285 Chenango Street Binghamton, NY 13901 Tel. (607) 771-0393 **Offering:** Custom video processing and timing generation designs.						✓				✓	✓	✓	✓
RTI 10560 Main St., Ste. 417 Fairfax, VA 22030 Web. **http://www.rti-world.com** Tel. (703) 293-9662 **Offering:** Experience with signal processing for space-based communication and sonar development. Specific experience in bean forming hardware and software.	✓	✓	✓	✓		✓	✓		✓	✓	✓	✓	
Sam Lowenstein & Associates 118 Melody Lane, SW Vienna, VA 22180 Tel. (703) 724-2082	✓			✓		✓	✓		✓	✓	✓	✓	
Szabo Electronic Systems 40 Purvis Street Watertown, MA 02472 Tel. (617) 924-0618 **Offering:** Significant RADAR, video processing, and pattern recognition experience. TI fixed-point DSPs.		✓		✓					✓	✓	✓	✓	✓

Partner	Expertise						Services						
	Error Detection & Correction	Filtering	Modulation/Demodulation	Control Loops	Signal Analysis/Transform	Imaging & Compression	IP Integration	Algorithm Optimization	Hardware Optimization	Software Development	Board Design	Prototype Development	Board Products
Vulcan ASIC Ltd., Unit 6, The Maltings, Royston, Herts, SG8 5DY, England Tel. (44) 0 1763 248163	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	

Communications

September 1999

Overview

Communication megafunctions provide networking building blocks to improve system performance. These megafunctions are ideal for a wide variety of networking applications, ranging from switches and routers to bridges and integrated services digital network (ISDN) terminal adapters. Typically, networking systems require high performance and the flexibility to scale a design to fit different speed rates. Using Altera® programmable logic devices (PLDs) and these Altera Megafunction Partners Program (AMPP℠) megafunctions, designers can meet the speed, density, and flexibility demands of their networking applications.

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The communications section contains the following functions:

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HDLC Controller with M6800 Interface

Vendor: CAST
Target Application:
Data link controllers and protocol generators, digital sets, private branch exchanges (PBXs) and private packet networks, D-channel controller for ISDN basic access
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C015

- Formats data as per X.25 (CCITT) level-2 standards
- Single byte address recognition
- 16-bit and 32-bit frame check sequence (CRC)
- High speed serially clocked output; the data rate is equal to the clock rate
- Motorola M6800 microprocessor interface
- Software reset
- Supports multiplexing multiple HDLCs
- Internal registers for buffering

General Description

The high-level data link controller (HDLC) megafunction handles bit-oriented protocol structures, and formats the data per the packet switching protocol defined in the X.25 (level 2) recommendations of the CCITT. The megafunction transmits and receives packed data (i.e., information or control data) serially in the format shown below, while providing the data transparency by zero insertion and deletion.

Flag	Address Field	Data Field	FCS	FLAG
One Byte	Optional	*N* Bytes ($N \geq 2$)	Two Bytes	One Byte

The HDLC controller megafunction generates and detects flags, various link channel states, and the abort sequence. Further, it provides a 16- or 32-bit cyclic redundancy code check on the data packets using the CCITT-defined polynomial. In addition, the megafunction recognizes a single-byte address in the received frame. The megafunction includes a provision to disable the protocol functions and provide transparent access to the serial bus through the parallel port.

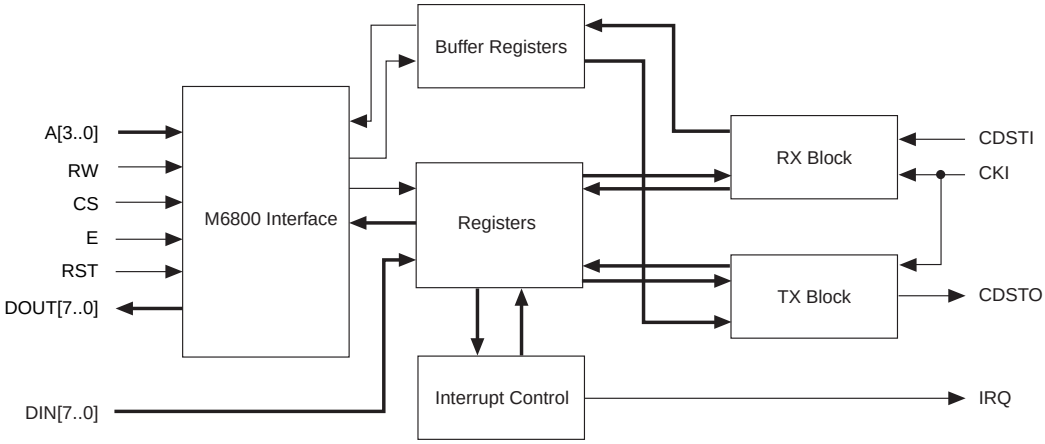
Modifiable Parameters

CAST can modify the size of the megafunction's transmit and receive first-in-first-out (FIFO) buffers. The bit rate can be programmed to be equal to the clock or to be divided by two.

Block Diagram

Figure 1 shows the block diagram for the HDLC controller megafunction.

Figure 1. HDLC Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	418	0	59 MHz	Contact CAST

HDLC Controller

Vendor: Integrated Silicon Systems
Target Application: X.25, frame-relay, ISDN B-channel and D-channel
Additional Deliverables: Behavioral VHDL testbench
ID Code: C38B-1119

- Single- and double-byte address recognition
- 16-bit (CRC-16) and 32-bit (CRC-32) frame check sequence
- Asynchronous 8-bit input data interface, suitable for a wide range of FIFO buffers
- Compatible with International Telegraphy Union (ITU) recommendation Q.921
- Serial interface with external clocking for interfacing to the PCM highway
- Transmission is synchronous to network interface with back pressure mechanism; buffering at the network interface not required
- Supports transparent mode
- Supports modular scaling of multiple HDLC channels through parallel functions or function multiplexing
- Supports data rates up to 20 Mbits/second

General Description

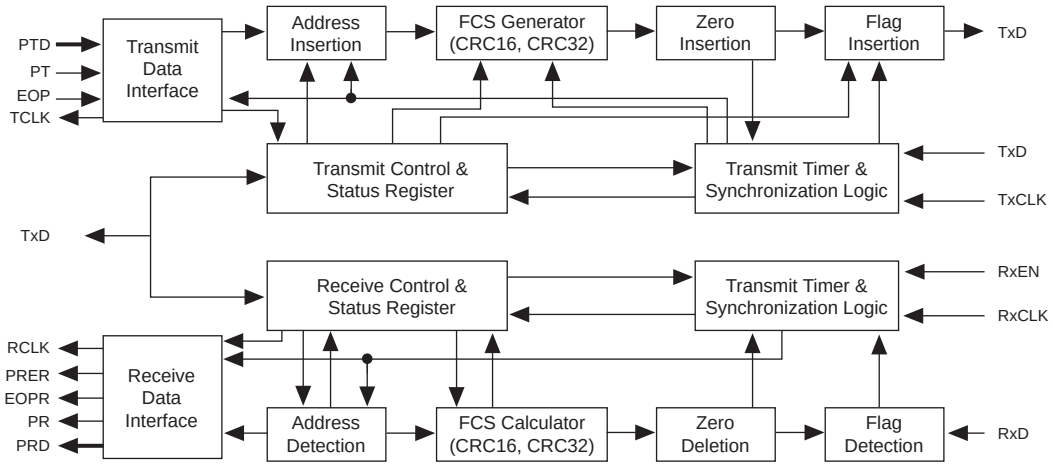
The ISS HDLC controller megafunction is a high-performance, third-level, soft-core module for the bit-oriented packet transmission mode. The megafunction is suitable for frame-relay, X.25, ISDN B-channel (64 Kbits/second), and D-channel (16 Kbits/second). The megafunction fulfills the specification according to the ITU Q.921, X.25 level 2 recommendation.

The data stream and transmission rate are controlled from the network node (PCM highway clock) with a back-pressure mechanism. This function eliminates additional synchronization and buffering of the data at the network interface. The data interface is 8-bits wide and asynchronous, and includes an 8-bit synchronization buffer. The megafunction provides basic adaptation for a wide range of FIFO buffers. It can be used as a single-channel HDLC protocol controller or as a switched parallel function used to implement an *N*-multiple channel controller. The high throughput and modular structure also enables multiplexing of the megafunction between channels for low data rate applications.

Block Diagram

Figure 2 shows the block diagram for the HDLC controller megafunction.

Figure 2. HDLC Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A *(1)*	-1	348	0	100 MHz	8-bit address
EPF10K30 *(2)*	-1	405	0	50 MHz	Fully programmable

Notes:
(1) This example is an 8-bit address, 16-bit CRC, bit-stuffing.
(2) This address is a fully programmable, bit-stuffing.

HDLC Bit-Oriented Controller

Vendor: Innocor
Target Application:
Frame relay, ISDN, X.25, point-to-point protocol controllers, multiple channel HDLC Controller
Additional Deliverables:
User manual, simulation files
ID Code:
3912

- Flag insertion and detection
- Abort generation and detection
- Zero insertion and deletion
- 16-bit CRC-CCITT generation and verification
- Operates up to STS-1 (51.84 MHz) rate
- Fully synchronous design
- Data valid and transmit enable signals for flow control
- Scalable to *N* channels
- Insert one to 255 flags between data
- Full duplex operation
- Customizable interface

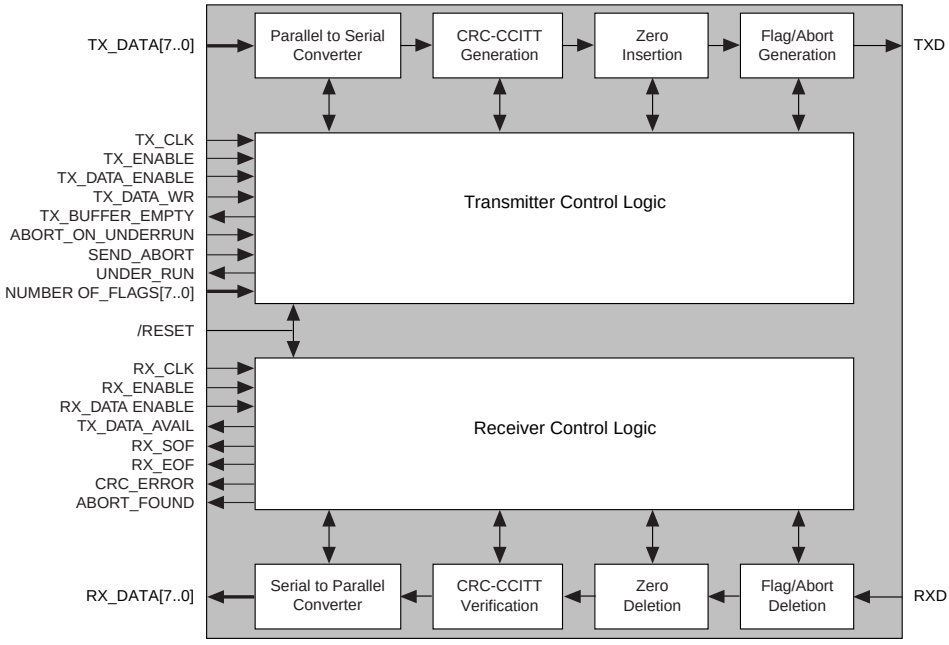
General Description

The Innocor HDLC bit-oriented controller is a high-performance megafunction module for bit-oriented data transmission. The megafunction is designed for high-speed and low-logic usage, and contains a 16-bit CRC, flag insertion/detection, zero insertion/deletion, and abort generation/detection. The megafunction's interface can be adapted for a wide range of FIFO controllers and microprocessor interfaces. Additionally, this megafunction can be easily enhanced to include advanced features such as transmit/receiver FIFO, address field recognition, CRC32, and frame length count. It supports a single channel.

Block Diagram

Figure 3 shows the block diagram for the HDLC bit-oriented controller megafunction.

Figure 3. HDLC Bit-Oriented Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	335	0	25 MHz	Contact Innocor
EPF10K10A	-1	337	0	52 MHz	Contact Innocor
EPF10K30E	-1	337	0	55 MHz	Contact Innocor

Data Encoder/Decoder

Vendor: Innocor
Target Application:
Data communications
Additional Deliverables:
User manual, simulation files
ID Code:
4993

- Encodes and decodes non-return to zero (NRZ) data to and from the following formats
  - Non-return to zero inverted (NRZI)
  - FM1 (bi-phase mark)
  - FM0 (bi-phase space)
  - Manchester (bi-phase level)
- Includes a digital phase-locked loop (DPLL)

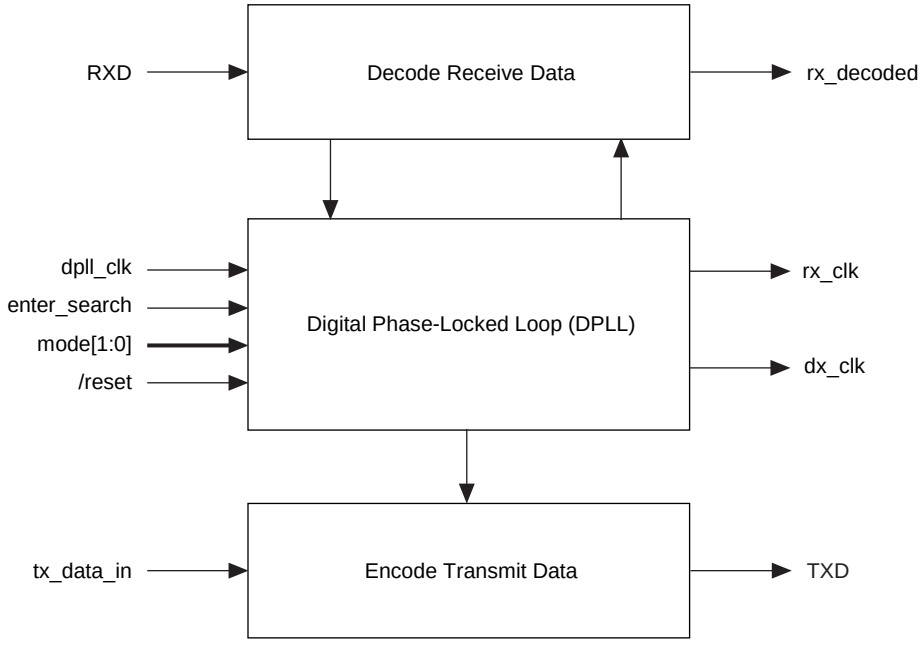
General Description

The DPLL recovers the clock from the incoming received data using a 16× (32× NRZI) DPLL clock and the incoming data. The encode path of the megafunction takes NRZ data as input and encodes it into NRZI, FM0, FM1, or Manchester encoded data. The decode path does the opposite: NRZI, FM0, FM1, or Manchester encoded data are decoded into NRZ data.

Block Diagram

Figure 4 shows the block diagram for the data encoder/decoder megafunction.

Figure 4. Data Encoder/Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *(1)*	Parameter Setting
		Logic Cells	EABs		
EPF6016	-3	140	0	26 MHz	Contact Innocor
EPF6010A	-1	140	0	40 MHz	Contact Innocor
EPF10K10A	-1	148	0	55 MHz	Contact Innocor

Note:
(1) Performance is for DPLL clock. Maximum data rate will be 1/16 for Manchester, FM0 and FM1. Maximum data rate will be 1/32 for NRZI.

Packet over SONET Controller

Vendor: Innocor
Target Application:
Packet over SONET
Additional Deliverables:
User manual, simulation files
ID Code:
3922

- Implements RFC 1619 POS and RFC 1662 HDLC—like framing specifications
- Supports STS-3c framers
- Provides statistics for the number of received packets and error packets received
- Provides signals for packets received with abort, CRC error, short, long, address and control error, protocol error, and dropped packets
- Programmable 16- or 32-bit FCS generation and verification
- Programmable address/control and protocol fields
- Optionally discards packets with address/control and protocol errors
- Optionally compresses address/control and protocol fields
- Optionally excludes protocol field for transparent mode
- One to 256 flags inserted between data
- FIFO interface

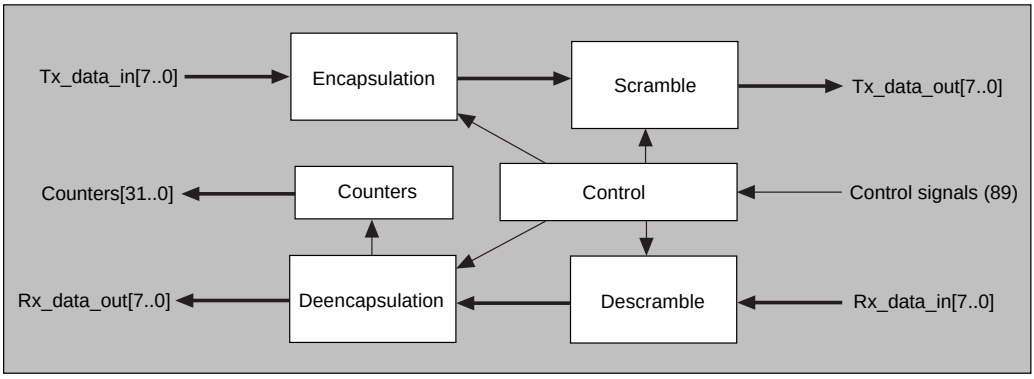
General Description

The Innocor packet over SONET controller implements RFC 1619 POS (Packet Over SONET) and RFC 1662 HDLC—like framing which allows an 8-bit data stream to be encapsulated into packets. The transmitter takes data from an 8-bit FIFO interface and performs flag, address, control, and protocol field insertion, escape character stuffing, and FCS insertion. The receiver extracts data, checks address, control, and protocol fields, performs escape character de-stuffing and verifies the FCS. The receiver also provides statistics for various errors and for the number of packets received.

Block Diagram

Figure 5 shows the block diagram for the packet over SONET controller megafunction.

Figure 5. Packet over SONET Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-3	1,182	0	20 MHz	Contact Innocor
EPF10K30A	-1	1,182	0	31 MHz	Contact Innocor
EPF10K30E	-1	1,214	0	46 MHz	Contact Innocor

ATM Receive Processor

Vendor: Innocor
Target Application:
ATM switches, ATM terminal adapters
Additional Deliverables:
User manual, simulation files
ID Code:
3941

- Cell delineation
- Cell filtering
- Payload descrambling
- HEC error counter
- Performance monitoring
- Output to indicate cell synchronization
- Operates up to OC-12 rate
- Byte-wide operation

General Description

The Innocor ATM receive processor megafunction performs cell delineation by searching for the HEC byte in the ATM cell header. Once the HEC byte is found, the cell boundary can be identified. Every ATM cell header is checked for HEC errors. An HEC error counter is provided. The incoming ATM cell payload is descrambled using a self-synchronized descrambler and the X^{43+1} polynomial. Idle cells are dropped and will not be presented to the output. A 32-bit cell counter is provided to collect statistics on a particular VPI/VCI channel which the user can use to calculate bandwidth usage. An output is also provided to signal ATM synchronization and to signal the programmed VPI/VCI channel match.

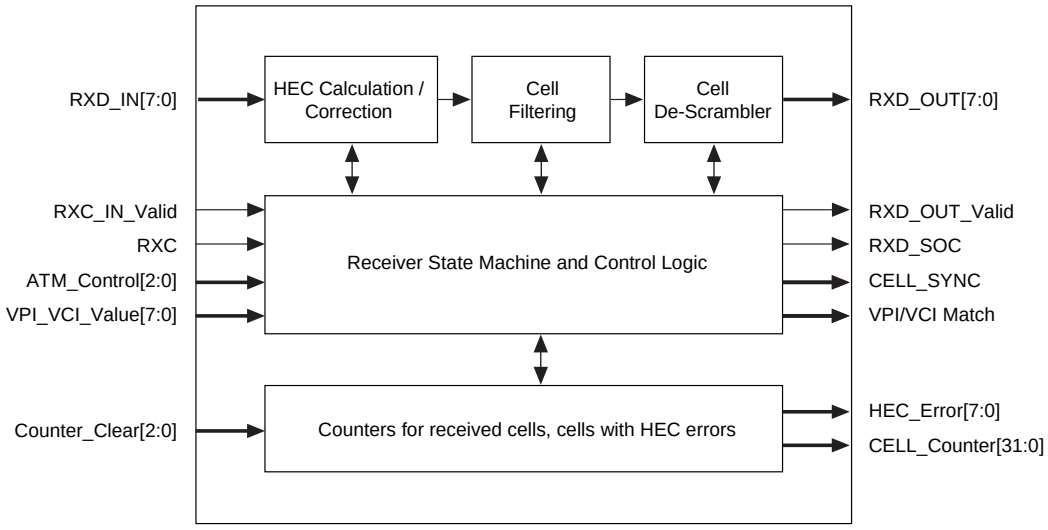
Modifiable Parameters

The ATM receive processor can be modified to include counters for different VPI/VCI channels. The 32-bit cell counter width can be increased or decreased. For other modifications, contact Innocor Ltd.

Block Diagram

Figure 6 shows the block diagram for the ATM receive processor megafunction.

Figure 6. ATM Receive Processor Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	494	0	47 MHz	Contact Innocor
EPF10K10A	-1	492	0	84 MHz	Contact Innocor

SONET Byte Telecommunications Bus Interface

Vendor: Innocor
Target Application:
SONET add/drop multiplexer, SONET terminal multiplexer, PPP over SONET
Additional Deliverables:
User manual, simulation files
ID Code:
5951

- Byte-wide operation
- STS-1/3/3c processing
- Separate data from overheads on DROP side
- Generate ADD side control signals
- Insert external data to ADD bus
- Loopback for diagnostic testing

General Description

The Innocor SONET byte telecom bus interface megafunction extracts data from, or maps data into the SONET payload envelope. By decoding the bus control signals, the payload data is separated from the overhead bytes. The megafunction includes the identification of positive or negative pointer justification events and fixed columns in STS-1 or STS-3 SONET frames.

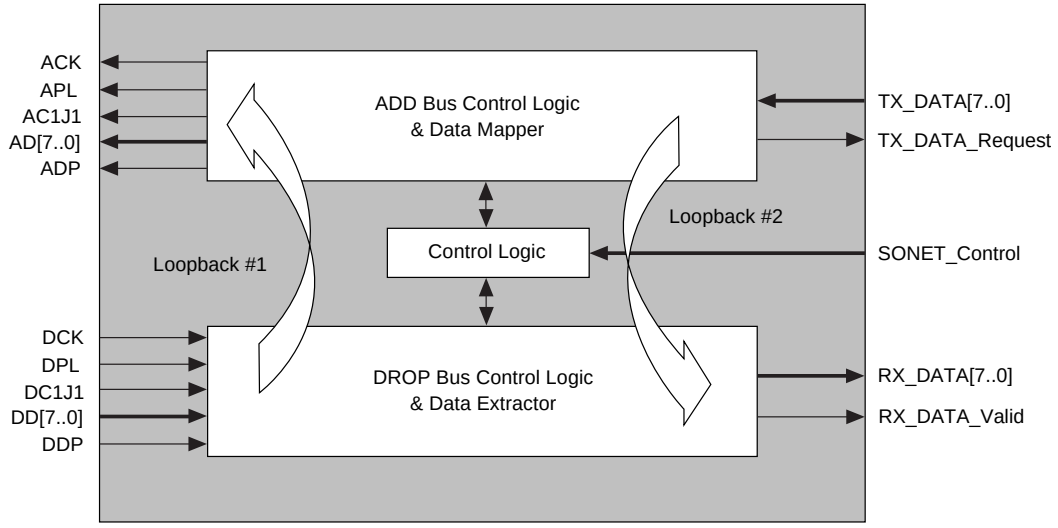
On the ADD side, the control signals can be derived from external mapping devices, the DROP side, or internally generated. External data is added into the SONET payload envelope by decoding the ADD control signals. For fixed column locations, the megafunction can be configured to carry data or zeros.

For testing and verification purposes, two loopback points are provided. One point connects the DROP bus to the ADD bus. The other point connects the data to be mapped into the payload to the data extracted from the payload.

Block Diagram

Figure 7 shows the block diagram for the SONET byte telecommunications bus interface megafunction.

Figure 7. SONET Byte Telecommunications Bus Interface Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	340	0	54 MHz	Contact Innocor
EPF10K10A	-1	340	0	86 MHz	Contact Innocor

Telephony Tone Generation (ToneGen)

Vendor: NComm, Inc.
Target Application:
PBX, T-1 trunk signaling, SS7 path verification, DTMF tones
Additional Deliverables:
Test vectors
ID Code: 423E-7212

- Generates single- and dual-frequency tones used in telephony applications
- Outputs ST-Bus, IOM-2, IDL, and other standard-compatible serial streams containing from 1 to 32 tones
- Supports both µ-Law and A-Law encoding algorithms
- Provides fully configurable gain control for individual tones and for each frequency component that makes up a tone
- Parameterization via the MegaWizard™ Plug-In features tone creating, tone editing, and tone testing using a sound-capable computer

General Description

The tone generation (ToneGen) megafunction is a Mitel ST-Bus-compatible device providing from 1 to 32 user-programmable tones used in telephony applications. The ToneGen megafunction can generate any combination of single- and/or dual-frequency tone sequences, such as dialtone, ringback, busy, DTMF, SS7 path validation, MF, and any other custom tone sequence. The ToneGen megafunction supports gain control, µ-law or A-law encoding, and other parameters on a tone-by-tone basis, providing complete control over the tones being generated. Because the megafunction is parameterized with the MegaWizard Plug-In, the ToneGen megafunction allows users to configure new tones, edit existing tones, listen to generated tones on a sound-capable computer, and minimize the ROM storage required to contain the tones. The Altera MegaWizard Plug-In provides a simple and powerful way to add tone generation to telephony or other applications.

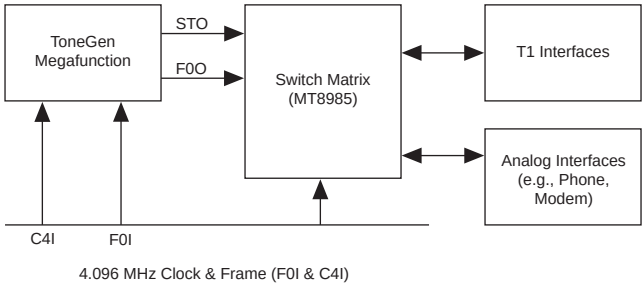
Modifiable Parameters

The ToneGen megafunction can be customized to create different tones. With the associated MegaWizard Plug-In, users can create virtually any set of tones required by the target application. In addition, the MegaWizard Plug-In allows users to minimize the number of embedded array blocks (EABs) required to synthesize a set of tones by calculating the least number of PCM samples required to generate the desired tone sequences.

Block Diagram

Figure 8 shows the block diagram for the ToneGen megafunction.

Figure 8. Telephony Tone Generation Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-4	445	6	23.14 MHz	MF tones 0 - 9, ST, and KP
		136	6	26.24 MHz	Dialtone, busy tone, and ringback
EPF10K50	-4	50	4	30.48 MHz	Dialtone
EPF10K20	-3	445	4	30.86 MHz	MF tones 0 - 9, ST, and KP
		136	6	26.24 MHz	Dialtone, busy tone, and ringback

UTOPIA Level 2: Slave MegaCore Function

Vendor: Altera
Target Application:
ATM, router controller, switch interface
Additional Deliverables:
UTOPIA Level 2: Slave MegaCore Data Sheet
Ordering Code:
PLSM-UTOPIA2SL

MegaCore™

MegaWizard™ Plug-In

- Conforms to UTOPIA level 2, version 1.0 specification
- Supports 8- or 16-bit UTOPIA bus operation and local bus widths of 8- or 16-bits
- Single PHY (SPHY) operation is supported, with both octet- and cell-level handshaking
- Multi-PHY (MPHY) operation supported with single `clav` signal
- Parity generation and detection
- Optional cell discard on parity error detection
- Internal 4-cell FIFO buffers supported for both transmit and receive
- Optimized for FLEX® 10KE and APEX™ 20K architectures
- Dramatically shortens design cycles
- Extensive simulation testing
- Includes test vectors
- OpenCore™ feature allows designers to instantiate and simulate designs in the Quartus™ and MAX+PLUS® II software prior to purchase

General Description

The UTOPIA level 2 slave MegaCore™ function is designed for use in PHY layer devices that transfer data to and from ATM devices using the standard UTOPIA bus. The MegaCore function comprises a separate transmitter and receiver; both support SPHY, and MPHY operation modes. SPHY mode supports octet- or cell-level handshake; MPHY mode supports cell-level handshake.

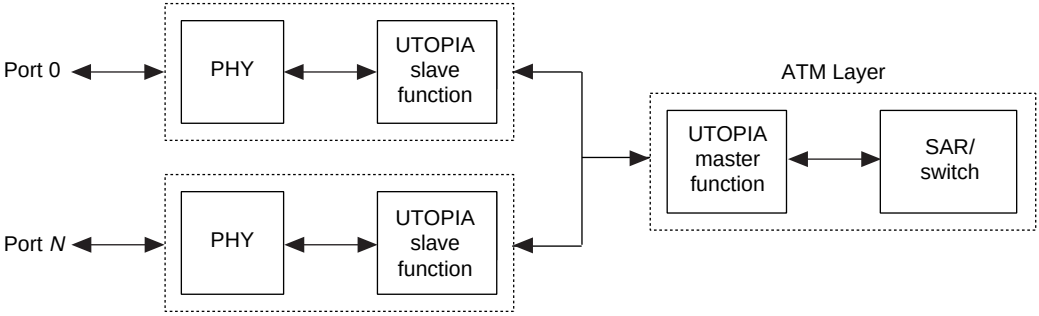
The transmitter is polled by the ATM layer to determine if it is ready to receive data transfers. The transmitter accepts cells from the ATM layer via the UTOPIA bus interface, and sends them to the PHY devices. It detects and discards cells it receives that are too short, and discards excess bytes from cells that are too long. It also checks for parity errors on the UTOPIA bus, and there is an option to discard cells with detected parity errors.

The receiver is polled by the ATM layer to determine if it is ready to send data transfers. The receiver accepts cells from the PHY layer, and sends them to the ATM layer device via the UTOPIA bus interface. There is an option to generate parity information for the UTOPIA bus.

Block Diagram

Figure 9 shows the block diagram for the UTOPIA level 2 slave megafunction.

Figure 9. UTOPIA Level 2: Slave Megafunction Block Diagram



Device Utilization Examples *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-2	222	1	79 MHz	16-bit user/UTOPIA width, 54 bytes user cell size, MPHY mode, using `parity_check` and `discard_on_error`.
		256	1	69 MHz	8-bit user/UTOPIA width, 52 bytes user cell size, MPHY mode, using `parity_check` and `discard_on_error`.

Device Utilization Examples *Note (2)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-2	201	1	73 MHz	16-bit user/UTOPIA width, 54 bytes user cell size, MPHY mode, using `parity_generation`.
		241	1	57 MHz	8-bit user/UTOPIA width, 52 bytes user cell size, MPHY mode, using `parity_generation`.

Notes to tables:
(1) Performance of the transmitter.
(2) Performance of the receiver.

UTOPIA Level 2: Master MegaCore Function

Vendor: Altera
Target Application:
ATM, router controller, switch interface
Additional Deliverables:
UTOPIA Level 2: Master MegaCore Data Sheet
Ordering Code:
PLSM-UTOPIA2MS

MegaCore™

MegaWizard™ Plug-In

- Compliant with ATM Forum UTOPIA level 2, version 1.0 specification
- Supports 8- or 16-bit UTOPIA bus operation
- SPHY operation is supported, with both octet- and cell-level handshaking
- MPHY operation supported with single `clav` signal
- Logical to physical address translation via programmable look-up table
- Parity generation and detection
- Optimized for FLEX 10KE and APEX 20K architecture
- Dramatically shortens design cycles
- Extensive simulation testing
- Includes test vectors
- OpenCore feature allows you to instantiate and simulate designs in the Quartus and MAX+PLUS II software prior to purchase

General Description

The UTOPIA level 2 master MegaCore function is designed for use in ATM layer devices that transfer data to and from PHY devices using the standard UTOPIA bus. The UTOPIA level 2 master MegaCore function comprises a separate transmitter and receiver; both support single PHY (SPHY), and multi PHY (MPHY) operation modes. SPHY mode supports octet- or cell-level handshake; MPHY mode supports cell-level handshake with up to 31 PHY devices.

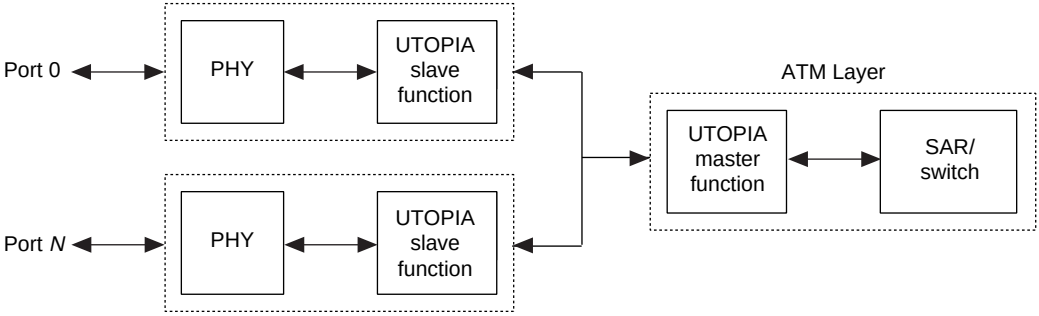
The transmitter polls the PHY layers in a round-robin fashion to determine which are ready to receive data transfers, and outputs the poll status to the ATM layer. The transmitter accepts cells from the ATM layer, and sends them to the PHY devices via the UTOPIA bus interface. There is an option to generate parity information for the UTOPIA bus.

The receiver polls the PHY layers in a round-robin fashion to determine which are ready to send data transfers, and outputs the poll status to the ATM layer. The receiver accepts cells from the PHY devices via the UTOPIA bus interface, and sends them to the ATM layer. There is an option to check parity errors on the UTOPIA bus.

Block Diagram

Figure 10 shows the block diagram for the UTOPIA level 2 master megafunction.

Figure 10. UTOPIA Level 2: Master Megafunction Block Diagram



Device Utilization Examples *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-2	357	2	60 MHz	16-bit UTOPIA width, 52 bytes user cell size, MPHY mode, using address translation.
		332	1	77 MHz	8-bit UTOPIA width, 53 bytes user cell size, MPHY mode.
		142	1	70 MHz	8-bit UTOPIA width, 52 bytes user cell size, SPHY mode.

Device Utilization Examples *Note (2)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-2	318	2	62 MHz	16-bit UTOPIA width, 52 bytes user cell size, MPHY mode, using address translation.
		302	1	76 MHz	8-bit UTOPIA width, 53 bytes user cell size, MPHY mode.
		117	1	88 MHz	8-bit UTOPIA width, 52 bytes user cell size, SPHY mode.

Notes to tables:
(1) Performance of the transmitter.
(2) Performance of the receiver.

UTOPIA Level 2: Slave Transmitter/Receiver

Vendor: Applied Microelectronics
Target Application: ATM, PHY interface to ATM, PHY interface to local bus
ID Code: B321-1001

- Cell or octet-level interface
- 8- or 16-bit data bus
- SPHY or MPHY (32 port) mode
- In SPHY, octet or cell-level handshaking, MPHY supports single CLAV
- Four cell depth transmit buffer and four cell depth receive buffer
- Optional parity generation in receive direction
- Optional parity checking in transmit direction
- Optional cell discard based on bad parity in transmit direction
- Optional output enables for counting good (non-errored) and bad (errored) cells
- Independent clocking for UTOPIA and local bus interfaces
- Static slave address
- Cell depth can be configured as 52 or 53 (8-bit)/54 (16-bit) bytes long
- 25-, 33-, and 50-MHz UTOPIA Level 2
- Compliant with ***ATM Forum UTOPIA Level 2, version 1.0***

General Description

The UTOPIA level 2 slave megafunction is a multi-PHY, multi-clock domain, bidirectional interface between a local bus and the ATM layer. The megafunction incorporates two rate matching FIFO buffers each with a cell depth of four.

Octet or cell data is received by the slave transmitter from an ATM layer, stored in the dual-port RAM (FIFO), and accessed from the RAM by the local bus. Data sent from the local bus is stored in the dual-port RAM (FIFO), and retrieved by the Slave receiver for transmission to the ATM layer.

The UTOPIA level 2 slave is a multi-clock domain megafunction that handles the different clock domains of the local bus and UTOPIA level 2 interface.

The UTOPIA level 2 slave megafunction is composed of a transmitter and receiver that are totally independent of one another and each may be acquired as separate megafunctions. The megafunction is designed with a modular architecture, allowing for upgrading to the UTOPIA level 3 megafunction. Additional consulting and development services are available. Contact the Applied Microelectronics for more details.

Modifiable Parameters

The following megafunction parameters can be modified:

Modifiable Parameters

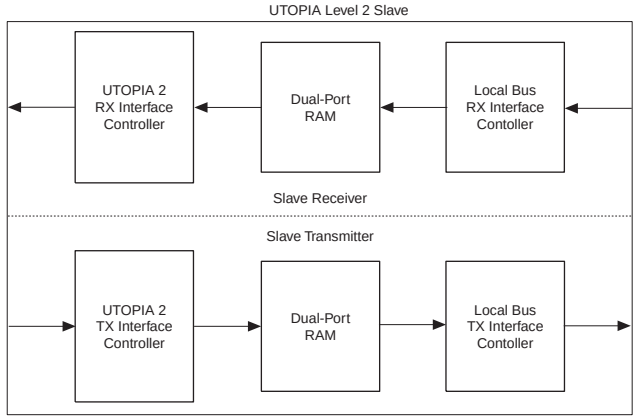
Parameter	Description
ParityGen	Parity generation in receiver
ParityCheck	Parity check in transmitter
Lwidth	Local bus width *(1)*
Uwidth	UTOPIA bus width *(1)*
TX Short_Cell	Selection of cell depth (transmitter)
TX Slave_Addr	Static slave address (transmitter)
TX Octet_Mode	Selection of octet or cell mode (transmitter)
Discard_Mode	Optionally discard bad cells
TX SPHY_Mode	Selection of SPHY or MPHY mode (transmitter)
RX Slave_Addr	Static slave address (receiver)
RX Short_Cell	Selection of cell depths (receiver)
RX Octet_Mode	Selection of octet or cell mode (receiver)
RX SPHY_Mode	Selection of SPHY or MPHY mode (receiver)

Note:
(1) Lwidth ≥ Uwidth.

Block Diagram

Figure 11 shows the block diagram for the UTOPIA level 2 slave megafunction.

Figure 11. UTOPIA Level 2 Slave Megafunction Block Diagram *Note (1)*



Note:
(1) The UTOPIA level 2 slave transmitter/receiver may be acquired separately.

Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	620/1728	4/6	70 MHz	`Lwidth` = 32, `Uwidth` = 16 Without `ParityGen/Check`
		487/1728	3/6	68 MHz	`Lwidth` = 16, `Uwidth` = 16 Without `ParityGen/Check`
		588/1728	4/6	60 MHz	`Lwidth` = 32, `Uwidth` = 8 Without `ParityGen/Check`
		518/1728	2/6	62 MHz	`Lwidth` = 16, `Uwidth` = 8 Without `ParityGen/Check`
		462/1728	2/6	63 MHz	`Lwidth` = 8, `Uwidth` = 8 Without `ParityGen/Check`
		699/1728	4/6	62 MHz	`Lwidth` = 32, `Uwidth` = 16 With `ParityGen/Check`
		531/1728	2/6	66 MHz	`Lwidth` = 16, `Uwidth` = 16 With `ParityGen/Check`
		649/1728	4/6	62 MHz	`Lwidth` = 32, `Uwidth` = 8 With `ParityGen/Check`
		536/1728	3/6	65 MHz	`Lwidth` = 16, `Uwidth` = 8 With `ParityGen/Check`
		479/1728	2/6	62 MHz	`Lwidth` = 8, `Uwidth` = 8 With `ParityGen/Check`

UTOPIA Level 2: Master Receiver

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL
ID Code: C08E-20A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 155 Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ***ATM Forum UTOPIA level 2, version 1.0***

General Description

The UTOPIA level 2 master receiver megafunction receives ATM cells from receive UTOPIA slaves on the UTOPIA bus. The megafunction conforms to UTOPIA level 2 specifications and is configurable to work with a maximum of 31 ports. During cell transfers, the megafunction reads 16 bits of data every clock cycle. Then, it assembles the data into a 32-bit word and writes the word to the cell FIFO buffer corresponding to the PHY port.

The state machine polls the available physical ports serially and stores the polling status. On the cell FIFO side, each FIFO buffer gives one bit of information indicating that it is ready to receive one cell. The port for cell reception is chosen from those ports that can transmit a cell and have the corresponding cell FIFO buffer ready. When the cell transfer is about to end, the state machine looks for the next port in round-robin fashion. If no other port is available, and the current port's FIFO buffer can accept one more cell, the current port is not deselected immediately. If the port has one more cell to transmit, the cell is taken in as the next cell for the same port. Therefore, this master function supports back-to-back cells.

The data received from the physical port is assembled in a 32-bit register in the data width matching multiplexer block and sent to the appropriate FIFO buffer. The FIFO buffer is selected using the `FIFOSelect` pins.

The logical to physical mapping block has a look-up table (LUT) that can be programmed through the control interface. After choosing a port for selection or polling, the port address is converted to the corresponding physical address and then placed on the `RxAddr` bus. This process allows flexibility in allocating an arbitrary physical address to a set of logical addresses.

Modifiable Parameters

The following megafunction parameters can be modified:

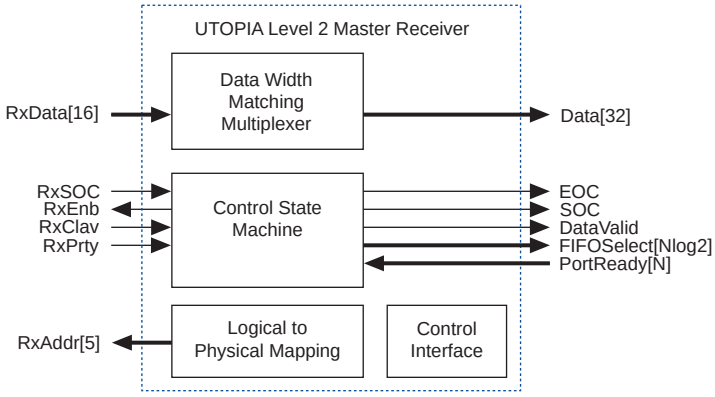
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 12 shows the block diagram for the UTOPIA level 2 master receiver megafunction.

Figure 12. UTOPIA Level 2 Master Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	528	0	65 MHz	P = 4, PB = 2

UTOPIA Level 2: Master Receiver

Vendor: Applied Microelectronics
Target Application: ATM, ATM interface to PHY, ATM interface to local bus
ID Code: B321-1002

- Cell- or octet-level interface
- 8- or 16-bit UTOPIA 2 data bus
- 8- or 16-bit local bus width
- SPHY or MPHY (31 port) mode
- In SPHY, octet or cell-level handshaking, MPHY supports single CLAV
- In MPHY mode, polls 1 to 31 addresses
- Optional parity checking in receive direction
- Cell depth can be configured as 52 or 53 (8-bit)/54 (16-bit) bytes long
- 25-, 33-, and 50-MHz UTOPIA Level 2
- Compliant with ***ATM Forum UTOPIA Level 2, version 1.0***

General Description

The UTOPIA level 2 master receiver megafunction is a receive interface between a local bus and the PHY layer. The megafunction handles the polling and selection of the PHY addresses and provides flow control of the data.

The UTOPIA 2 master receiver is designed with a modular architecture, allowing for upgrade to UTOPIA 3 megafunction. Additional consulting and development services are available. Contact Applied Microelectronics for more details.

Modifiable Parameters

The following megafunction parameters can be modified:

Modifiable Parameters

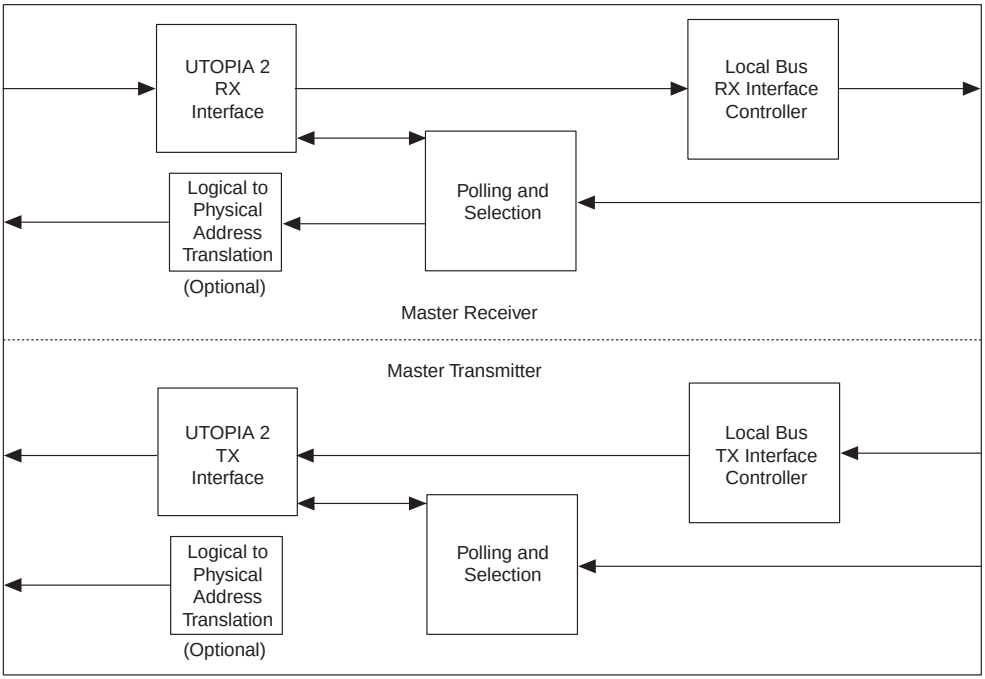
Parameter	Description
`ParityCheck`	Parity check in receiver
`Lwidth`	Local bus width *(1)*
`Uwidth`	UTOPIA bus width *(1)*
`Short_Cell`	Selection of cell depth
`Octet_Mode`	Selection of octet or cell mode
`SPHY_Mode`	Selection of SPHY or MPHY mode

Note:
(1) `Lwidth` = `Uwidth`.

Block Diagram

Figure 13 shows the block diagram for the UTOPIA level 2 master receiver megafunction.

Figure 13. UTOPIA Level 2 Master Block Diagram *Note (1)*



Note:
(1) The UTOPIA 2 master transmitter or receiver may be acquired separately.

Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30E	-1	497/1728	0	60 MHz	`Lwidth` = 8, `Uwidth` = 8, without parity
		592/1728	0	58 MHz	`Lwidth` = 16, `Uwidth` = 16, without parity
		529/1728	0	62 MHz	`Lwidth` = 8, `Uwidth` = 8, with parity gen/check
		615/1728	0	59 MHz	`Lwidth` = 16, `Uwidth` = 16, with parity gen/check

UTOPIA Level 2: Master Transmitter

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C08E-40A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 622 Mbps
- 25-, 33- and 50-MHz UTOPIA level 2 bus support
- Supports up to 32 ports
- Supports physical to logical address mapping
- Compliant with ***ATM Forum UTOPIA Level 2, version 1.0***

General Description

The UTOPIA Level 2 master transmitter megafunction reads asynchronous transfer mode (ATM) cell data from different ports and sends it to physical layer (PHY) devices across the UTOPIA interface. The megafunction acts as a master (***ATM Forum UTOPIA level 2, version 1.0*** specification) and follows UTOPIA level 2 specification, version 1.0 for multi-PHY cell-level handshake protocol in 16-bit mode.

The state machine polls the available PHY ports serially and stores the polling status. On the cell FIFO side, each FIFO buffer sends one bit of information indicating that it is ready to transmit one cell. The port for cell transmission is chosen from those ports ready to accept a cell and have the corresponding cell FIFO buffer ready. When the cell transfer is almost finished, the state machine looks for next port transmission in round-robin fashion. If no other port is available and the current port's FIFO buffer has one more cell to transmit, the next cell's transmission starts immediately after the current cell transmission is over.

Each cell FIFO buffer sends data to the megafunction via the 32-bit data bus. The data width matching multiplexer module accepts data from all FIFO buffers and chooses the appropriate data. This data is sent on the `TxData` bus to the PHY device, 16 bits at a time. The logical to physical mapping module has a look-up table (LUT) that can be programmed through the control interface. After choosing a port for selection or polling, the port address is converted to the corresponding physical address and then placed on the `TxAddr` bus. This sequence allows flexibility in allocating an arbitrary physical address to a set of logical addresses.

Modifiable Parameters

The following megafunction parameters can be modified:

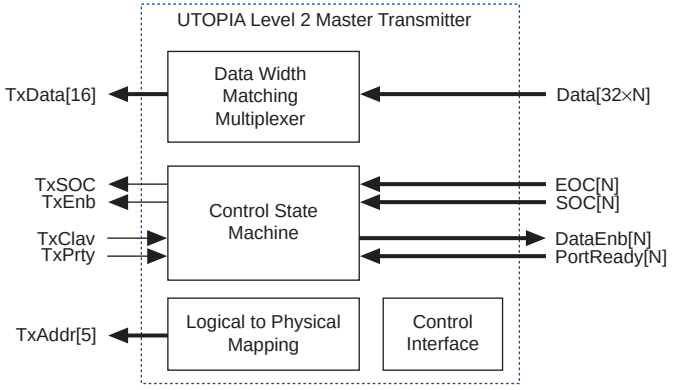
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 14 shows the block diagram for the UTOPIA level 2 master transmitter megafunction.

Figure 14. UTOPIA Level 2 Master Transmitter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	363	0	82 MHz	P = 4, PB = 2

UTOPIA Level 2: Slave Receiver

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, RTL documentation
ID Code: C08E-30A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 622 Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ***ATM Forum UTOPIA level 2, version 1.0***

General Description

The UTOPIA level 2 slave receiver megafunction supports multiple PHY operation and transmits data on the UTOPIA bus. The cell FIFO buffer receives data in a 32-bit double-word format, and then sends it to the UTOPIA bus in a 16-bit word format.

The UTOPIA level 2 slave receiver megafunction has a cell-based interface, and it can support as many as 32 ports. A UTOPIA level 2 master receiver megafunction polls the slave megafunction for the availability of cells in various ports through the polling interface. The master receiver megafunction presents the PHY address to check if any cells are available for that PHY port. Cell availability is solely dependent on the cell FIFO interface, which gives the port ready status. A port ready status indicates that the port has an outgoing cell. The `RxClav` signal is asserted when the cell FIFO interface asserts the port ready status. The cell FIFO buffer stores the outgoing cells on a per port basis.

The UTOPIA level 2 slave receiver megafunction works in a 54-byte mode and transfers take place on a 16-bit wide UTOPIA data bus. Twenty-six transfers occur for each cell. The HEC word, which is the third word in the transfer, is a dummy byte. The physical layer places the appropriate HEC byte in the cell.

Data is packed according to the standard transmission convention. The upper byte of the word is the first one on the line.

Physical to logical address mapping is supported through a set of configuration registers, which are programmed through a standard microprocessor interface.

Modifiable Parameters

The following megafunction parameters can be modified:

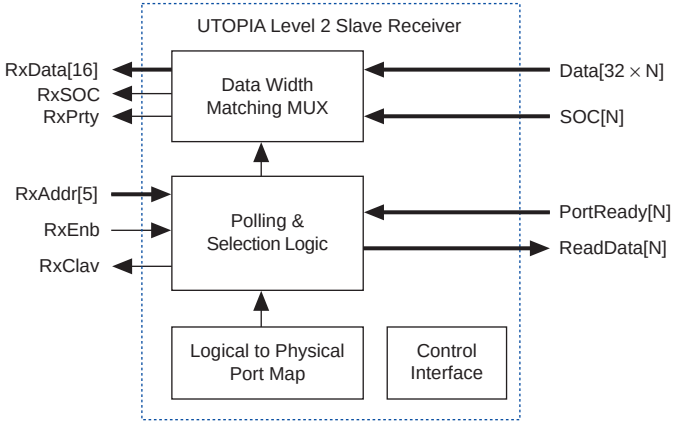
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 15 shows the block diagram for the receive UTOPIA level 2 slave receiver megafunction.

Figure 15. UTOPIA Level 2 Slave Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	449	0	54 MHz	P = 4, PB = 2

UTOPIA Level 2: Slave Transmitter

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C08E-50A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 622-Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ***ATM Forum UTOPIA level 2, version 1.0***

General Description

The UTOPIA level 2 slave transmitter megafunction operates in a multi-PHY environment. It receives cells from the UTOPIA bus and assembles the data into 32-bit double words. Thereafter, the megafunction passes the data to the cell FIFO interface controller along with the appropriate port number. The `TxClav` signal generation is dependent on the cell FIFO interface controller. If the cell FIFO interface can accept a new cell when the master polls the megafunction, the `TxClav` signal is asserted.

The UTOPIA level 2 slave transmitter megafunction accepts 16-bit words on the UTOPIA bus and assembles them into double words before transferring them to the cell FIFO buffer. When a port is selected, the megafunction sends the assembled 32-bit data to the cell FIFO buffer and validates that data with a data enable signal.

The megafunction operates in a 16-bit UTOPIA data bus mode. There are 26 transfers for each cell transfer. The third word is masked because it is the HEC byte. The HEC check is performed by the physical layer device and data is packed in the standard way.

Physical to logical address mapping is supported through configuration registers that are programmable via the microprocessor interface.

Modifiable Parameters

The following megafunction parameters can be modified:

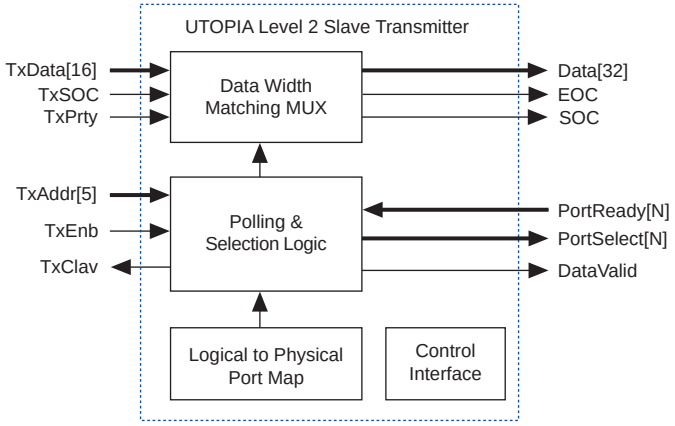
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 16 shows the block diagram for the UTOPIA level 2 slave transmitter megafunction.

Figure 16. UTOPIA Level 2 Slave Transmitter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	363	0	82 MHz	P = 4, PB = 2

10/100 Mbits Fast Ethernet Media Access Controller Receiver

Vendor: CoreEl MicroSystems
Target Application: Ethernet
ID Code: C08E-FE24

CoreEl MicroSystems

- Meets the ISO/IEC 8802.3 1996 specification
- Supports 10- and 100-Mbit media-independent interface-based physical devices
- Compact and modular design is ideal for multiport, switch, and router applications
- Supports half- and full-duplex operations
- Extensive statistical information on transmit and receive frames
- Flexible frame retransmission or abort feature
- Short frame transmission provided by padding
- Optional long frame transmission and reception feature up to 4,096 octets
- Media independent interface (MII) for connection to physical layer
- Simple host data transfer interface
- Host interface data path width configurable for 8 or 16 bits
- Fully synthesizable register transfer level (RTL) VHDL code provided
- Synthesized tools from the following vendors:
  - Synopsys
  - Mentor Graphics
  - Exemplar Logic
- Synthesis scripts supplied with megafunction
- Fully synchronous single-clock logic
- Meets virtual socket interface (VSI) specification for a soft virtual component
- User-programmable, comprehensive testbench available
- Modular design facilitates user customization
- OpenCore evaluation available
- Meets the ISO/IEC 8802.3 1996 specification

General Description

The fast Ethernet media access controller (MAC) receiver megafunction implements the Ethernet media access control protocol in accordance with the fast Ethernet IEEE 802.3 specification. The MAC protocol has a standard MII for connection to any physical interface. The FEM is suitable for both 10-Mbit and 100-Mbit operation.

The FEM receiver is designed as a fully synthesizable function. The megafunction is written in the RTL and is fully synchronous with the receive clock (RX_CLK) from the MII interface.

The FEM receiver provides a MII to a physical interface and a host interface to an on-chip FIFO buffer or RAM. Frame reception starts if the receiver has been enabled and data valid (RX_DV) becomes true on the MII interface. The FEM receiver then looks for the preamble and start of the frame delimiter pattern. The FEM receiver then switches to receiving frame data and transferring it to the host via an 8- or 16-bit interface. The width of the interface is configurable.

The function was designed according to the recommendations of the Virtual Socket Interface (VSI) Alliance and is recommended for integration with other custom functions in a top-down design flow. The megafunction is ideally suited for incorporating into a programmable logic device (PLD) or an application-specific integrated circuit (ASIC) together with other higher-level functions. For example, the megafunction is ideal for the design of a multi-channel MAC chip, where it can be implemented with other common functions such as a linked list buffer manager and a DMA control function.

A distinguishing feature of this megafunction is its detailed and comprehensive frame transmission statistics vector reports. The frame statistics vector information can be used to implement Ethernet management information base (MIB) counters or to facilitate support for remote monitoring (RMON) and the simple network management protocol (SNMP).

The FEM megafunction can be used in various integrated applications. One example is a multiport Ethernet MAC controller with a peripheral component interconnect (PCI) interface. A single channel version of such a device is an ideal solution for inexpensive network interface controller (NIC) cards. Because of the low gate count of the FEM megafunction, several Ethernet ports can be put on a single device together with the switching fabric to produce an integrated low-cost switch.

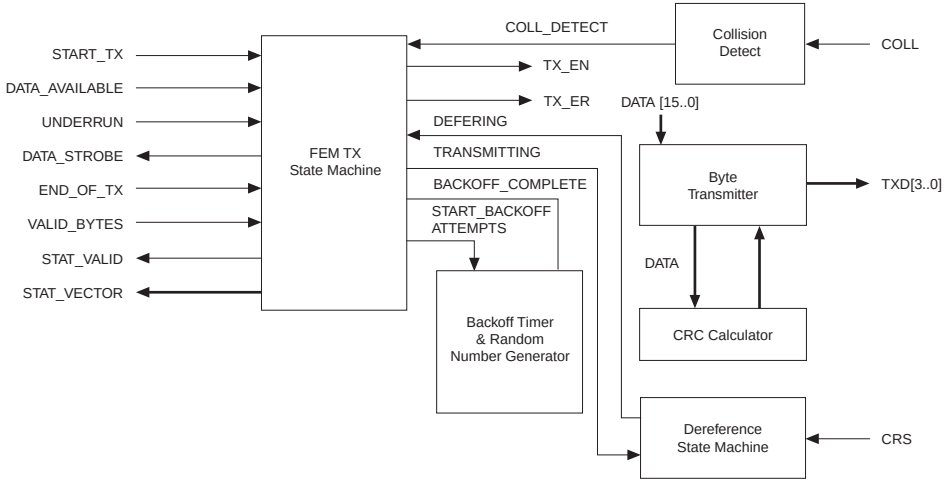
The FEM megafunction has been tested independently using an Ethernet-compliant testbench. The fully modular design of the function facilitates easy customization.

The FEM megafunction meets the ***Virtual Socket Interface Alliance, version 1.0*** recommendation for a soft virtual component. Compliance is achieved by providing a detailed and comprehensive specification, a theory of operation document, a clearly defined and modeled user interface, a programmable Ethernet-compliant testbench, and compilation and synthesis scripts.

Block Diagram

Figure 17 shows the block diagram for the FEM access controller receiver megafunction.

Figure 17. FEM Access Controller Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	681	0	45 MHz	Contact CoreEl Microsystems

10/100 Mbits Fast Ethernet Media (FEM) Access Controller Transmitter

Vendor: CoreEl MicroSystems
Target Application: Ethernet
ID Code: C08E-FE25

CoreEl MicroSystems

- Meets the ISO/IEC 8802.3 1996 specification
- Supports 10- and 100-Mbit media-independent interface-based physical devices
- Compact and modular design is ideal for multiport, switch, and router applications
- Supports half- and full-duplex operations
- Extensive statistical information on transmit and receive frames
- Flexible frame retransmission or abort feature
- Short frame transmission provided by padding
- Optional long frame transmission and reception feature up to 4,096 octets
- Media independent interface (MII) for connection to physical layer
- Simple host data transfer interface
- Host interface data path width configurable for 8 or 16 bits
- Fully synthesizable register transfer level (RTL) VHDL source code provided
- Synthesized tools from the following vendors:
  - Synopsys
  - Mentor Graphics
  - Exemplar Logic
- Synthesis scripts supplied with the megafunction
- Fully synchronous single-clock logic
- Meets virtual socket interface (VSI) specification for a soft virtual component
- User-programmable, comprehensive testbench available
- Modular design facilitates user customization cell-based interface
- 16-bit data bus
- Performance up to 622 Mbps
- 25-, 33-, and 50-MHz UTOPIA level 2 bus support
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ***ATM Forum UTOPIA Level 2, version 1.0***

General Description

The fast Ethernet media (FEM) access controller transmitter megafunction implements the Ethernet media access control (MAC) protocol in accordance with the Fast Ethernet IEEE 802.3 specification. The MAC protocol has a standard MII for connection to any physical interface. The FEM function is suitable for both 10-Mbit and 100-Mbit operation.

The FEM transmitter is designed as a fully synthesizable function. It is written at the register transfer level (RTL) and is fully synchronous with the transmit clock (TX_CLK) from the MII interface.

The FEM transmitter provides a MII to a physical interface and a host interface to an on-chip FIFO buffer or RAM. Frame transmission is initiated from the host and frame data is provided to the FEM transmitter via an 8-bit or 16-bit user-configurable data bus. The user merely designs a simple control function to read data from a FIFO buffer and initiate a frame transfer through the FEM transmitter.

The function was designed according to the recommendations of the Virtual Socket Interface (VSI) Alliance and is recommended for integration with other custom functions in a top-down design flow. The megafunction is ideally suited for incorporating into a PLD or an ASIC together with other higher level functions. It is ideal, for example, for the design of a multichannel MAC chip, in which it can be implemented with other common functions such as a linked list buffer manager and a direct memory access (DMA) control function.

A distinguishing feature of this megafunction is its detailed and comprehensive frame transmission statistics vector reports. Care has been taken to provide as much statistical information as possible. The frame statistics vector information can be used to implement Ethernet management information base (MIB) counters or to facilitate support for remote monitoring (RMON) and the simple network management protocol (SNMP).

The FEM megafunction can be used in various integrated applications. One example is a multiport Ethernet MAC controller with a peripheral component interconnect (PCI) interface. A single channel version of such a device is an ideal solution for inexpensive network interface controller (NIC) cards. Because of the low gate count of the FEM megafunction, several Ethernet ports can be put on a single device together with the switching fabric to produce an integrated low cost switch.

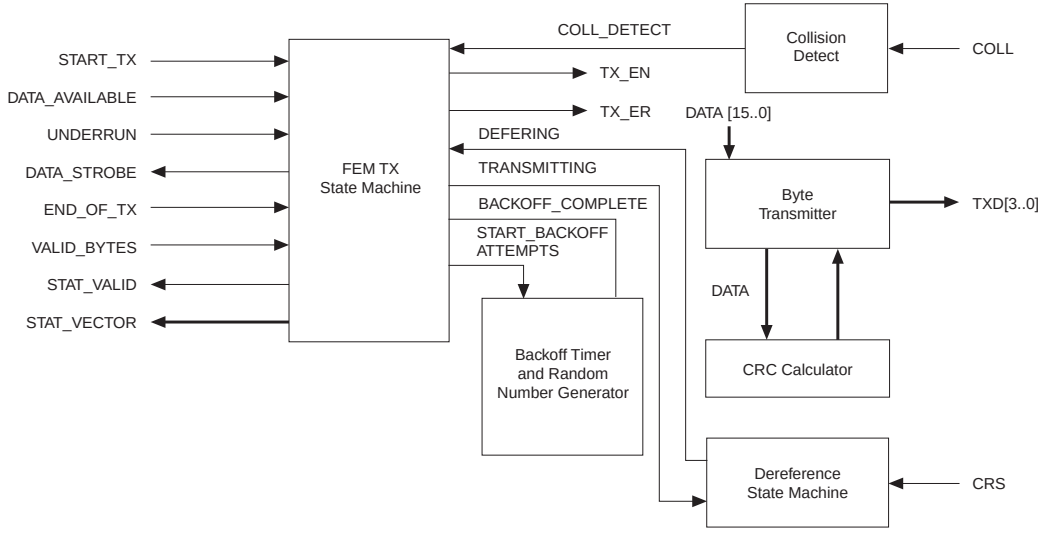
The FEM megafunction has been independently tested using an Ethernet-compliant testbench. The fully modular design of the function facilitates easy customization.

The FEM megafunction meets the ***Virtual Socket Interface Alliance version 1.0*** recommendation for a soft virtual component. Compliance is achieved by providing a detailed and comprehensive specification, a theory of operation document, a clearly defined and modeled user interface, a programmable Ethernet-compliant testbench, and compilation and synthesis scripts.

Block Diagram

Figure 18 shows the block diagram for the fast Ethernet media access controller transmitter megafunction.

Figure 18. FEM Access Controller Transmitter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	805	0	45 MHz	Contact CoreEl Microsystems

10/100 Ethernet Media Access Controller

Vendor: Stargate Solutions
Target Application:
Graphics, industrial controls, networking, telecommunications
ID Code: 6B8A-E1000

- Simple request/acknowledge application interface
- IEEE Std. 802.3-compatible and supports IEEE Std. 802.3x and
- IEEE Std. 802.3Q for flow control
- Optional two-part deferral
- Full and half duplex
- Automatic retries after collision
- Automatic padding and removal of the padded bytes to meet the frame size requirement
- RMII, MII management interface
- Frequency conversion subsystem (FCS) generation and check-on received packets
- MDIO interface
- Programmable address filtering

General Description

The Ethernet MAC controller megafunction provides a simple data interface to receive and transmit data, as well as an interface to program the fast Ethernet controller. The megafunction has standard MII and MDIO interfaces to the physical layer, and handles synchronization of data and configuration across the application and physical layer clocks. The 10/100 Ethernet MAC controller supports features such as multiple retries, address check, loop back monitor, and flow control.

The 10/100 Ethernet MAC controller includes the building blocks described in Table 1.

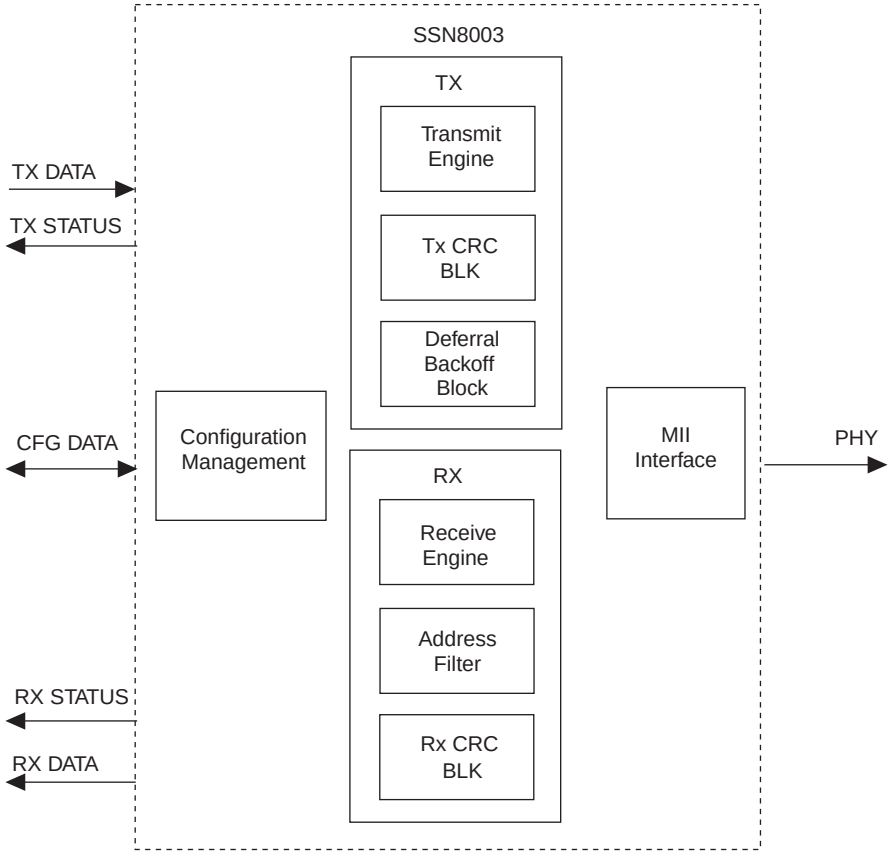
Table 1. System Building Blocks in the 10/100 Ethernet MAC Controller Megafunction

System Block	Description
MII Interface	The MII interface handles the MII communication protocol with the physical layer (PHY). The interface also performs a loop-back feature and sends a Jam™ sequence upon request from the application.
Transmit Engine	The transmit engine block allows the application to receive data as bytes. The data is then forwarded to the MII interface as nibbles. The engine controls back-off state machines and deferral state machines, as well as appends cyclic redundancy code (CRC) checks to the packet. Also, the engine appends padding to the packet base and generates the status for the packet transmitted.
Back-off and Deferral Block	This block performs back-off algorithms to retry the packet on collision. It also performs deferrals based on the carrier sense, allowing the next packet to be sent after the deferral time.
Transmit CRC Block	The transmit CRC block packet generates the CRC that needs to be appended to the packet. The Ethernet MAC controller uses a 32-bit CRC as specified in IEEE Std. 802.3 specification.
Receive Engine	The receive engine block gathers the data provided by the MII block and sends it to the application. It performs several operations on the data received, including padding and detecting pause packet status generation for the packet received.
Address Filtering Block	The address filtering block checks for the address of the packet being received. It checks the destination address field of the packet to detect uni-cast address, multi-cast address, and broadcast address. A mask register is provided to enable partial address checks on the received packet. This block has programmable registers for the address that need to be checked.
Receive CRC Block	The receive CRC block checks the CRC of the packet received and reports it to the receive engine. The receive engine then provides a status to the application.
Configuration Management Block	The configuration management block contains all the programmable registers to control the functionality of the MAC. These registers control the transmit and receive blocks.

Block Diagram

Figure 19 shows the block diagram for the 10/100 Ethernet media access controller megafunction.

Figure 19. 10/100 Ethernet Media Access Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50E	-1	2,035	0	25 MHz	Contact Stargate Solutions

Cell Delineation A

Vendor: CoreEl MicroSystems
Target Application: Data communications, telecommunications
ID Code: C08E-A120

CoreEl MicroSystems

- Octet-wide operation
- Byte-boundary detection
- Delineation state machine with hunt, presync, and sync states
- Correction and detection states within the sync state
- Out-of-cell-delineation indication
- Idle cell discard
- Header error control (HEC) verification with single-bit and multiple-bit error detection
- Indication upon an uncorrectable error (cell discard)
- Optional cell descrambling
- Cell-received and cell-discarded pulse outputs
- Continuous clock with cycle-by-cycle enable

General Description

The cell delineation A (CC200A) megafunction performs the functions required in the receive stream of the transmission convergence sub-layer of an asynchronous transfer mode (ATM) physical layer processor. The function can be used for synchronous optical networking (SONET) or synchronous digital hierarchy (SDH) applications. The input is a non-byte-aligned cell stream containing 53 byte cells with 5 bytes of header and 48 bytes of payload. The CC200A delineates the cells as prescribed in the International Telecommunications Union (ITU) specification I.432.1 and passes out the header and payload.

Functional Description

When the CC200A function begins to process data, the non-byte-aligned input data is aligned in the alignment buffer using the HEC computation results. The HEC computation module checks whether the HEC computed over the first four header bytes matches the data in the fifth byte, using the polynomial specified in ATM UNI 3.1. Eight parallel HEC computations are carried out to determine the byte alignment. The byte-aligned data is then passed through a data buffer and fed to the idle cell detect block, which determines whether the cell is assigned or idle.

Cell delineation is carried out by the cell delineation state machine and the controller block, which controls the mechanism.

The correction mask generator block takes the remainder from the HEC computation module and determines the correction mask that should be applied to the header to correct a single bit error. The descrambler module optionally descrambled only the payload octets using the self-synchronizing polynomial specified in ATM UNI 3.1. This feature is enabled or disabled only on the cell boundary.

Tables 2 and 3 describe the input/output interface signals.

Table 2. Interface Signal Descriptions

Input Signals	Description
reset_b	Active-low asynchronous reset.
data_in[7..0]	Non-byte-aligned input data carrying a continuous stream of 53 byte cells.
clock	Clock of up to 80 MHz compatible with E3, STS-3c, and STS-12c applications.
clockenable	Indicates cycles of the clock during which the module is active.
corr_enable	Active-high command indicating that an attempt is to be made to correct single bit errors in the cell header.
descr_enable	Active-high indication to enable cell descrambling on the cell boundary.

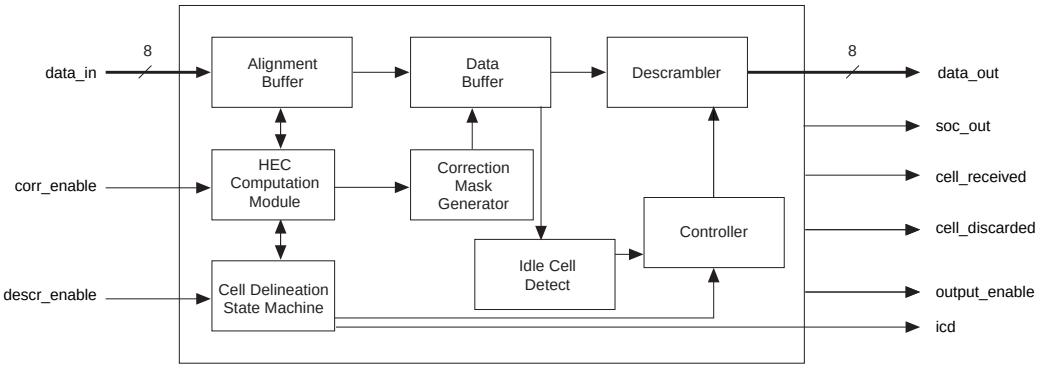
Table 3. Interface Signal Descriptions

Output Signals	Description
output_enable	Active-high signal indicating that data on the output bus is valid in the current clock cycle.
data_out[7..0]	Output data containing 52 byte cells with 4 bytes of header and 48 bytes of payload.
soc_out	Active-high start of cell indication, one clock wide.
cell_received	Active-high indication upon the complete reception of a cell, one clock wide.
cell_discarded	Active-high indication that a cell has been discarded due to a header error, one clock wide.
ocd	Active-high indication during an out of cell delineation.

Block Diagram

Figure 20 shows the block diagram for the cell delineation A megafunction.

Figure 20. Cell Delineation A Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10K	-1	1,149	0	50 MHz	Contact CoreEl Microsystems

Intermediate Data Rate (IDR) Framer/Deframer

Vendor: Integrated Silicon Systems
Target Application: Satellite communications, DVB
Additional Deliverables: Testbench, simulation files, constraint files
ID Code: C38B-1123

- Frame and multiframe synchronization signals
- Four backward alarm signals
- Single voice channel of 8 Mbps
- Two voice channels of 32 Mbps
- Compatible IESS-308

General Description

The ISS IDR framer/deframer megafunction performs engineering service circuit (ESC) channel data, voice, and alarm extraction, along with frame synchronization signal detection. The recovered data streams are buffered and then clocked out at different rates. Clock signals for the slower data rate signals are generated. Four clock rate combinations are supported. Both input data rate and composite data rate clocks must be supplied at the exact frequency ratios defined by IESS-308.

Synchronous Detection

The incoming data stream is sampled one bit at a time, over a succession of frames. If no synchronization pattern is detected within 16 frames at that bit position, a bit is skipped and synchronization detection moves on to the next bit position. Once a valid synchronization is detected, frame data extraction begins on the next superframe. The `InSync` signal will be asserted when the initial data appears on the `DataOut` pin. In the absence of transmission bit errors, synchronization will be achieved within a time specified by the following formula.

$$\text{SyncTime} = \texttt{CrClk}\ \text{period} \times 16 \times (\text{TotalBitsPerFrame})^2$$

Data FIFO Buffer

Input data is loaded into an asynchronous FIFO buffer for data rate conversion. No data is loaded when frame overhead bits are being received. Data bits are extracted from the FIFO buffer at the intermediate rate, and output to the `DataOut` pin.

ESC Data Clocks and Buffers

The composite rate clock, `CrClk`, derives the clock signals for the ESC voice channels, ESC data channels, and ESC alarm signals. These signals have defined frequencies. Data for the relevant channel is loaded into small buffers on receipt from the composite stream. Data is removed from the buffers a maximum of two frames later, on the rising edge of the relevant clock signal, and driven onto the appropriate output pin.

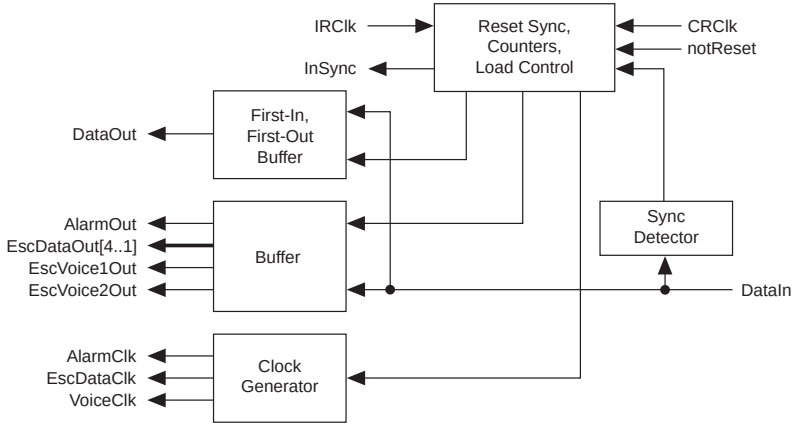
Counters & Buffer Load Control

A number of counters keep track of the frame, subframe, and bit number, and control the input stream disassembly. IESS-308 does not specify a relationship between the content of the data streams and the framing signals. The equipment connected to the data streams is responsible for synchronizing to the data carried in those streams.

Block Diagram

Figure 21 shows the block diagram for the IDR framer/deframer megafunction.

Figure 21. IDR Framer/Deframer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	171	0	60 MHz	Framer
		205	0	83 MHz	Deframer

Universal Digital Data Acquisition Megafunction

Vendor: PLD Applications
Target Application: Video, audio, scientific, process monitoring, digital data processing, high-speed data transfer applications, CNA, digital control/command, real-time applications
ID Code: 73E2-DAC0

- Up to 44 configurable I/O ports
- Available resources for user-added custom digital processing functions
- Real-time, ultra-high speed digital data acquisition
- Two programmable 16-bit counters
- Two programmable timers
- Two configurable signal generators (pulse, clock)
- Pulse counters
- Two 8-bit UARTs operated via RS232, RS485, or custom protocol
- Embedded external FLEX device configuration engine
- All resources operated from 33 MHz or 66 MHz, 32- or 64-bit PCI bus
- PCI megafunction fully complies with Peripheral Component Interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***
- Functions are optimized for the APEX 20K and FLEX 10K device architectures.
- Data acquisition performed at full PCI bandwidth (up to 528 Mbps peak)
- PCI back-end transfers are operated through bidirectional embedded first-in-first-out (FIFO) buffers
- Sustained transfer rate of overall acquisition is not limited by the PCI bus
- Fully customizable PCI megafunction and data acquisition functions

General Description

The universal digital data acquisition megafunction contains most of the digital data acquisition functions found on the market. It also integrates the latest version of PLD Applications PCI master-target interface megafunction, which can be configured for 32 bits or 64 bits, 33-MHz, or 66-MHz operation. The PCI bus interface megafunction is used for high-speed data transfers and real-time computing applications.

The data acquisition megafunction can be fully parameterized via the PCI bus and a provided end-user software. Users can select which function they want to use, operate the functions, and collect the results on their compact PCI bus.

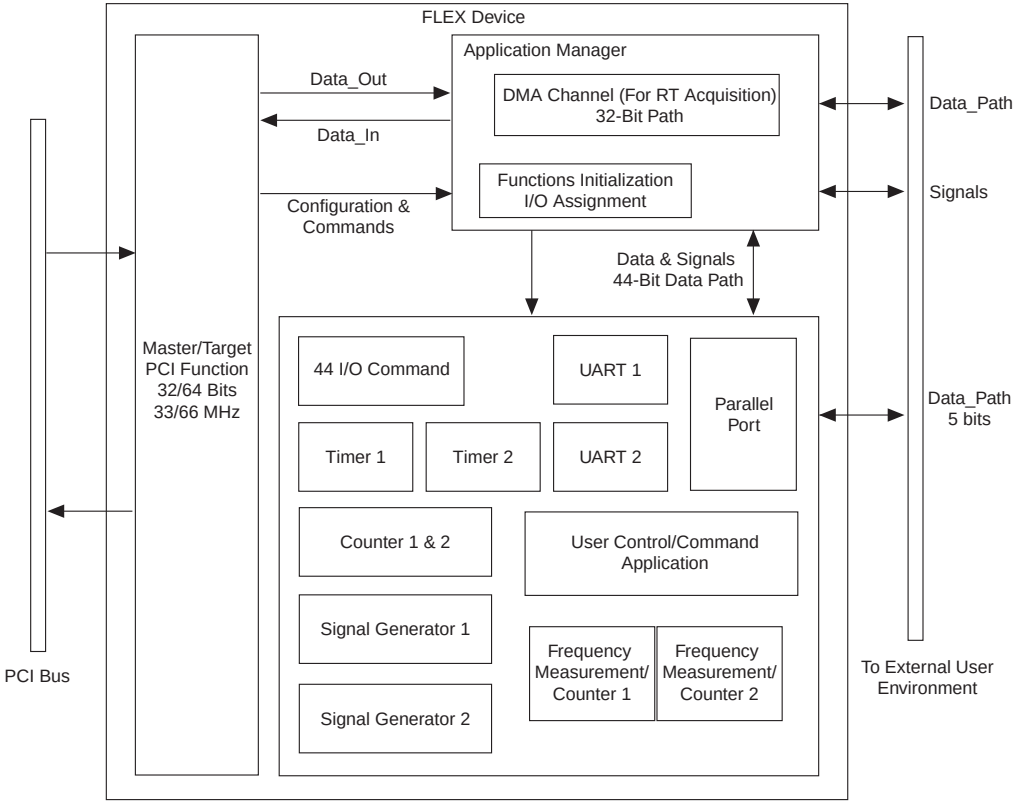
The compact PCI data acquisition megafunction implements a direct path (real-time acquisition input/output channel), which is used for high-speed sustained digital acquisition and directly connects the PCI bus and the external bus. A second path is used to initialize, control, and monitor each embedded data acquisition function.

The data acquisition megafunction benefits from a wide portfolio of digital functions with the power and flexibility of the PCI bus.

Block Diagram

Figure 22 shows the block diagram for the universal digital data acquisition megafunction.

Figure 22. Universal Digital Data Acquisition Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	–	2,000	0	528 Mbps	Contact PLD Applications

Communication Design Services (ACAP Partners)

The following table lists the ACAP partners who offer design services for communications.

Partner	Expertise								Services					
	ATM/UTOPIA	SONET/SDH/PDH	T1/E1	HDLC	Ethernet	Satellite Communications	Cellular Systems	Telephony	IP Integration	ASIC Conversion	Software Development	Board Design	Board Manufacturing	Board Products
Advanced Logical Design, Inc. 12280 Saratoga-Sunnyvale Rd. #201 Saratoga, CA 95070 Tel. (408) 446-1004	✓			✓	✓							✓	✓	
Applied Microelectronics Inc. 1046 Barrington Street, Halifax Nova Scotia, Canada, B3H 2R1 Tel. (902) 421-1250 **Offering:** Expertise in UTOPIA 1, 2, and 3 interfaces.	✓					✓	✓		✓	✓	✓	✓	✓	✓
Bright Design Services 10436 NE 112th Street Seattle, WA 98033 Tel. (425) 576-1524	✓					✓			✓	✓	✓	✓		
DesignPRO Inc. 35 Stafford Road, Unit 1 Nepean, Ontario, Canada, K2H 8V8 Tel. (613) 596-5030 **Offering:** Reusable blocks, including ATM and packet over SONET/SDH (OC3c, OC12c, and OC48c), UTOPIA level 1, 2, and 3, and 8-bit and 32-bit PPP.	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		

Partner	Expertise								Services					
	ATM/UTOPIA	SONET/SDH/PDH	T1/E1	HDLC	Ethernet	Satellite Communications	Cellular Systems	Telephony	IP Integration	ASIC Conversion	Software Development	Board Design	Board Manufacturing	Board Products
Coded Solutions Pty Ltd 65 Johnston Street Annandale, NSW 2038 Australia Tel. (61) 2 9518 7011		✓	✓								✓	✓		
DMC Manufacturing, Inc. 7025 Central Highway Pennsauken, NJ 08109 Tel. (609) 665-5400 **Offering:** Experience with design optimization and integration of the Altera design with the printed circuit board for increasing performance, improving manufacturing, and easing testing.												✓	✓	✓
Eberwein & Associates, Inc. 9449 Briar Forest, #507 Houston, TX 77063 Tel. (713) 784-1226					✓							✓		
Gid'el Ltd. 14 Ein Ayyala ISRAEL 30825 Tel. (972)-6639-1708	✓					✓			✓	✓	✓	✓		
Innovative Configuration, Inc. (ICI) 712 via Palo Alto Aptos, CA 95003 Tel. (831) 688-6917	✓			✓	✓		✓	✓	✓	✓	✓	✓		
Intrinsix 33 Lyman St. Westboro, MA 01581 Tel. (508) 836-4100	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
I/O Consulting A/S Gaaseagervej 6 DK-8250 Egaa Tel. (45) 87 43 80 74					✓				✓	✓	✓	✓	✓	

Partner	Expertise								Services					
	ATM/UTOPIA	SONET/SDH/PDH	T1/E1	HDLC	Ethernet	Satellite Communications	Cellular Systems	Telephony	IP Integration	ASIC Conversion	Software Development	Board Design	Board Manufacturing	Board Products
Locke's Digital Developments Ltd. New Street, Marnhull, Dorset, England. DT10 1PY Tel. (44) 0 1258 821 222					✓			✓	✓	✓	✓	✓		
Mettrix Technology Corporation 25 Corporate Park Drive, Suite C Hopewell Junction, NY 12533 Tel. (914) 897-4960					✓			✓	✓	✓	✓	✓	✓	✓
Norton Engineering Consultants 2307 Damuth Street Oakland, CA 94602 Tel. (510) 482-1818 **Offering:** Expertise includes router and switch design, verilog/simulation/synthesis.	✓	✓	✓	✓	✓				✓			✓	✓	✓
Northwest Logic Design, Inc. 1905 NW 169th Place, Suite 121 Beaverton, OR 97006 Tel. (503) 533-5800	✓	✓	✓		✓	✓		✓	✓		✓	✓		
Nova Electronic Design & Analysis Corporation 459B Carlisle Drive Herndon, VA 20170 Tel. (703) 618-2877	✓		✓	✓	✓			✓	✓		✓	✓		
RTI 10560 Main St., Ste. 417 Fairfax, VA 22030 Web. **http://www.rti-world.com** Tel. (703) 293-9662 **Offering:** Experience in the development of FDDI and ATM hardware as well as TDMA processing and GSM communication			✓	✓	✓	✓	✓	✓		✓	✓			

Partner	Expertise								Services					
	ATM/UTOPIA	SONET/SDH/PDH	T1/E1	HDLC	Ethernet	Satellite Communications	Cellular Systems	Telephony	IP Integration	ASIC Conversion	Software Development	Board Design	Board Manufacturing	Board Products
Sam Lowenstein & Associates 118 Melody Lane, SW Vienna, VA 22180 Tel. (703) 724-2082	✓	✓	✓	✓	✓	✓		✓				✓		
SyncAccess, Inc. 5279 Folsom Blvd. Sacramento, CA 95819 Web. **http://www.syncaccess.com** Tel. (916) 457-4838 Fax. (916) 456-8505	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓		✓
Vulcan ASIC Ltd., Unit 6, The Maltings, Royston, Herts, SG8 5DY, England Tel. (44) 0 1763 248163	✓	✓			✓				✓	✓	✓			

PCI & Other Bus Interfaces

September 1999

Overview

Implementing a bus interface function that meets design specifications is a challenging task that requires considerable design expertise. Altera offers pre-synthesized and pre-verified solutions for standard serial and parallel buses. Megafunctions can shorten the development cycle dramatically, not only during the design entry phase using the OpenCore™ feature, but also during the simulation phase with hardware-proven solutions and testbenches. Altera and its Altera Megafunction Partner Program (AMPP℠) partners also have the expertise to provide drivers for complex bus protocols such as peripheral component interconnect (PCI), 1394, and universal serial bus (USB).

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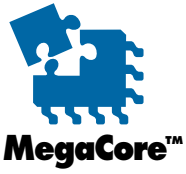
32-Bit, 33-MHz PCI Master/Target Interface

Vendor: Altera
Target Application: All PCI-based systems
Additional Deliverables: PCI Master/Target MegaCore Function DMA Data Sheet, FLEX 10K PCI Prototype Board Data Sheet, Prototype Board
Ordering Code: PLSM-PCI/A



- `pci_a` MegaCore™ function implementing a 32-bit peripheral component interconnect (PCI) master/target interface
- Optimized for the APEX™ 20K and FLEX® 10K architectures
- Extensive hardware testing using:
  - HP E2925A PCI Bus Exerciser and Analyzer
  - FLEX 10K PCI prototype board
  - Validated against common PCI chipsets such as: Intel 430 and 440 chipsets, and DEC PCI-to-PCI bridges
- Dramatically shortens design cycles
- Includes a FLEX 10K PCI prototype board
- Includes test vectors for user simulation
- OpenCore feature allows designers to instantiate and simulate designs in the Quartus™ and MAX+PLUS® II software prior to licensing
- Uses approximately 1,000 FLEX logic elements (LEs), e.g., 35% the capacity of an EPF10K50 device
- PCI master features:
  - Memory read/write
  - Bus parking
  - Fully integrated direct memory access (DMA) engine including address counter register, byte counter register, control and status register, and interrupt status register
  - Configurable interrupt source, including DMA terminal count, master abort, target abort, and local side interrupt
  - 64-byte (16 double words or DWORDs) RAM buffer implemented in FLEX 10K embedded array blocks (EABs)
  - Zero-wait-state PCI read and write burst transactions
- PCI target features:
  - Type zero configuration space
  - Parity error detection
  - Memory read/write and configuration read/write
  - Target retry and disconnect
  - 1 Mbyte to 2 Gbytes of parameterized target memory space
- Configuration registers:
  - Parameterized: device ID, vendor ID, class code, revision ID, base address zero, subsystem ID, subsystem vendor ID
  - Non-parameterized: command, status, header type, latency timer, interrupt pin, interrupt line

General Description

The pci_a MegaCore function provides a timely solution for integrating 32-bit PCI peripheral devices, and is fully tested to meet the requirements of the PCI specification. The pci_a function is optimized for the APEX 20K and FLEX 10K device families, reducing the design task and enabling designers to focus efforts on the custom logic surrounding the PCI interface.

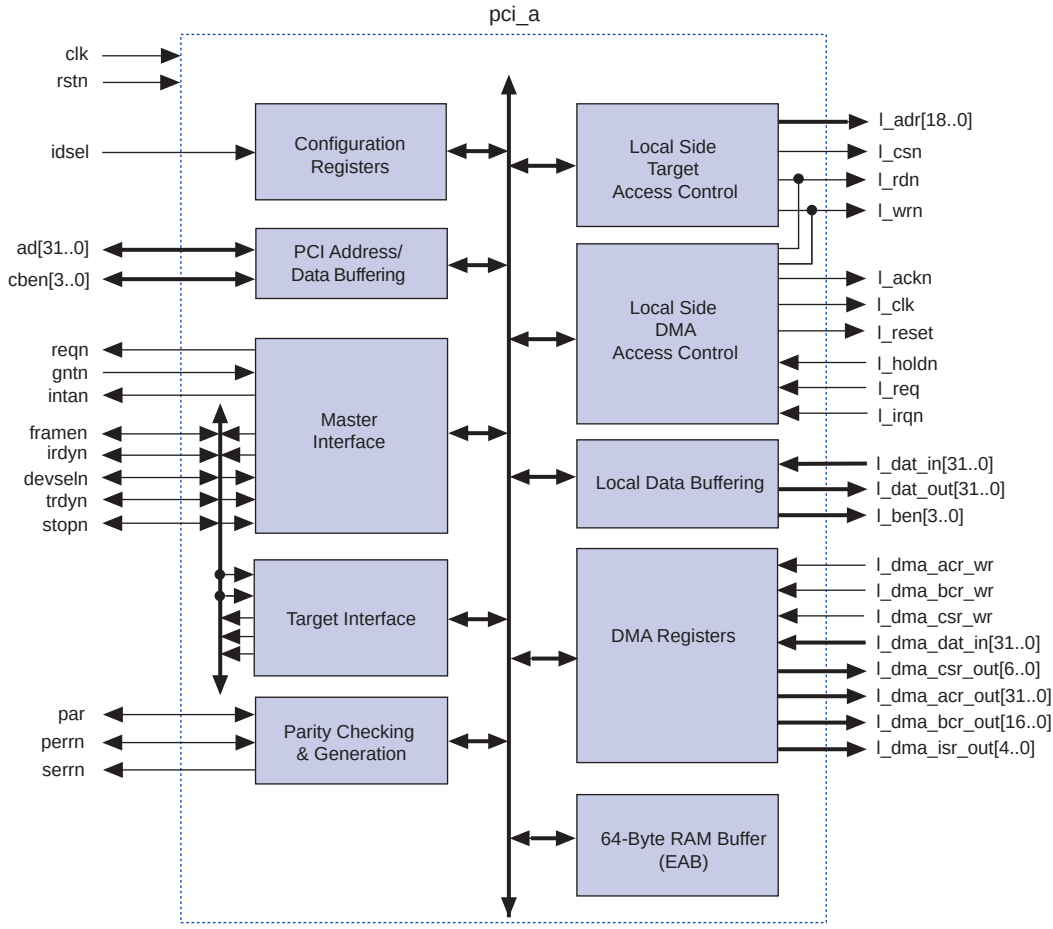
Functional Description

The pci_a function consists of three main components:

- A defined 64-byte PCI bus configuration register space and master control logic
- PCI bus target interface control logic, including target decode and register read/write signals
- Embedded DMA control engine, which operates with four registers and includes a 64-byte (16 DWORD) RAM buffer, and local side interface DMA control logic, including read/write control and PCI bus arbitration for master/target accesses

Figure 1 shows the block diagram for the pci_a MegaCore function.

Figure 1. pci_a Megafunction Block Diagram

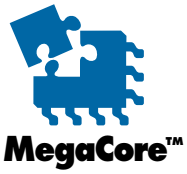


Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K100E	-1	1,060	4	60 MHz	Default

32-Bit, 33-MHz PCI Bus Master/Target Interface

Vendor: Altera
Target Application: All PCI-based systems
Additional Deliverables: pci_b MegaCore Function User Guide
Ordering Code: PLSM-PCI/B



- A flexible general-purpose interface that can be customized for specific peripheral requirements
- Dramatically shortens design cycles
- Fully compliant with the peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** timing and functional requirements
- Extensively hardware tested using the following hardware and software
  - FLEX 10K PCI prototype board
  - HP E2925A PCI Bus Exerciser and Analyzer
  - Validated against common PCI chipsets, such as the Intel 430-FX and 440-FX, and Intel 21052-AB and 21152-AA PCI-to-PCI bridges
- Optimized for the APEX 20K, FLEX 10K, and FLEX 6000 architectures
- PCI master features:
  - Zero-wait-state memory read/write operation (up to 132 Mbytes per second)
  - Initiates most PCI commands including: configuration read/write, memory read/write, I/O read/write, memory read multiple (MRM), memory read line (MRL), and memory write and invalidate (MWI)
  - Bus parking
  - Independent master operation allows self configuration capability for host bridge applications
- PCI target features:
  - Zero-wait-state memory read/write (up to 132 Mbytes per second)
  - Parity error detection
  - Up to 6 base address registers (BARs) with adjustable memory size and type
  - Capabilities list pointer support, which includes compact PCI Hot Swap support
  - Expansion ROM BAR support
  - CardBus CIS pointer register
  - Most PCI bus commands are supported; interrupt acknowledge, configuration read/write, memory read/write, I/O read/write, MRM, MRL, and MWI
  - Local side can request a target abort, retry, or disconnect
  - Local-side interrupt
- Configuration registers:
  - Parameterized registers: device ID, vendor ID, class code, revision ID, BAR0 through BAR5, subsystem ID, subsystem vendor ID, interrupt pin, maximum latency, minimum grant, capabilities list pointer, CIS pointer, and expansion ROM BAR

- Parameterized default or preset base address (available for all 6 BARs) and expansion ROM base address
- Non-parameterized registers: command, status, header type, latency timer, cache line size, and interrupt line

General Description

The pci_b MegaCore function is a hardware-tested, high-performance, flexible implementation of the 32-bit, 33-MHz PCI master/target interface. Because this function handles the complex PCI protocol and stringent timing requirements internally, designers can focus their engineering efforts on value-added custom development, significantly reducing time-to-market.

Optimized for Altera® APEX 20K, FLEX 10K, and FLEX 6000 architectures, the pci_b function supports configuration, I/O, and memory transactions. With the high density of APEX and FLEX devices, designers have ample resources for custom local logic after implementing the PCI interface. The high performance of FLEX devices also enables the function to support unlimited cycles of zero-wait-state memory-burst transactions, thus achieving 132 Mbytes per second throughput, which is the theoretical maximum for a 32-bit, 33-MHz PCI bus.

In the pci_b function, the master and target interface can operate independently, allowing maximum throughput and efficient usage of the PCI bus. For instance, while the target interface is accepting zero-wait state burst write data, the local logic may simultaneously request PCI bus mastership, thus minimizing latency. In addition, the pci_b function's separate local master and target data paths allow independent data prefetching and posting. Depending on the application, first-in first-out (FIFO) functions of variable length, depth, and type can be implemented in the local logic.

To ensure timing and protocol compliance, the functions have been vigorously hardware tested.

As a parameterized function, pci_b has configuration registers that can be modified upon instantiation. This feature provides scalability, adaptability, and efficient silicon usage. As a result, the same MegaCore function can be used in multiple PCI projects with different requirements. For example, the pci_b function offers up to six base address registers (BARs) for multiple local-side devices. However, some applications require only one contiguous memory range. PCI designers can choose to instantiate only one BAR, which reduces logic cell consumption. After designers define the parameter values, the MAX+PLUS II software automatically and efficiently modifies the design and implements the logic.

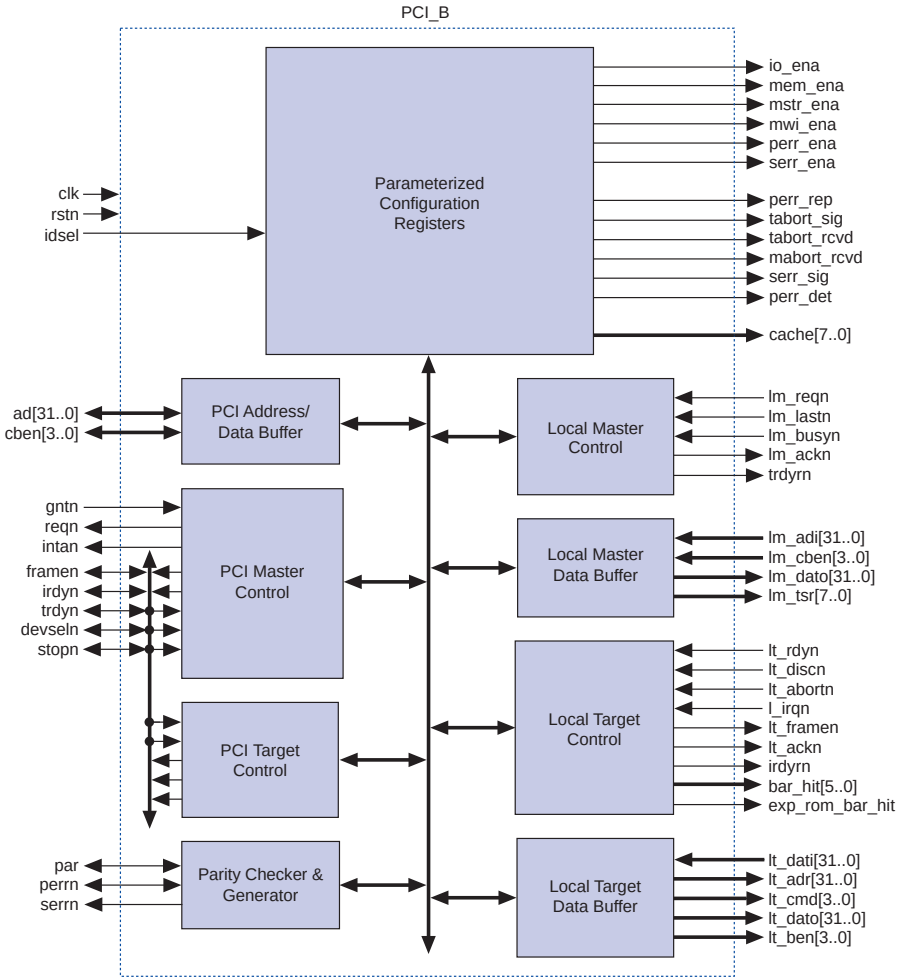
Functional Description

The pci_b function consists of three main elements:

- A parameterized PCI bus configuration register space
- Target interface control logic
- Master interface control logic

Figure 2 shows the block diagram for the pci_b MegaCore function.

Figure 2. pci_b Megafunction Block Diagram

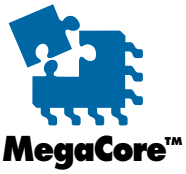


Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K100E	-1	1,052	0	60 MHz	Default

32-Bit, 33-MHz PCI Bus Target Only Interface

Vendor: Altera
Target Application: All PCI-based systems
Additional Deliverables: pcit1 MegaCore Function User Guide
Ordering Code: PLSM-PCIT1



- A flexible general-purpose interface that can be customized for specific peripheral requirements
- Dramatically shortens design cycles
- Fully compliant with the PCI SIG ***PCI Local Bus Specification, Revision 2.2*** timing and functional requirements
- Extensively hardware tested using the following hardware and software
  - FLEX 10K PCI prototype board
  - HP E2925A PCI Bus Exerciser and Analyzer
  - Validated against common PCI chipsets, such as the Intel 430-FX and 440-FX, and Intel 21052-AB and 21152-AA PCI-to-PCI bridges
- Optimized for the APEX 20K, FLEX 10K, and FLEX 6000 architectures
- PCI target features:
  - Zero-wait-state memory read/write (up to 132 Mbytes per second)
  - Parity error detection
  - Up to 6 base address registers (BARs) with adjustable memory size and type
  - Capabilities list pointer support, which includes compact PCI Hot Swap support
  - Expansion ROM BAR support
  - CardBus CIS pointer register
  - Most PCI bus commands are supported; interrupt acknowledge, configuration read/write, memory read/write, I/O read/write, MRM, MRL, and MWI
  - Local side can request a target abort, retry, or disconnect
  - Local-side interrupt
- Configuration registers:
  - Parameterized registers: device ID, vendor ID, class code, revision ID, BAR0 through BAR5, subsystem ID, subsystem vendor ID, interrupt pin, maximum latency, minimum grant, capabilities list pointer, CIS pointer, and expansion ROM BAR
  - Parameterized default or preset base address (available for all 6 BARs) and expansion ROM base address
  - Non-parameterized registers: command, status, header type, latency timer, cache line size, and interrupt line

General Description

The pcit1 MegaCore function is an implementation of the 32-bit, 33-MHz PCI target interface. Because this function handles the complex PCI protocol and stringent timing requirements internally, designers can focus their engineering efforts on value-added custom development, significantly reducing time-to-market.

Optimized for Altera APEX 20K, FLEX 10K, and FLEX 6000 architectures, the pcit1 function supports configuration, I/O, and memory transactions. With the high density of FLEX devices, designers have ample resources for custom local logic after implementing the PCI interface. The high performance of FLEX devices also enables the functions to support unlimited cycles of zero-wait-state memory-burst transactions, thus achieving 132 Mbytes per second throughput, which is the theoretical maximum for a 32-bit, 33-MHz PCI bus.

To ensure timing and protocol compliance, the functions have been vigorously hardware tested.

As a parameterized function, pcit1 has configuration registers that can be modified upon instantiation. This feature provides scalability, adaptability, and efficient silicon usage. As a result, the same MegaCore functions can be used in multiple PCI projects with different requirements. For example, the pcit1 function offers up to six base address registers (BARs) for multiple local-side devices. However, some applications require only one contiguous memory range. PCI designers can choose to instantiate only one BAR, which reduces logic cell consumption. After designers define the parameter values, the MAX+PLUS II software automatically and efficiently modifies the design and implements the logic.

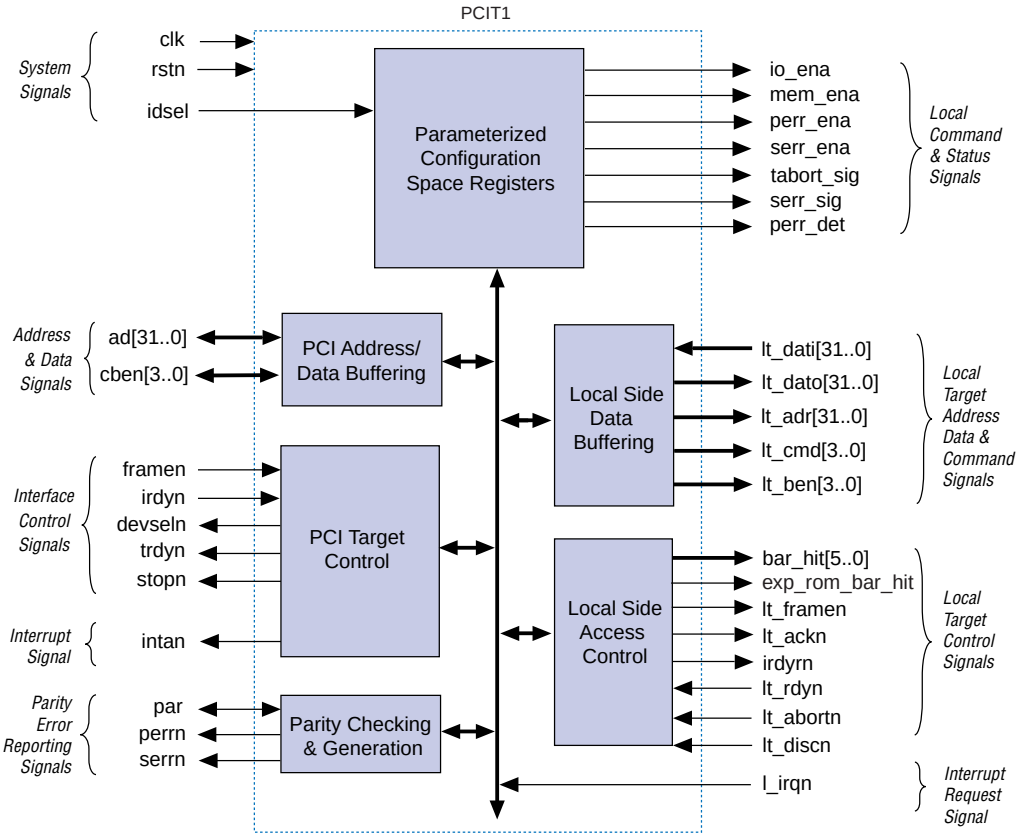
Functional Description

The pcit1 function consists of three main elements:

- A parameterized PCI bus configuration register space
- Target interface control logic

Figure 3 shows the block diagram for the pcit1 MegaCore function.

Figure 3. pcit1 Megafunction Block Diagram

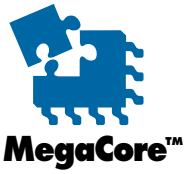


Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K100E	-1	635	0	66 MHz	Default

64-Bit, 66-MHz PCI Master/Target Interface with DMA

Vendor: Altera
Target Application: All PCI-based systems
Additional Deliverables: pci_c MegaCore Function User Guide
Ordering Code: PLSM-PCI/C



- A flexible general-purpose interface that can be customized for specific peripheral requirements
- Dramatically shortens design cycles
- Fully compliant with the PCI SIG ***PCI Local Bus Specification, Revision 2.2*** timing and functional requirements
- Extensively verified using industry-proven Phoenix Technology test bench
- Extensively hardware tested using the following hardware and software
  - HP E2928A PCI Bus Analyzer and Exerciser
  - HP E2920 Computer Verification Tools, PCI series
  - Altera's intellectual property (IP) development board
- Optimized for the APEX and FLEX 10K architectures
- 66-MHz compliant with APEX 20K and FLEX 10KE-1 devices
- No-risk OpenCore feature allows designers to instantiate and simulate designs in the Quartus and MAX+PLUS II software prior to purchase
- PCI master features:
  - Infinite cycles zero-wait state PCI read/write operation (up to 528 Mbytes per second)
  - Initiates most PCI commands including: configuration read/write, memory read/write, I/O read/write, memory read multiple (MRM), memory read line (MRL), memory write and invalidate (MWI)
  - Initiates 64-bit addressing, using Dual-Address Cycle (DAC)
  - Initiates 64-bit memory transactions
  - Initiates 32-bit memory, I/O, and configuration transactions
  - Dynamically negotiates 64-bit transactions and automatically multiplexes data on the local 64-bit data bus
  - PCI bus parking
- PCI target features:
  - Type zero configuration space
  - Capabilities list pointer support
  - Parity error detection
  - Up to six base address registers (BARs) with adjustable memory size and type
  - Expansion ROM BAR support
  - Zero-wait state PCI read/write (up to 528 Mbytes per second)
  - Most PCI bus commands are supported; configuration read/write, memory read/write, I/O read/write, MRM, MRL, and MWI
  - Local side can request a target abort, retry, or disconnect
  - 64-bit addressing capable
  - Automatically responds to 32- or 64-bit transactions
  - Local-side interrupt request

- Configuration registers:
  - Parameterized registers: device ID, vendor ID, class code, revision ID, BAR0 through BAR5, subsystem ID, subsystem vendor ID, maximum latency, minimum grant, capabilities list pointer, expansion ROM BAR
  - Non-parameterized registers: command, status, header type, latency timer, cache line size, interrupt pin, interrupt line

General Description

The `pci_c` MegaCore function is a hardware-tested, high-performance, flexible implementation of the 64-bit PCI master/target interface. This function handles the complex PCI protocol and stringent timing requirements internally, and its backend interface is designed for easy integration. Therefore, designers can focus their engineering efforts on value-added custom development, significantly reducing time-to-market.

Optimized for Altera APEX 20K and FLEX 10K devices, the `pci_c` function supports configuration, I/O, and memory transactions. With the high density of APEX and FLEX devices, designers have ample resources for custom local logic after implementing the PCI interface. The high performance of APEX and FLEX devices also enables the `pci_c` function to support unlimited cycles of zero-wait-state memory-burst transactions. The `pci_c` function can run at either 33-MHz or 66-MHz PCI bus clock speeds, thus achieving 264 Mbytes per second throughput in a 64-bit, 33-MHz PCI bus system, or 528 Mbytes per second throughput in a 64-bit, 66-MHz PCI bus system.

In the `pci_c` function, the master and target interface can operate independently, allowing maximum throughput and efficient usage of the PCI bus. For instance, while the target interface is accepting zero-wait state burst write data, the local logic may simultaneously request PCI bus mastership, thus minimizing latency.

To ensure timing and protocol compliance, the `pci_c` function has been vigorously hardware tested.

As a parameterized function, pci_c has configuration registers that can be modified upon instantiation. These features provide scalability, adaptability, and efficient silicon implementation. As a result, the same MegaCore functions can be used in multiple PCI projects with different requirements. For example, the pci_c function offers up to six BARs for multiple local-side devices. However, some applications require only one contiguous memory range. PCI designers can choose to instantiate only one BAR, which reduces logic cell consumption. After designers define the parameter values, the Quartus and MAX+PLUS II software automatically and efficiently modifies the design and implements the logic.

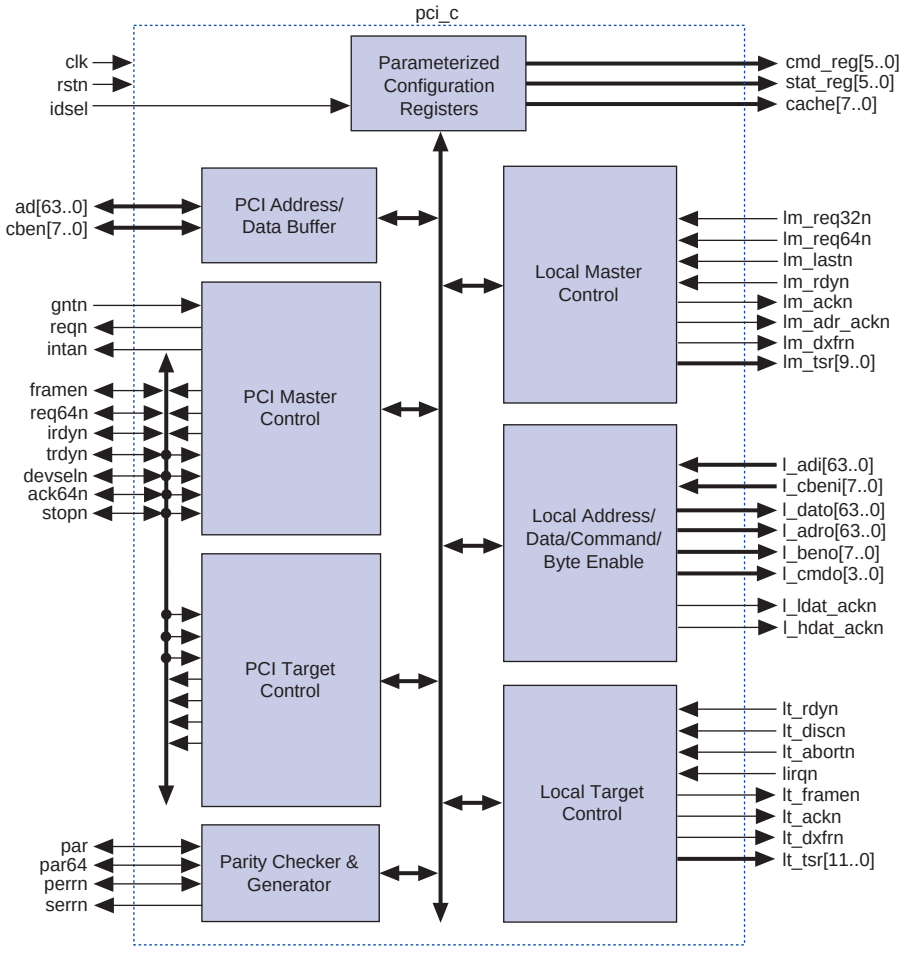
Functional Description

The pci_c function consists of three main elements:

- A parameterized PCI bus configuration register space
- Target interface control logic
- Master interface control logic

Figure 4 shows the block diagram for the pci_c MegaCore function.

Figure 4. pci_c Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K100E	-1	1,235	–	74 MHz	Contact Altera

32-Bit PCI Bus Target Interface

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-A112

- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Supports zero-wait state burst mode data transfer
- Internal write buffer to maximize data bandwidth
- Optional FIFO interface
- 33-MHz operating frequency

General Description

The 32-bit PCI target interface megafunction provides a user-friendly interface between a target device and a PCI bus. This megafunction is a very compact design that minimizes logic cell count while providing a high-bandwidth data transfer. The megafunction performs all data transfer functions requested by the PCI bus master. To maximize data bandwidth, the megafunction provides an internal write buffer and supports burst mode data transfer. All PCI configuration requests are processed locally by the megafunction.

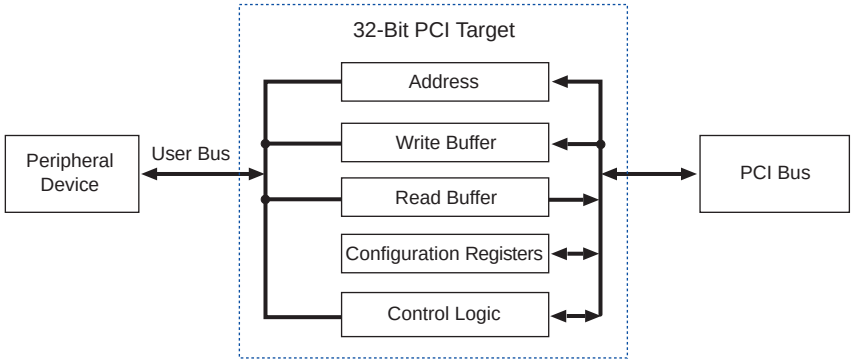
Modifiable Parameters

The megafunction is available in Altera Hardware Description Language (AHDL), Verilog HDL, VHDL, and netlist format. Eureka Technology can customize the megafunction to meet user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 5 shows the block diagram for the 32-bit PCI target interface megafunction.

Figure 5. 32-Bit PCI Target Interface Megafunction Block Diagram

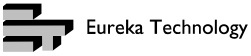


Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10	-3	310	0	33 MHz	Non-burst target design
EPF6016	-2	310	–	33 MHz	Non-burst target design

32-Bit PCI Bus Master/Target Interface

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-B040



- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Supports zero-wait state burst data transfer
- Provides bus initiator and target capability
- 33-MHz operating frequency

General Description

The 32-bit PCI master/target interface megafunction is a flexible interface between a bus master device, such as a DMA controller or video coprocessor, and the PCI bus. The megafunction supports high bandwidth data transfer up to 133 Mbytes per second. All PCI configuration registers are included in the megafunction, and configuration requests are processed locally by the megafunction.

This megafunction also includes PCI target capability, which is useful for transferring data as a target and for setting up the control register of a bus mastering device.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format.

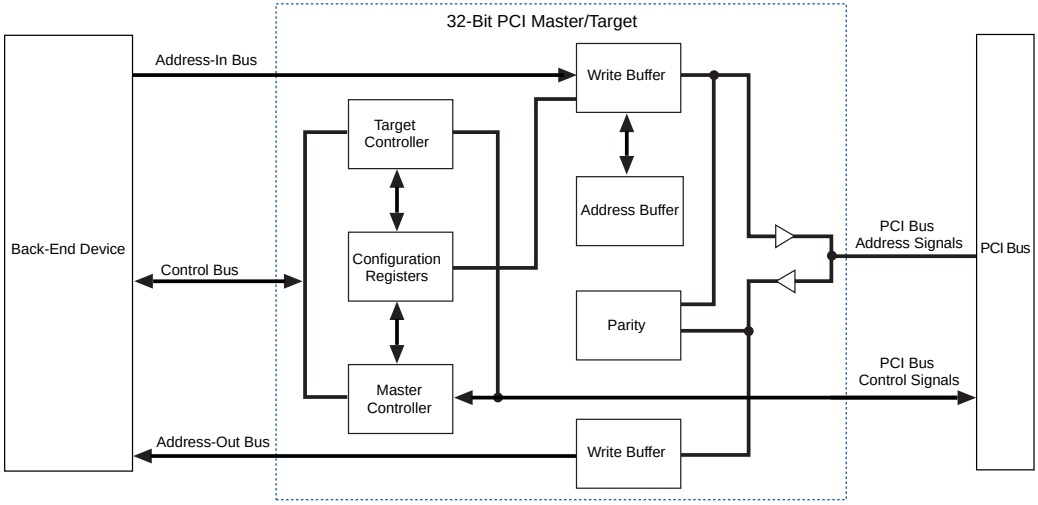
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 6 shows the block diagram for the 32-bit PCI master/target interface megafunction.

Figure 6. 32-Bit PCI Master/Target Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	650	0	33 MHz	Contact Eureka Technology
EPF6016	-2	650	–	33 MHz	Contact Eureka Technology

32/64-Bit PCI Bus Master/Target Interface

Vendor: PLD Applications
Target Application: DSP, high-speed data transfer applications, bus migration, technology migration
Additional Deliverables: CompactPCI, CardBus, PCI Master/Target Core User Guide, Getting Started Guide, PCI VHDL Testbench User Guide, encrypted VHDL files with unlimited/unrestricted authorization code, optimized ACF files, testbench simulation scripts and output logs, example ALTERA .SCF simulation waveform, example VHDL backend applications, PCI MegaWizard, PCI and CompactPCI prototyping board (optional), one year warranty and technical support including new releases and upgrades
ID Code: 73E2-A464

- 32-bit or 64-bit, 33-MHz or 64-MHz PCI function
- Supports 64-bit addressing
- Fully synchronous design
- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Optimized for Altera APEX 20K, FLEX 10K, and FLEX 6000 architectures
- Suitable for application-specific integrated circuit (ASIC) conversion
- Extensively tested on hardware (on multiple chipsets including Ali, SiS, Intel HX, TX, LX, BX, FX, Digital66, DEC)
- Supports zero-wait state unlimited burst transfers up to 528 Mbytes per second.
- Can burst up to 16 Mbytes of data, with zero-wait states
- Supports all six configurable BARs and Expansion ROM Base Address
- Includes support for CardBus and CompactPCI
- Unlimited address space size (memory or I/O), up to 4 Gbytes
- Automatic re-iteration of interrupted transactions
- Supports four independent DMA channels configurable from the PCI side and local side
- Generates all existing PCI commands
- Performs 64-bit addressing with dual-address cycle
- Dynamically negotiate 32-bit/64-bit transactions
- Controls byte enables from the local side
- Flexible local-side interface with embedded FIFO and SRAM control signals
- Plug-n-Play configuration registers can be hardwired for operation in closed-systems
- Generates RETRYs, DISCONNECTs, and TARGET ABORTs from the local side (target operation)
- Inserts wait-states from the local side (target operation)
- Medium-speed target decoder
- Supports fast back-to-back accesses (target operation)
- Inserts configuration space registers from the local side
- Implements a user-configurable general-purpose mailbox register
- Supports one configurable interrupt line
- Free back-end reference designs available

General Description

The PCI bus master/target interface megafunction is a 32/64-bit, 33/66-MHz PCI bus interface that is suitable for high-speed data transfer applications.

The PCI bus master/target interface megafunction provides a simple and flexible interface between the PCI bus and a user-developed back-end design. The megafunction comes with a set of VHDL back-end reference designs that designers can use as-is and can be customized for their own projects. These reference designs include interfaces that use FLEX 10K embedded array blocks (EABs) as a synchronous SRAM buffer or as a FIFO buffer. The PCI bus master/target interface megafunction is fully parameterizable.

The megafunction has a built-in DMA controller that interfaces with either internal EAB memory (SRAM or FIFO) or external memory. DMA operations can be programmed through software or by the user application's logic.

The megafunction has been intensively simulated with PLD Applications' PCI VHDL testbench and hardware tested using PLD Applications' commercialized PCI prototyping cards.

Modifiable Parameters

The following megafunction parameters can be modified using PLD Applications PCI Wizard:

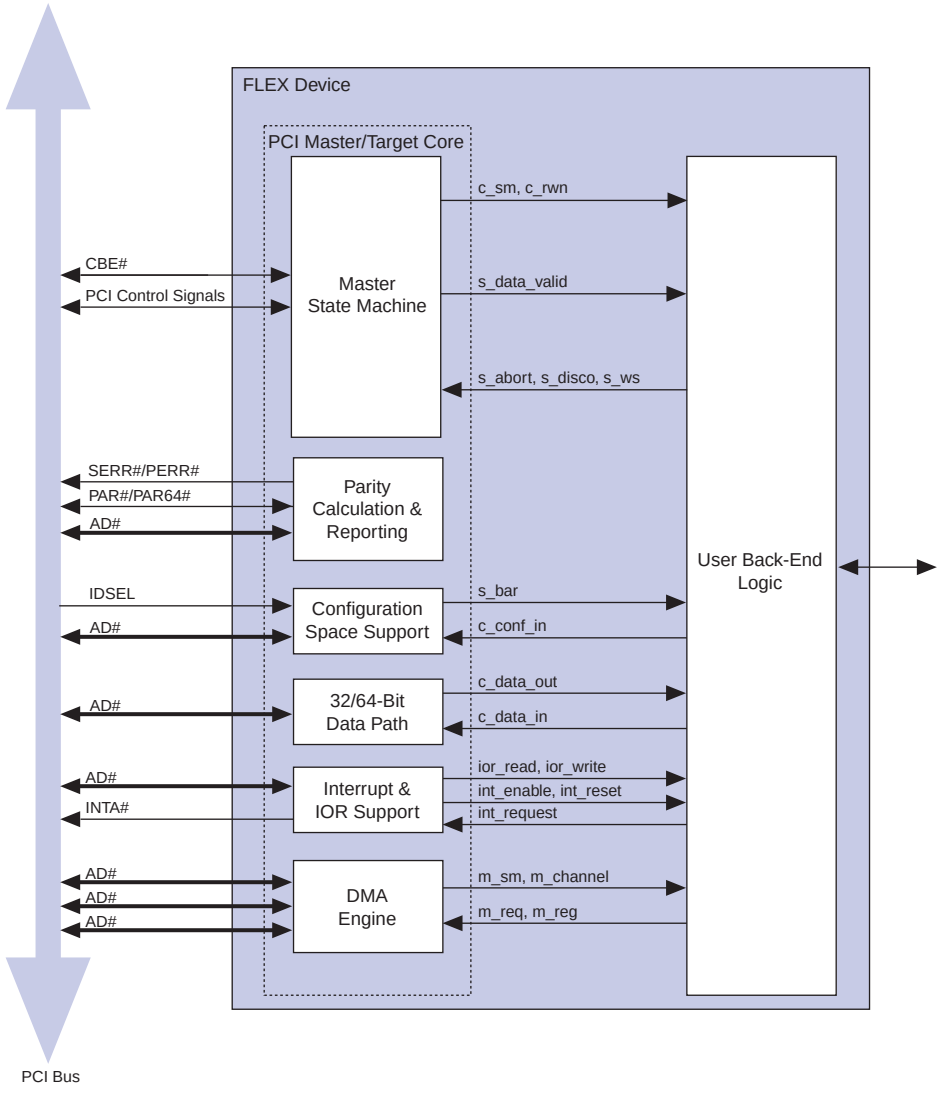
Modifiable Parameters

Parameter	Description
DPS/CPS:	Data (CBE) path size
CNF_DID_VID:	Vendor ID/Device ID
CNF_SUBSYS_DID_VID:	Subsystem Vendor ID/Device ID
CNF_CCODE_REVID:	Class code ID/Revision number
CNF_CARDBUS_PTR:	CardBus CIS pointer
CNF_CAPABILITY_PTR:	CompactPCI capability pointer
CNF_66_CAPABLE:	66-MHz capable flag
CNF_INTERRUPT_PIN:	Interrupt pin select
CNF_MEMORY_ENABLE:	Memory enable bit preset
CNF_IO_ENABLE:	I/O enable bit preset
CNF_PARITY_REPORTING:	Parity error reporting enable bit preset
BARn_SIZE:	BAR0 to BAR5 space size
BARn_PARAM:	BAR0 to BAR5 space attributes
ROMBAR_SIZE:	ROM base address size
ROMBAR_ADDR:	ROM base address preset
CNF_INTERRUPT_LINE:	Interrupt line preset
DAC_ENABLE:	DAC support
CNF_MASTER_ENABLE:	Master enable bit preset
CNF_LATENCY_TIMER:	Latency timer preset
CNF_MAX_LATENCY:	Maximum latency register preset
CNF_MIN_GRANT:	Minimum grant register preset
DMAn_SIZE:	DMA channel 0 to 3 buffer size
DMA_MAX_SIZE:	Maximum DMA channel buffer size
DMA_64ADDR:	64-bit addressing enable

Block Diagram

Figure 7 shows the block diagram for the 32/64-bit PCI master/target megafunction.

Figure 7. 32/64-Bit PCI Master/Target Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-2	50	0	>33 MHz	DAC_ENABLE = 0 (no DAC support)
EPF10K30E	-3	50	0	>66 MHz	DMA0_SIZE = 8 (1KB DMA buffer size)
EPF10K50	-3	50	0	>33 MHz	BAR0_SIZE = 15 (32 Kbytes of memory space)
EPF10K50V	-2	50	0	>33 MHz	DMA_64ADDR = 0 (no 64-bit address)
EPF10K100B	-3	50	0	>33 MHz	
EPF10K130E	-2	50	0	>66 MHz	
EPF10K200E	-2	50	0	>66 MHz	
EPF6016	-3	50	–	>33 MHz	*(1)*
EPF6024A	-2	50	–	>33 MHz	*(2)*

Notes:
(1) 66-MHz compliance on only FLEX 10KE-1 devices.
(2) Same performances in 64-bit mode.

32/64-Bit PCI Bus Target Interface

Vendor: PLD Applications
Target Application: DSP, high-speed data transfer applications, bus migration, technology migration
Additional Deliverables: PCI Master/Target Core User Guide, Getting Started Guide, PCI VHDL Testbench User Guide, PCI core encrypted VHDL files with unlimited/unrestricted authorization code, optimized ACF files, testbench simulation scripts and output logs, example ALTERA .SCF simulation waveform, example VHDL backend applications, PCI MegaWizard, PCI and CompactPCI prototyping board (optional), one year warranty and technical support including new releases and upgrades
ID Code: 73E2-A364

- 32/64-bit, 33/64-MHz PCI function
- Supports 64-bit addressing
- Fully synchronous design
- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Optimized for Altera APEX 20K, FLEX 10K, and FLEX 6000 architectures
- Suitable for ASIC migration
- Extensively tested on hardware (on multiple chipsets including Ali, SiS, Intel HX, TX, LX, BX, FX, Digital66, and DEC)
- Supports zero wait-state unlimited burst transfers up to 528 Mbytes per second
- Bursts up to 16 Mbytes of data, with zero wait-states
- Supports all six configurable BARs and expansion ROM base address
- Includes support for CardBus and CompactPCI
- Unlimited address space size (memory or I/O) up to 4 Gbytes
- Dynamically negotiates 32-bit/64-bit transactions
- Generates RETRYs, DISCONNECTs, and TARGET ABORTs the local side
- Inserts wait-states from the local side
- Medium-speed decoder
- Supports fast back-to-back accesses
- Inserts configuration space registers from the local side
- Implements a user-configurable general-purpose mailbox register from the local side
- Supports one configurable interrupt line
- Plug-n-Play configuration registers can be hardwired for operation in closed-systems
- Free back-end reference designs available

General Description

The PCI bus target interface megafunction is a 32/64-bit, 33/66-MHz PCI bus interface that is suitable for high-speed data transfer applications.

The PCI bus target interface megafunction provides a simple and flexible interface between the PCI bus and a user-developed back-end design. The megafunction comes with a set of VHDL back-end reference designs that designers can use as-is and customize for their own projects. These reference designs include interfaces that use FLEX 10K EABs as a synchronous SRAM buffer or as a FIFO buffer. Another back-end design realizes the interface to an external SRAM buffer.

In addition to all of the required target features, the megafunction supports 64-bit addressing, handles one interrupt line, supports fast back-to-back accesses, and implements a 32-bit user-configurable generic mailbox port.

The megafunction has been intensively simulated using PLD Applications' PCI VHDL testbench, and hardware tested using PLD Applications' commercialized PCI prototyping cards.

Modifiable Parameters

The following megafunction parameters can be modified:

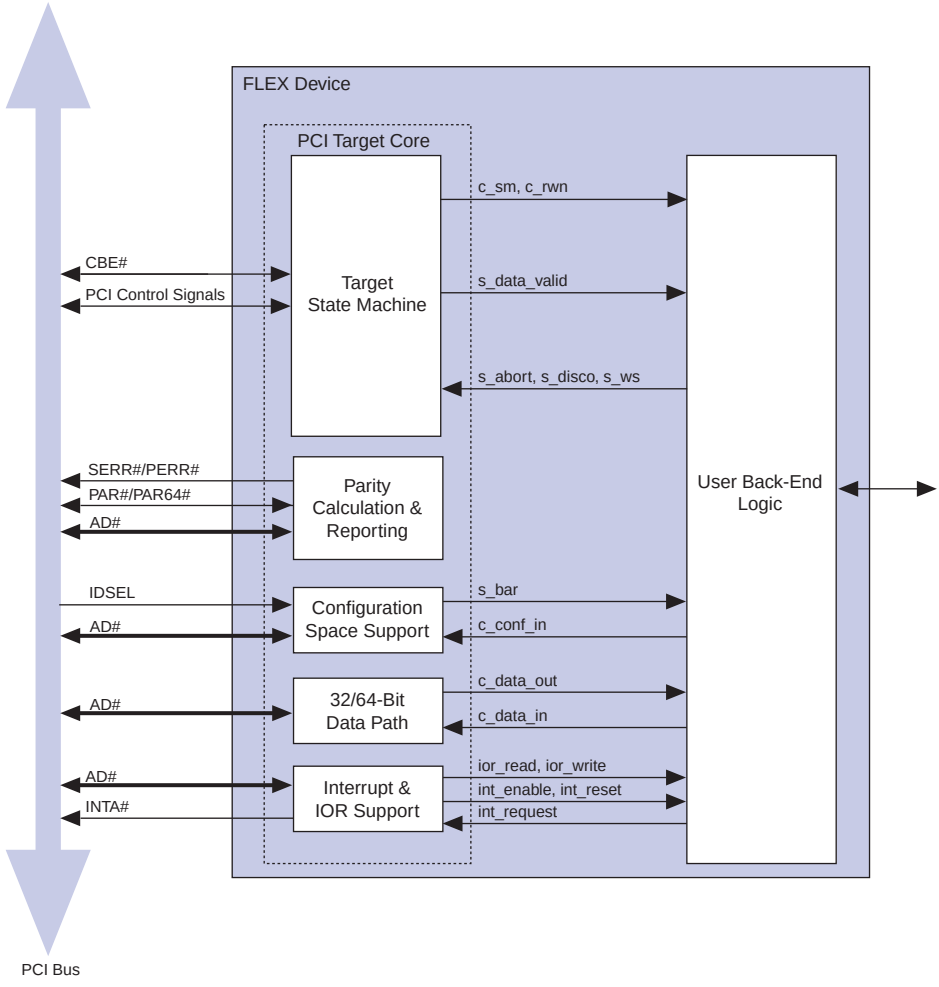
Modifiable Parameters

Parameter	Description
DPS/CPS	Data (CBE) path size
CNF_DID_VID	Vendor ID/Device ID
CNF_SUBSYS_DID_VID	Subsystem Vendor ID/Device ID
CNF_CCODE_REVID	Class code ID/Revision number
CNF_CARDBUS_PTR	CardBus CIS pointer
CNF_CAPABILITY_PTR	CompactPCI capability pointer
CNF_66_CAPABLE	66-MHz capable flag
CNF_INTERRUPT_PIN	Interrupt pin select
CNF_MEMORY_ENABLE	Memory enable bit preset
CNF_IO_ENABLE	I/O enable bit preset
CNF_PARITY_REPORTING	Parity error reporting enable bit preset
BARn_SIZE	BAR0 to BAR5 space size
BARn_PARAM	BAR0 to BAR5 space attributes
ROMBAR_SIZE	ROM base address size
ROMBAR_ADDR	ROM base address preset
CNF_INTERRUPT_LINE	Interrupt line preset
DAC_ENABLE	Dual address cycle (DAC) support

Block Diagram

Figure 8 shows the block diagram for the 32/64-bit PCI bus target interface megafunction.

Figure 8. 32/64-Bit PCI Bus Target Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	550	0	>33 MHz	DPS = 32, CPS = 4 (32-bit megafunction)
EPF10K30A	-2	550	0	>33 MHz	DAC_ENABLE = 1 (DAC support)
EPF10K30E	-3	550	0	>66 MHz	
EPF10K50	-3	550	0	>33 MHz	BAR0_SIZE = 15 (32 Kbytes of memory space)
EPF10K50V	-2	550	0	>33 MHz	
EPF10K100B	-3	550	0	>33 MHz	
EPF10K130E	-3	550	0	>66 MHz	
EPF10K200E	-3	550	0	>66 MHz	
EPF6010A	-3	550	–	>33 MHz	*(1)*
EPF6016	-3	550	–	>33 MHz	*(2)*
EPF6024A	-3	550	–	>33 MHz	*(3)*

Notes:
(1) Slower speed grade usable.
(2) 66-MHz compliance on only FLEX 10KE-1 devices.
(3) Same performances in 64-bit mode.

64-Bit PCI Bus Target Interface

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-C42A

- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- 64-bit PCI bus
- Zero-wait state burst data transfer with internal write buffer
- 33-MHz operating frequency

General Description

The 64-bit PCI target megafunction is designed for interfacing user logic with a 64-bit PCI bus. This megafunction is a very compact design that minimizes logic cell count while offering double the bandwidth performance of a 64-bit bus system.

An internal write buffer is included in this design to support zero-wait state burst transfer and a very long burst length. The megafunction can transfer data up to 266 Mbytes per second. Both 64-bit and 32-bit data transfer rates are supported by this megafunction. All compliant configuration registers are included in the megafunction and all configuration accesses are processed automatically.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with features and customization. Contact Eureka Technology for a logic cell count that is based on user specifications.

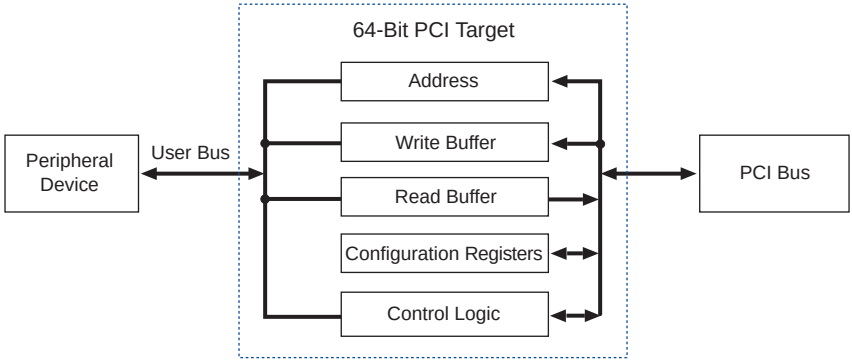
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 9 shows the block diagram for the 64-bit PCI target megafunction.

Figure 9. 64-Bit PCI Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30	-2	500	0	33 MHz	Contact Eureka Technology
EPF6016	-2	500	–	33 MHz	Contact Eureka Technology

64-Bit PCI Master/Target Interface

Vendor: Eureka Technology
Target Application: Video co-processing, real-time imaging, embedded communications
Additional Deliverables: Constraint files, simulation files, top-level design template, training
ID Code: 2107-C061

- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- 64-bit PCI bus
- Zero-wait state burst data transfer
- Includes both bus master and bus target functions

General Description

The 64-bit PCI master/target megafunction interfaces bus mastering devices, such as DMA controllers or video coprocessors, to the PCI bus. It processes all data requests from the bus mastering device and translates them into PCI bus requests.

This megafunction is designed for a 64-bit PCI bus system, which doubles the data bandwidth of a 32-bit PCI system. It supports zero-wait state burst transfers and a very long burst length. The megafunction supports up to a 266 Mbytes per second data transfer rate, and both 64-bit and 32-bit data transfers.

The 64-bit PCI master/target megafunction contains the functions of a bus master and a bus target. The device data and status can be accessed as a PCI master or target. All compliant configuration registers are included in the megafunction and all configuration accesses are processed automatically. This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format.

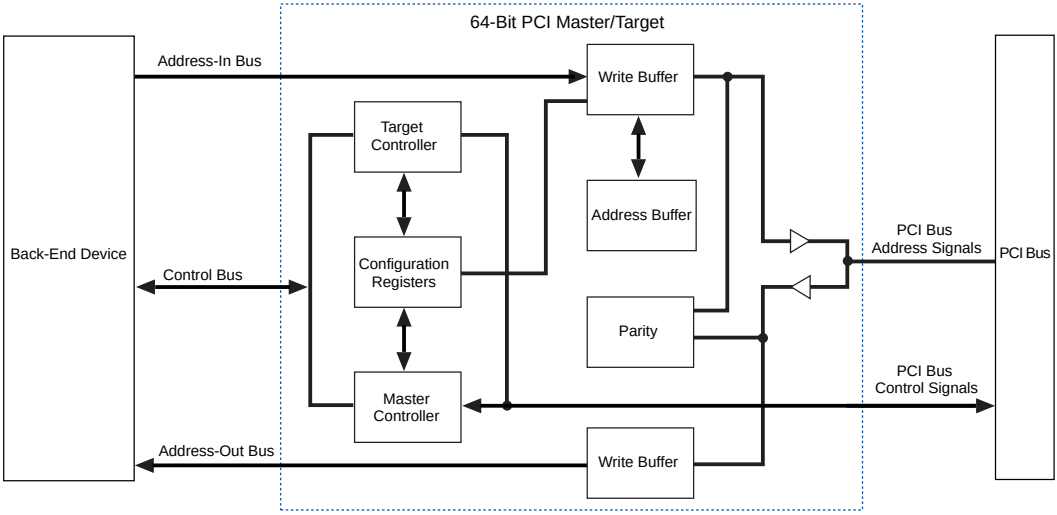
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements.

Block Diagram

Figure 10 shows the block diagram for the 64-bit PCI master/target interface megafunction.

Figure 10. 64-Bit PCI Master/Target Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30A	-2	950	0	33 MHz	Contact Eureka Technology

PCI Host Bridge

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 1207-D410

- Combined host bridge, bus master, and bus target functions in one megafunction
- Fully compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Designed for PLD and ASIC implementations in various system environments
- 32/64-bit bus master and target support
- Supports burst transfer to maximize memory bandwidth
- Zero wait-state PCI data transfer. Up to 133 Mbytes per second at 33 MHz
- Supports target retry, disconnect, and target abort
- Automatic transfer restart on target retry and disconnect
- Concurrent bus master and target function
- Generate standard PCI type 0 and type 1 configuration access
- High-speed bus request and arbitration
- Supports all PCI-specific configuration registers

General Description

The bidirectional PCI host bridge is a bus interface designed for efficient interfacing between the host CPU and the PCI bus. It contains the functions of a bus master and bus target, and has the ability to initiate configuration access all in one megafunction. It performs all the data transfer functions necessary for the bus mastering device to access data through the PCI bus. It supports burst data transfer to maximize data bandwidth. The target function allows other PCI masters to access system resources on the CPU local bus. It supports high-speed bus request and arbitration to minimize transfer latency.

Single and burst data transfers are supported both as bus master and bus target. The interface to the internal controller is through a synchronous X86 PCI host-bridge style local bus interface. All data transfer on the PCI bus can be accessed through the local bus.

This megafunction is available in AHDL, Verilog HDL, VHDL, as well as netlist format. Megafunction sizes vary with features and customization.

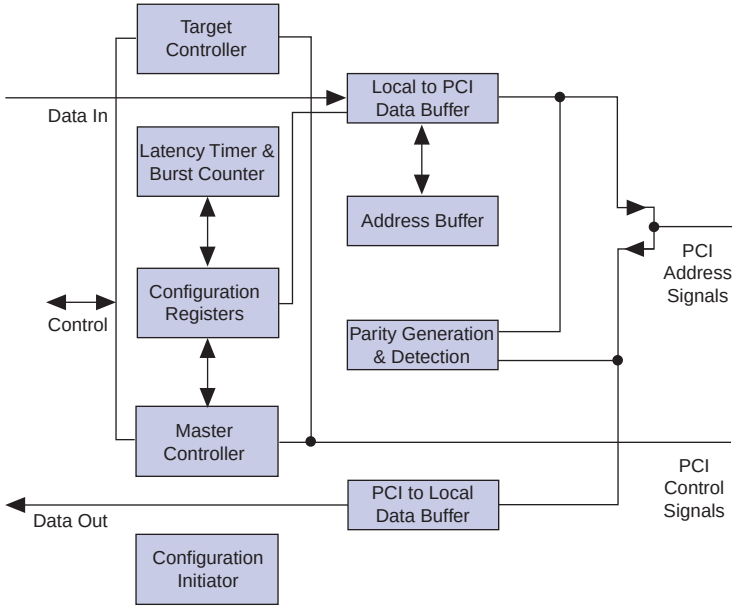
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 11 shows the block diagram for the PCI host bridge megafunction.

Figure 11. PCI Host Bridge Megafunction Block Diagram

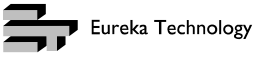


Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	–	1,000	0	33 MHz	Contact Eureka Technology
EPF6016	–	1,000	0	33 MHz	Contact Eureka Technology

PCI Bus Arbiter

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Source code, test bench and test vectors, top-level design template, documentation
ID Code: 2107-A331



- Compliant with PCI SIG ***PCI Local Bus Specification, Revision 2.2***
- Designed for PLDs and ASICs and implementations in various system environments
- Supports up to eight bus masters
- Rotating priority scheme
- Bus parking
- Single cycle request-to-grant turn-around time
- Quiet cycle during master switch
- Master time-out

General Description

The PCI bus arbiter megafunction performs bus arbitration among multiple masters on the PCI bus.

The PCI bus arbiter implements a rotating priority scheme. The requestor that was granted the bus most recently receives the lowest priority, while the requestor position next to it receives the highest priority; the remaining requestors receive subsequently lower priority based on their position.

Bus parking is implemented by the arbiter. When no requestor is active, the arbiter grants the bus to the requestor that was granted most recently.

This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with features and customization.

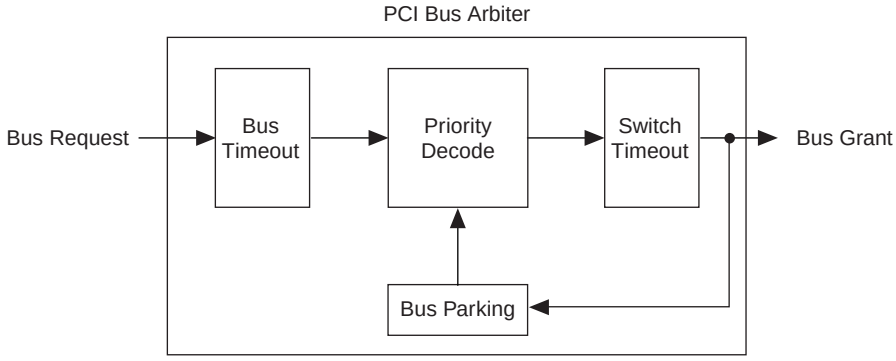
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 12 shows the block diagram for the PCI bus arbiter megafunction.

Figure 12. PCI Bus Arbiter Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10K	–	100	0	33 MHz	Contact Eureka Technology
FLEX 6000	–	100	0	33 MHz	Contact Eureka Technology

CAN Bus

Vendor: SICAN Microelectronics
Target Application: Automotive electronics, home automation, simple sensor/actuator systems
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-47A4

- Compatible with ***CAN Specification, Revision 2.0B*** passive/active
- Completely synchronous flipflop design
- Self-test mode
- Readable error counters
- Data transfer rate up to 1 Mbit per second
- Cycle frequency of 12 MHz

General Description

The Controller Area Network (CAN) bus megafunction fulfills all protocol functions according to ***CAN Specification, Revision 2.0B***, including extended functionality (***CAN Specification, Revision 2.0B*** active). The CAN bus megafunction incorporates all of the features required by ***CAN Specification Revision 2.0***, including error handling capabilities, stuff bit generation, cyclic redundancy code (CRC), and multiple sample points.

The CAN bus megafunction has a universal interface for connection to the receive and transmit buffers, allowing the megafunction to be optimized for specific applications. The megafunction does not contain receive or transmit buffers; these buffers must be implemented externally.

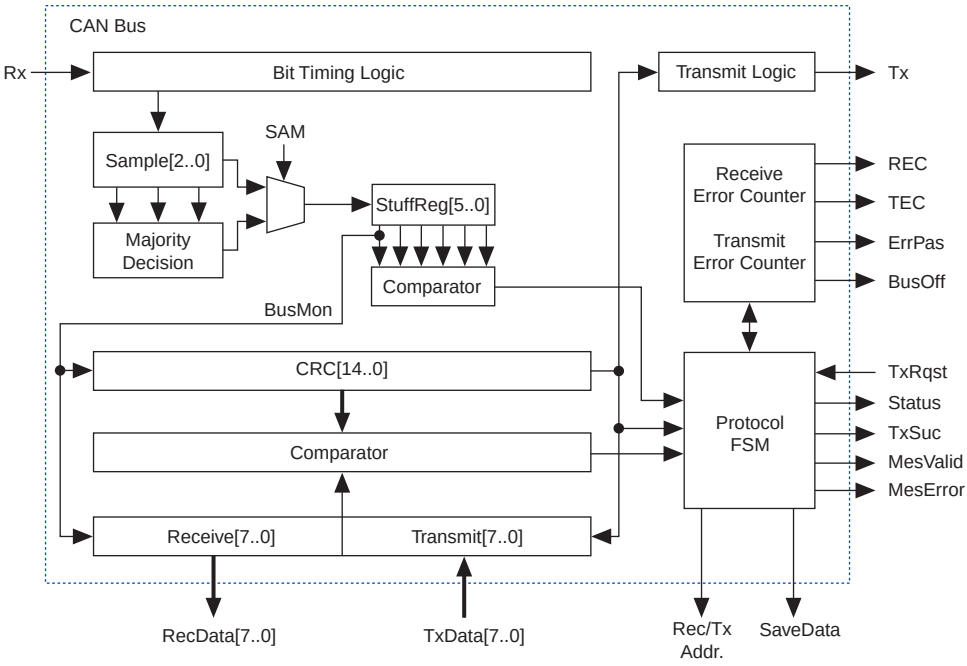
Modifiable Parameters

SICAN can customize the data output size on the back-end device.

Block Diagram

Figure 13 shows the block diagram for the CAN bus megafunction.

Figure 13. CAN Bus Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K20	-3	720	0	12 MHz	8-bit data output

IEEE 1394 Bus FireFox Link Layer Controller

Vendor: SIS Microelectronics
Target Application:
Buses and interfaces, processors and peripherals, telecommunications and data communications
ID Code: 7D0E-1394

- Conforms to IEEE 1394a standard for cable environment
- Supports all required 1394a features
- Interfaces to any IEEE 1394-1995 or IEEE 1394a physical layer device
- Supports 100, 200, and 400 Mbits per second 1394 Bus Speeds
- Cycle master capable
- Generic 32-bit Host Bus Interface
- Chip control and status available through directly addressable registers
- Host clock is asynchronous to Annex J SCLK
- Contains two FIFO buffers: packet receive and packet transmit—each 512 quadlets deep
- Also available as RTL source Verilog HDL

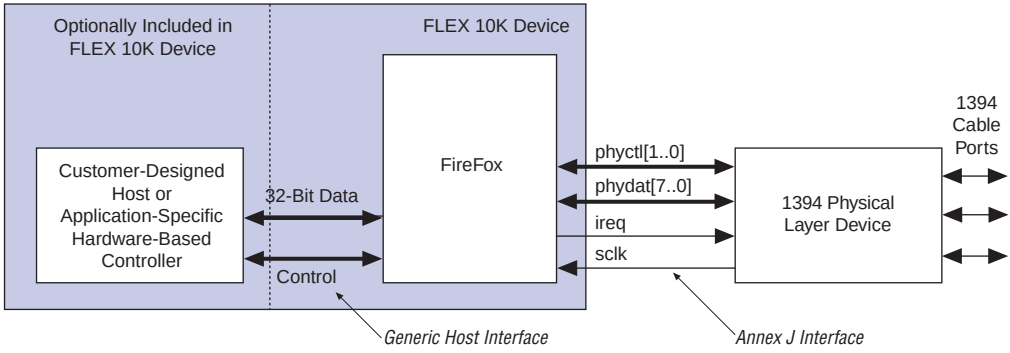
General Description

The FireFox megafunction provides IEEE 1394 asynchronous packet link layer support between a controller implementing the IEEE 1394 transaction layer and an external device implementing the IEEE 1394 physical layer. This design is ideal for embedded applications that require an IEEE 1394 interface.

Block Diagram

Figure 14 shows the block diagram for the FireFox link layer controller megafunction.

Figure 14. FireFox Link Layer Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *(1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K250A	-1	4,049	18	50 MHz	Contact SIS Microelectronics

Note:

(1) The host interface is 32 bits wide with a maximum speed of 50 MHz. The Annex J interface is 8 bits wide and clocked at 49.152 MHz.

IEEE 1394 Link Layer Controller

Vendor: Simple Silicon
Target Application: Home LAN, ATM bridge, real-time multimedia, DSS, set-top boxes
Additional Deliverables: User manual, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE01

- Compliant with ***IEEE 1394 Specification, Draft 8.0 Version 2***
- Supports both asynchronous and isochronous data transfer modes
- Designed for 100 Mbytes per second (Mbps), 200 Mbps, and 400 Mbps bus speeds
- Supports PCI/industry-standard architecture (ISA) interface
- Includes transaction layer, node controller, and bus management facility
- Provides physical layer (PHY) interface compliant with IEEE 1394 specification
- Supports external FIFO and ROM interfaces
- Includes testbench and test suites covering the functionality, protocol, and error conditions

General Description

The IEEE 1394 link layer controller megafunction is the hardware implementation of the link layer and hardware portions of the transaction layer and node controller protocols. The megafunction sends and receives data by forming it into packets, adding headers, and generating and checking the CRCs. When the megafunction wants to send data, it tells the PHY to gain access to the serial bus. When the PHY has accessed the bus, the megafunction sends parallel data to the PHY for serialization transmission through the cable. As data is received by the PHY, it delivers and sends the data to its link. The link determines whether the data is meant for it by reading the address in the header. If it is, the data is accepted and stored appropriately. If not, the data is ignored. A PCI interface is also available with the megafunction.

Modifiable Parameters

The following megafunction parameters can be modified:

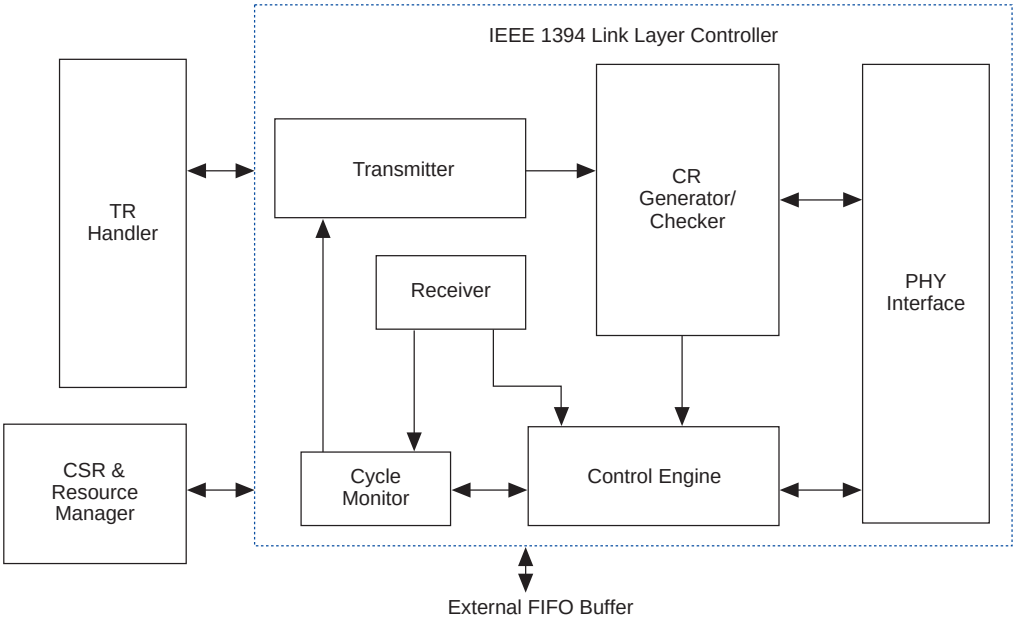
Modifiable Parameters

Parameter	Description
MAX_SPEED	Maximum speed can be 100 Mbps, 200 Mbps, or 400 Mbps.
DATA BUS WIDTH	For link PHY interface. Data bus width can be 2, 4, or 8 bits.

Block Diagram

Figure 15 shows the block diagram for the IEEE 1394 link layer controller megafunction.

Figure 15. IEEE 1394 Link Layer Controller Megafunction Block Diagram



Device Utilization Example *Notes (1), (2)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-3	2,748	0	50 MHz	Contact Simple Silicon

Notes:
(1) External FIFO buffers can be modeled as EABs, if needed.
(2) The megafunction is designed to support both isochronous and asynchronous modes. However, most applications require only one or the other. Choosing only one mode can result in over 30% savings in logic cell utilization.

IEEE 1284 Parallel Slave Interface

Vendor: SIS Microelectronics
Target Application: Asynchronous parallel communications
Additional Deliverables: Simulation file
ID Code: 7D0E-1284

- Bidirectional interface between host computers and peripheral devices
- Uses standard parallel port found on many computer systems
- Fully tested, includes a complete test suite
- Configurable for compatible mode timing of nACK and BUSY ports
- Asserts interrupt or DMA requests when the transmit buffer is empty or the receive buffer contains data

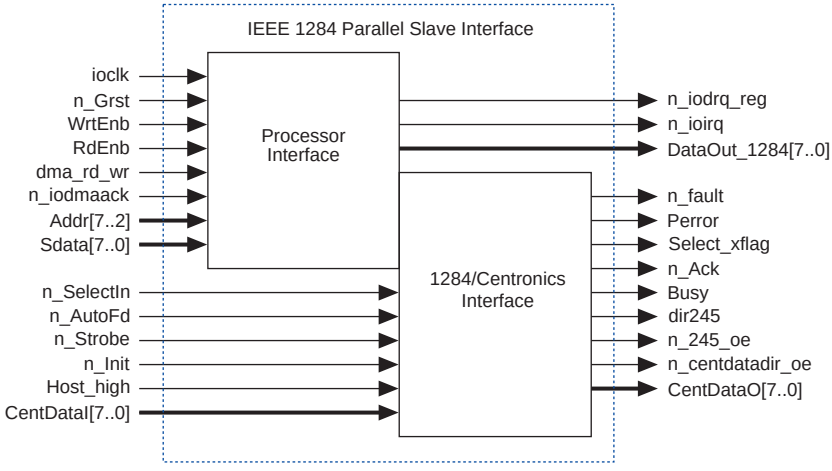
General Description

The IEEE 1284 parallel slave interface megafunction is an interface for fully interlocked, asynchronous bidirectional parallel communications between host computers and peripherals. The megafunction is compatible with the 8-bit IEEE 1284 and Centronics parallel port (printer) interfaces, and it can read data from and write data to the parallel printer port interface. It supports five operational modes: forward compatibility mode, extended capabilities port (ECP) mode with forward-only run-length encoding (RLE), ECP mode (forward and reverse), reverse nibble mode, and request device ID using nibble mode (reverse mode).

Block Diagram

Figure 16 shows the block diagram for the IEEE 1284 parallel slave interface megafunction.

Figure 16. IEEE 1284 Parallel Slave Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	1,350	0	33 MHz	Contact SIS Microelectronics
EPF6016	-2	910	–	27 MHz	Contact SIS Microelectronics

IIC Master Interface

Vendor: SICAN Microelectronics
Target Application: Communication interface for processors, serial data transfer, simple two-wire bus system
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-5A7B

- Supports system clocks up to 50 MHz
- Supports inter integrated circuit (IIC) fast mode up to 400 kHz
- Reads and writes data bursts
- Supports special modes for IIC read and write access to dedicated register address
- Filters spikes on the IIC bus
- Generates wait states
- Fully synchronous design

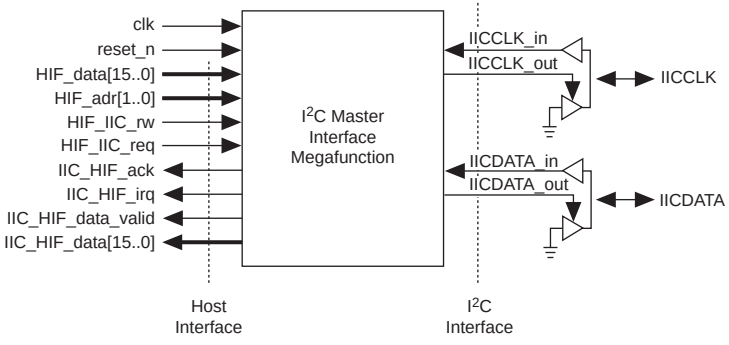
General Description

The IIC master interface megafunction interfaces a host CPU with an IIC bus. This megafunction is essentially a parallel-to-serial/serial-to-parallel converter, converting a host CPU's parallel data into serial format for transfer over the IIC bus, and visa versa. Thus, a host CPU can control other devices on the same IIC bus through this megafunction. The IIC master interface megafunction also takes care of all interface timing, data structure, and error handling.

Block Diagram

Figure 17 shows the block diagram for the IIC master interface megafunction.

Figure 17. IIC Master Interface Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10	-4, -3	309	0	28, 34 MHz	Contact Sican Microelectronics
EPF10K10A	-3, -2, -1	313	0	29, 39, 47 MHz	Contact Sican Microelectronics
EPF10K30E	-1	313	0	53 MHz	Contact Sican Microelectronics
EPF10K50E	-3, -2, -1	313	0	31, 40, 49 MHz	Contact Sican Microelectronics
EPF10K100B	-2, -1	313	0	40, 45 MHz	Contact Sican Microelectronics
EPF10K200E	-1	313	0	41 MHz	Contact Sican Microelectronics

Note:
(1) Contact Sican Microelectronics for EP20K400 device performance data.

IIC Slave Interface

Vendor: SICAN Microelectronics
Target Application: Communication interface for processors, serial data transfer, simple two-wire bus system
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-9A7A

- Supports system clocks up to 50 MHz
- Supports IIC standard (100 kHz) and fast mode (400 kHz)
- Reads and writes data bursts
- Supports special modes for IIC read and write access to dedicated register address
- Filters spikes from the IIC bus
- General wait states
- Synchronous design

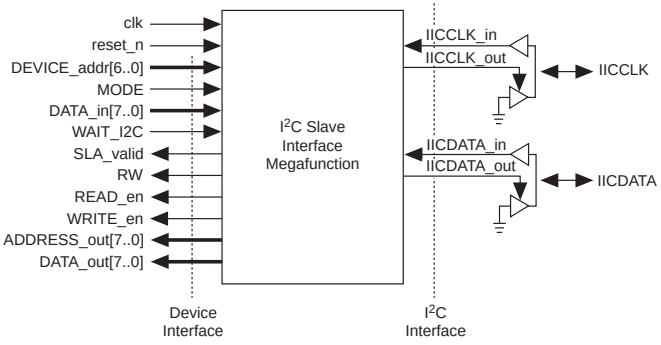
General Description

The IIC slave interface megafunction interfaces a device with an IIC bus. This megafunction is essentially a parallel-to-serial/serial-to-parallel converter, converting a device's parallel data into serial format for transfer over the IIC bus, and visa versa. Thus, a host CPU controls a device through the I2C bus and this megafunction.

Block Diagram

Figure 18 shows the block diagram for the IIC slave interface megafunction.

Figure 18. IIC Slave Interface Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K20	-4, -3, -2, -1	166	0	26, 29, 39, 47 MHz	Contact Sican Microelectronics
EPF10K30E	-1	166	0	66 MHz	Contact Sican Microelectronics
EPF6010A	-1	202	–	28 MHz	Contact Sican Microelectronics
EPF6016	-3, -2	202	–	20, 24 MHz	Contact Sican Microelectronics
EPM9320	-20, -15	131	–	32, 45 MHz	Contact Sican Microelectronics

Note:
(1) Contact Sican Microelectronics for EP20K400 device performance data.

Sony/Philips Digital Audio Interface (Input)

Vendor: SICAN Microelectronics
Target Application: DVD, digital audio
Additional Deliverables: Simulation files, user guide
ID Code: 18CD-9SPD

- Processes two-channel pulse-code modulation (PCM) encoded audio data (IEC 958)
- Processes compressed audio bitstreams (IEC 1937)
- Bit serial output of decoded audio data
- 16-bit output of user data and channel status information
- Validity and parity information of each subframe

General Description

The Sony/Philips digital audio interface megafunction is a standardized interconnect for audio equipment. It is self-clocking and self-synchronizing. The cabling uses either optical fiber or RCA connectors and 75-Ω coaxial cable. This interface is the consumer version of the AES/EBU interface (IEC 958) for professional audio equipment, which uses XLR connectors in combination with 110-Ω impedance. For both standards, the digital signal processing is the same; only the cable connectors are different.

The interface can be used for sampling rates of 32 kHz, 44.1 kHz, and 48 kHz and up to 24-bit word width per sample for the transmission of two-channel PCM encoded audio data. An extension to convey non-PCM encoded bitstreams is subject within IEC 1937. As a result, the Sony/Philips digital audio interface megafunction can handle compressed multi-channel audio data such as MPEG-2 or Dolby AC-3 audio bitstreams. This capability is critical to DVD decoder applications.

Functional Description

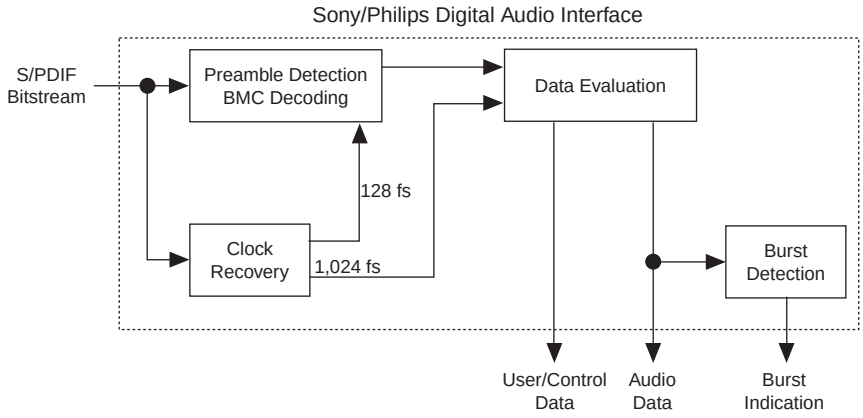
Biphase mark code (BMC) decoding and synchronization is applied to the input S/PDIF bitstream. The subsequent data evaluation module is supplied with the BMC-decoded data and outputs the audio data, control (channel status) data, and user data. A clock recovery function from the input bitstream is then necessary because two clock signals—with factors 128 and 1,024 of the audio sampling frequency—are required for synchronization and data evaluation.

A phase-locked loop (PLL) circuit is essential for clock recovery.

Block Diagram

Figure 19 shows the block diagram for the Sony/Philips digital audio interface megafunction.

Figure 19. Sony/Philips Digital Interface (Input) Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10A	-2	340	0	60 MHz	Contact Sican Microelectronics

Note:
(1) Contact Sican Microelectronics for EP20K400 device performance data.

Sony/Philips Digital Audio Interface (Output)

Vendor: SICAN Microelectronics
Target Application: DVD, digital audio
Additional Deliverables: Simulation files, user guide
ID Code: 18CD-8SPD

- Processing of two-channel PCM encoded data (IEC 958)
- Processes compressed audio bitstreams (IEC 1937)
- Bit serial output of encoded audio data
- Support of user data and channel status information
- Validity information of each subframe

General Description

The S/PDIF interface is a standardized interconnect for audio equipment. It is self-clocking and self-synchronizing. The cabling uses either optical fiber or RCA connectors and 75-Ω coaxial cable. S/PDIF is the consumer version of the AES/EBU interface (IEC 958) for professional audio equipment, which uses XLR connectors in combination with 110-Ω impedance. For both standards, the digital signal processing is the same; only the connectors are different.

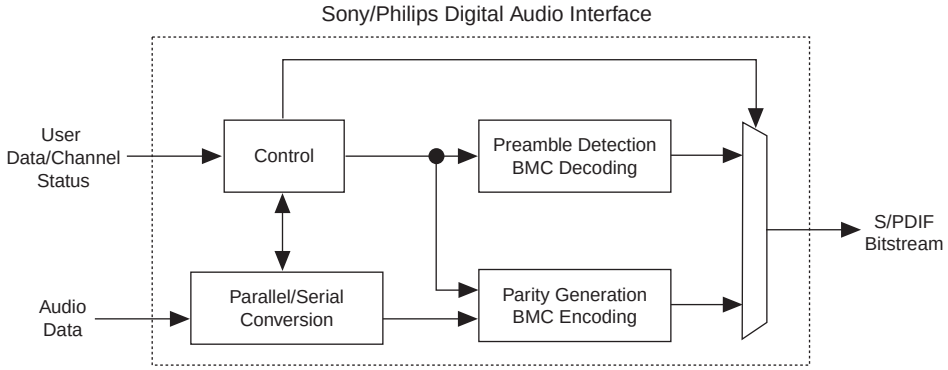
Functional Description

First, a parallel-to-serial conversion is applied to audio data samples, user data, or channel status information. Subsequently, parity generation and BMC encoding is performed. Preambles are inserted into the resulting bitstream by a multiplexer, which provides the S/PDIF as outputs.

Block Diagram

Figure 20 shows the block diagram for the Sony/Philips digital audio interface megafunction.

Figure 20. Sony/Philips Digital Interface (Output) Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10A	-1	276	2	66 MHz	Contact Sican Microelectronics

Note:
(1) Contact Sican Microelectronics for EP20K400 device performance data.

Smart Card Interface (ICC)

Vendor: SICAN Microelectronics
Target Application: Smart card
ID Code: 18CD-8ICC

- Support of ISO/IEC 7816-based communication with integrated circuit cards, including:
  - Answer-to-reset (ATR)
  - Character mode
  - Block mode
  - Baud rate adjustment
- Card clock selection:
  - Internally generated clock of 3.5712 MHz
  - One of three externally generated card clocks
- Possible baud rates, when the internal card clock of 3.5712 MHz is used:
  - 9.600, 19.200, 38.400, 76.800, 15.3600, and 307.200 bits per second
  - Easy adaptation to different system clocks is possible
- Optional use of a programmable card clock divider for the baud rate: Range 1..(2^{16} – 1)
- A single buffer for input and output direction for 16 bytes, adjustable via generics
- Parity check
- Checking of timeouts

General Description

The smart card interface ICC supports the communication between a host processor and an external smart card ICC in compliance with the ISO/IEC-7816 standard.

Functional Description

The smart card interface megafunction implements the complete physical layer and important parts of the data link layer in accordance with the OSI reference model. Some parts of the data link layer must be implemented in software on a host processor. The application layer is not implemented in the ICC and is also part of a host processor.

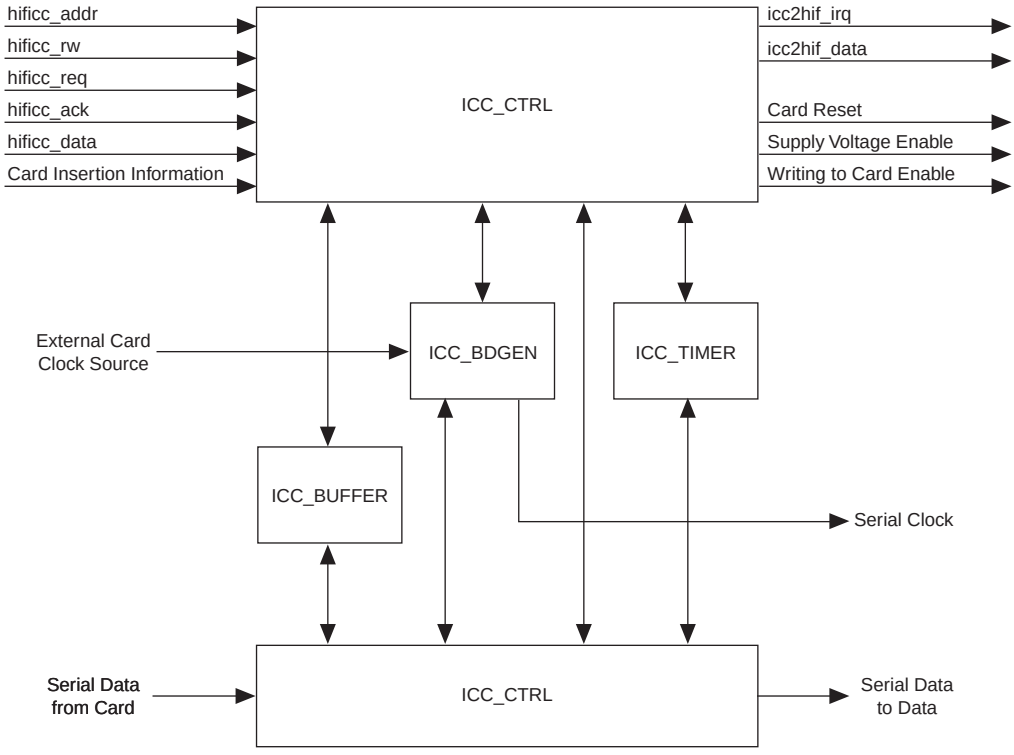
The smart card interface megafunction enables the power supply voltage (VCC) for the smart card. The power supply to the card must be enabled outside of the ICC. Programming a card by using the programming voltage (VPP) also must be performed outside of the ICC.

Data input and output of a smart card is performed through a bidirectional tri-state port. Therefore, the ICC data input port, the ICC data output port, and output enable port must to be connected outside of the ICC through a bidirectional pad cell with the card I/O port.

Block Diagram

Figure 21 shows the block diagram for the smart card interface megafunction.

Figure 21. Smart Card Interface ICC Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30A	-1	933	1	21 MHz	Contact Sican Microelectronics
EPF10K30E	-1	933	1	33 MHz	Contact Sican Microelectronics

Note:
(1) Contact Sican Microelectronics for EP20K400 device performance data.

USB Function Controller

Vendor: Sapien Design
Target Application: High-speed interface PC peripherals, including audio, video, and storage devices
Additional Deliverables: Simulation test environment available
ID Code: BI0E-1100

- Fully compliant with ***USB Specification, Revision 1.0***
- Automatic hardware-managed protocol
- Up to 16 end points of any type
- Simple application interface

General Description

The USB function controller megafunction implements the complete ***USB Specification, Revision 1.0*** and is suitable for audio, human interface, and storage applications. This megafunction automatically manages all USB protocol requirements in hardware. It also offers a fast, low-risk method of implementing a USB connection that can be easily integrated into any application.

The USB function controller megafunction efficiently uses the Altera FLEX 10K, FLEX 8000, and FLEX 6000 architectures and offers a low-risk prototype or production solution. This megafunction is available in EDIF netlist, Verilog HDL, or VHDL format.

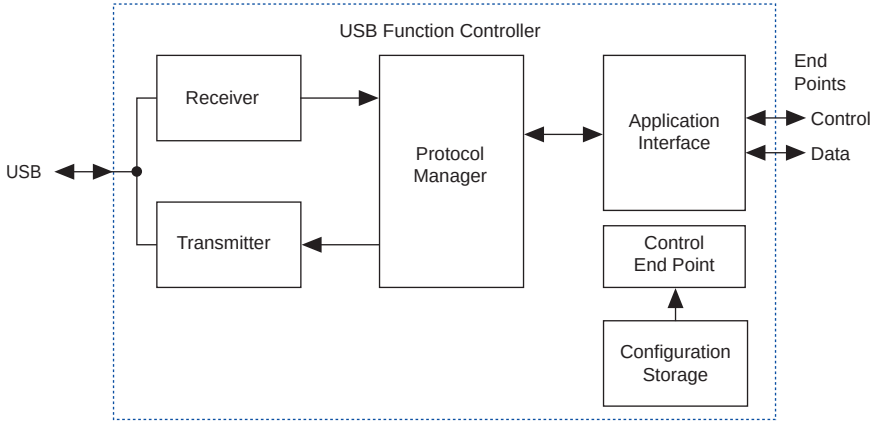
The megafunction is comprised of receiver, transmitter, protocol manager, configuration storage, and application interface logic blocks. The receiver and transmitter blocks support low-level USB protocol operations, such as bit-stuff, NRZI, PID, and CRC. The receiver block decodes the destination of incoming packets and classifies them according to the transfer type. It also checks the CRC and detects bit errors for reporting to the protocol manager. The transmitter block formats packets from the data stream, adding the appropriate CRC header and other protocol requirements.

The protocol manager is responsible for managing higher-level USB protocol functions, such as ACK, NACK, and STALL handshakes. The protocol manager responds to control transfers by accessing the configuration storage for configuration transfers. The configuration storage contains the device, configuration, interface, and end point descriptor information, which is used to dynamically define and configure the megafunction. The application interface communicates with the USB through the protocol manager and, in turn, is used by the application logic to transfer data, control, and status.

Block Diagram

Figure 22 shows the block diagram for the USB function controller megafunction.

Figure 22. USB Function Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance (1)	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-4	1,120	3	12 MHz	Three end points
EPF81500A	-4	1,172	–	12 MHz	Contact Sapien Design

Note:
(1) The standard USB operating frequency is 12 MHz. However, these devices are capable of operating at higher speeds.

USB Function Controller

Vendor: Simple Silicon
Target Application: Computer telephony, plain old telephone service (POTS), integrated services digital network (ISDN), private branch exchange (PBX), printers, scanners, keyboards, HID, audio, compressed video
Additional Deliverables: User manual, documentation, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE02

- Fully compliant with ***USB Specification, Revision 1.0***
- Supports up to 16 end points (user-selectable number, depending on the application)
- Supports back-end execution of vendor-specific and class-specific USB requests
- Extensive set of back-end interface signals are provided to access FIFO buffers and to indicate events like suspend, start of frame (SOF), change in configuration, and remote wakeup
- Supports four transfer types: isochronous, control, bulk, and interrupt
- Includes extensive test suites covering the functionality, protocol check, and error conditions
- User can write tests using high-level constructs like SETUP and IN
- Compatible with the available USB transceiver devices
- Supports both 12-Mbps and 1.5-Mbps transfer rates

General Description

The USB function controller megafunction consists of four main modules: serial interface engine (SIE), control engine, end point FIFO buffer, and digital PLL. The SIE consists of a transmitter, receiver, suspend detector, and reset detector. The function can be used to design and prototype any USB peripheral device. A working keyboard function demonstration and prototype board is available for evaluation.

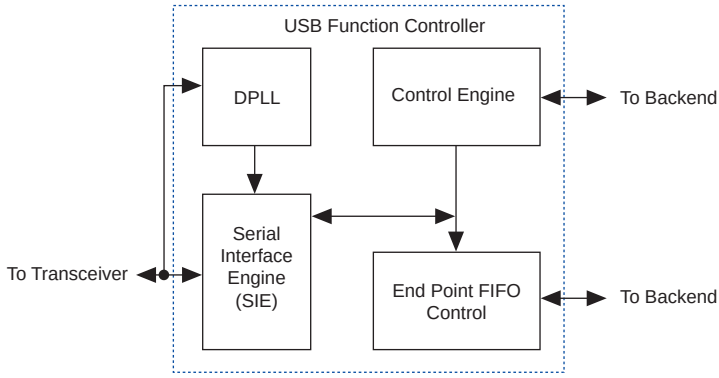
Modifiable Parameters

Simple Silicon can customize the number of end points and the end point FIFO depth to meet user specifications. The default number of end points is 4.

Block Diagram

Figure 23 shows a block diagram of the USB function controller megafunction.

Figure 23. USB Function Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K70	-3	3,240	0	48 MHz	Full-speed operation with 4 end point FIFO buffers.
EPF10K30	-4	1,592	0	6 MHz	Low-speed operation with 2 end point FIFO buffers.

USB Host Controller

Vendor: Sapien Design
Target Application: USB host control for embedded systems
Additional Deliverables: Board, simulation files
ID Code: BI0E-2100

- Compatible with ***USB Specification, Revision 1.0***
- Automatic, hardware-managed protocol
- Supports suspend, resume, and reset signaling

General Description

The USB host controller megafunction implements the complete ***USB Specification, Revision 1.0*** for host controllers and is suitable for embedded system applications that drive USB devices. The megafunction automatically manages all USB protocol requirements in hardware. It offers a fast, low-risk method of implementing a USB connection that can be integrated into any application. The megafunction is available in netlist, Verilog HDL, or VHDL register transfer language (RTL) format.

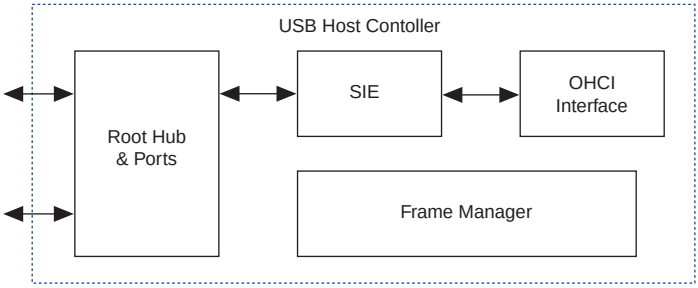
The Serial Interface Engine (SIE) performs receiver and transmitter functions, including packet formation and serialization. The SIE also supports low-level USB protocol operations, such as bit-stuff, NRZI, PID, and CRC. The SIE decodes incoming packets, checks the CRC, and detects bit errors, which are all reported to the frame manager. The SIE formats outgoing packets, adding the appropriate header CRC and other protocol requirements.

The Frame Manager generates SOF packets, schedules periodic and non-periodic packets into frames, and manages data and handshake packets. The system processor queues packets, which contain headers with direction, size, and destination information, into memory. Packet locations are written to channel registers, and subsequent packets are chained together. Packets that time out or return a NACK signal are automatically retried. Packet sizes are used as a criteria for inclusion into a frame. For more information, contact Sapien Design.

Block Diagram

Figure 24 shows the block diagram for the USB host controller megafunction.

Figure 24. USB Host Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-4	1,250	3 to 6	12 MHz	Contact Sapien Design
EPF81500A	-4	1,250	–	12 MHz	Contact Sapien Design

USB Hub Controller

Vendor: Simple Silicon
Target Application:
Home LAN, ATM bridge, real-time multimedia, DSS, set-top boxes
Additional Deliverables:
User manual, documentation, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE03

- Fully compliant with ***USB Specification, Revision 1.1 RC2***
- Works with commercially available USB transceivers
- Supports both bus-powered and self-powered mode
- Supports test mode, which improves simulation speed
- Supplied with user-friendly test environment
- Test vectors cover the USB compliance checklist
- Supports full and low speeds
- Supports standard USB requests and hub-specific requests, as required by the ***USB Specification, Revision 1.1 RC2***

General Description

The USB hub controller megafunction manages multiple USB connections. Hubs can also act as peripherals, for example, when a printer simultaneously serves as a USB peripheral and USB hub, which allows other USB peripherals to connect to the peripheral. The megafunction consists of a repeater, a hub, and port controllers. The megafunction contains a 4× digital PLL, which recovers synchronized clocks and data from the received USB data. The USB hub controller megafunction is supported with a behavioral host model, USB bus analyzer models, and extensive test suites.

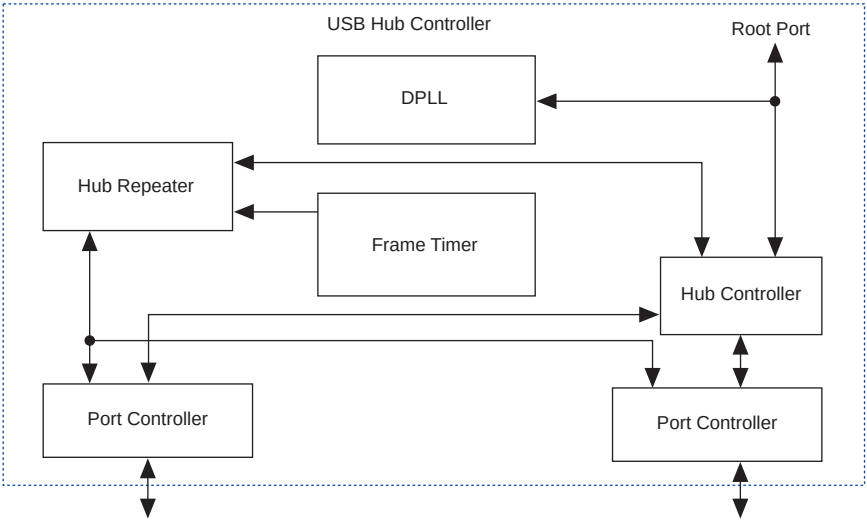
Modifiable Parameters

Simple Silicon can customize the number of downstream ports (the default is two) and whether the power switch is on or off.

Block Diagram

Figure 25 shows the block diagram for the USB hub controller megafunction.

Figure 25. USB Hub Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-3	2,278	0	48 MHz	12 MHz operation with 4× clock

USB Device & Host Controller (VUSB)

Vendor: VAutomation
Target Application:
USB peripherals, USB hosts that do not require full OHCI functionality
Additional Deliverables:
VUSB reference manual
ID Code: 3A0F-BA12

- Integrated USB microcontrollers for USB device and/or host applications
- Verified in silicon, 100% USB '1' compliant
- Uses embedded 8-bit reduced instruction set computers (RISC) CPU for USB command processing
- Supports low/full-speed devices and any number of end points and configurations
- Easily modified to support class or vendor-specific commands

General Description

VAutomation's USB megafunction is a complete solution for USB peripheral and/or host applications. The megafunction has been verified in silicon and is fully compliant with the USB 1.1 specification.

As a device controller, USB is a one-function USB solution. Unlike traditional USB megafunctions, USB contains an embedded 8-bit RISC processor (V8-uRISC). This processor performs all USB command processing and manages USB FIFOs that are built in RAM. This architecture allows you to easily accommodate changes in specification (e.g., buffer size), application, or any operating system.

As an embedded host controller, VUSB meets the needs of non-PC product developers that require USB host capability but do not benefit from the complexity of existing PC-centric USB host controllers. VUSB-HOST is ideal for products that have simple, well-defined requirements for applications where size and cost are critical. A robust application programming interface (API) simplifies the development of host controller application software.

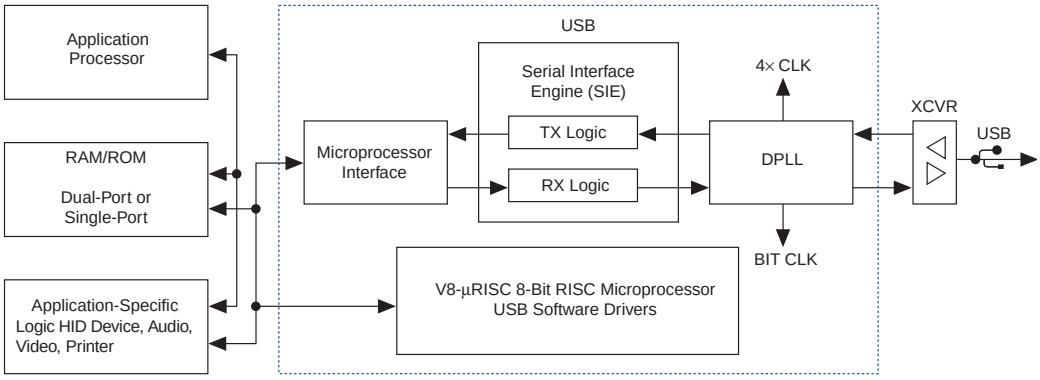
Unique to the USB is the ability of a single megafunction to function as either a device or a host controller. This capability is ideal for products like digital cameras where a connection to a PC and a peripheral (e.g., a printer) is required.

The embedded RISC microprocessor delivers 6 MIPS in a FLEX 10K device, much of which is available for non-USB tasks. This excess bandwidth, along with a wide range of CPU peripherals and a robust set of development tools, allows the VUSB megafunction to be a single-function solution for many USB applications.

Block Diagram

Figure 26 shows the block diagram for the VUSB host controller megafunction.

Figure 26. VUSB Embedded Host Controller Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-1	2,479	0	12 Mbits	Contact VAutomation

Speedbridge

Vendor: SIS Microelectronics
Target Application: Network communication, interface
Additional Deliverables: Documentation, Verilog HDL RTL sources
ID Code: 7D0E-5BA1

- Elastic FIFO buffer for bridging data between various speed domains
- User-parameterizable width and depth
- Provides full/empty status flags
- Independently clocked input and output interfaces
- Register based
- Full/empty status flags

General Description

The speedbridge megafunction is a speed-matching FIFO buffer that transfers data across an asynchronous interface. The read and write ports have independent clocks and synchronous enables for accessing their respective functions. These features allow the clocks to run without read or write operations occurring.

The speedbridge megafunction eliminates the need for an external asynchronous FIFO buffer, which minimizes system development and debugging time and reduces development cost and risk in design.

Modifiable Parameters

The following megafunction parameters can be modified:

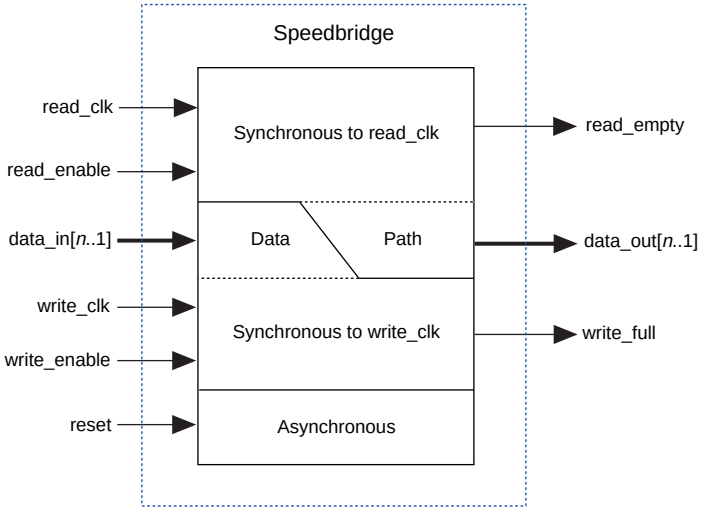
Modifiable Parameters

Parameter	Description
DEPTH	Number of words
WIDTH	Width of data bus

Block Diagram

Figure 27 shows the block diagram for the speedbridge megafunction.

Figure 27. Speedbridge Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	424	0	R: 108 MHz W: 126 MHz	Contact SIS Microelectronics

Note:
(1) R = Read clock frequency; W = Write clock frequency.

PCI & Bus Interface Design Services (ACAP Partners)

The following table lists ACAP partners who offer design services for PCI and bus interfaces.

Partner	Expertise						Services					
	PCI	1394	1284	USB	IIC	ISA	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
Advanced Logical Design, Inc. 12280 Saratoga-Sunnyvale Rd. #201 Saratoga, CA 95070 Tel. (408) 446-1004	✓		✓		✓	✓				✓	✓	✓
Applied Computing Technology, Inc. 1020F Commerce Park Drive Oak Ridge, TN 37830 Tel. (423) 220-0777	✓			✓	✓	✓	✓		✓	✓	✓	
Applied Microelectronics Inc. 1046 Barrington Street, Halifax Nova Scotia, Canada, B3H 2R1 Tel. (902) 421-1250	✓				✓		✓	✓	✓	✓	✓	✓
BARCO SILEX Rue du Bosquet 7 1348 Louvain La Neuve Belgium Tel. (32) 10-45 49 04	✓	✓					✓					
DesignPRO Inc. 35 Stafford Road, Unit 1 Nepean, Ontario, Canada, K2H 8V8 Tel. (613) 596-5030	✓			✓			✓	✓	✓	✓	✓	
Coded Solutions Pty Ltd 65 Johnston Street Annandale, NSW 2038 Australia Tel. (61) 2 9518 7011	✓		✓	✓	✓	✓			✓	✓	✓	

Partner	Expertise						Services					
	PCI	1394	1284	USB	IIC	ISA	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
Digital Design Solutions 6696 Fossil Creek Dr. Memphis, TN 38120 Tel. (901) 759-1802 **Offering:** Custom backplanes, MVIP telephony bus.						✓				✓	✓	✓
DMC Manufacturing, Inc. 7025 Central Highway Pennsauken, NJ 08109 Tel. (609) 665-5400 **Offering:** Experience with design optimization and integration of the Altera design with the printed circuit board for increasing performance, improving manufacturing, and easing testing.										✓	✓	✓
Eberwein & Associates, Inc. 9449 Briar Forest, #507 Houston, TX 77063 Tel. (713) 784-1226 **Offering:** VME, HIPPI, and fiber channel.	✓	✓		✓		✓				✓	✓	✓
Innovative Configuration, Inc. (ICI) 712 via Palo Alto Aptos, CA 95003 Tel. (831) 688-6917	✓				✓		✓		✓	✓	✓	
Intrinsix 33 Lyman St. Westboro, MA 01581 Tel. (508) 836-4100	✓	✓		✓		✓	✓	✓	✓			
I/O Consulting A/S Gaaseagervej 6 DK-8250 Egaa Tel. (45) 87 43 80 74	✓						✓	✓	✓	✓	✓	

Partner	Expertise						Services					
	PCI	1394	1284	USB	IIC	ISA	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
Lewis Innovative Technologies, Inc. 11405 Alabama Highway 33 (P.O. Box 624) Moulton, AL 35650 Tel. (256) 974-8931 **Offering:** VME bus.										✓		
Locke's Digital Developments Ltd. New Street, Marnhull, Dorset, England. DT10 1PY Tel. (44) 0 1258 821 222	✓		✓			✓	✓	✓	✓	✓	✓	
Mettrix Technology Corporation 25 Corporate Park Drive, Suite C Hopewell Junction, NY 12533 Tel. (914) 897-4960	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
Northwest Logic Design, Inc. 1905 NW 169th Place, Suite 121 Beaverton, OR 97006 Tel. (503) 533-5800	✓			✓	✓	✓	✓		✓	✓	✓	
RPA Electronics Design, LLC 1285 Chenango Street Binghamton, NY 13901 Tel. (607) 771-0393	✓			✓	✓				✓	✓	✓	
RTI 10560 Main St., Ste. 417 Fairfax, VA 22030 Web. **http://www.rti-world.com** Tel. (703) 293-9662 **Offering:** Specialize in embedded and distributed real-time hardware and software development on numerous mainstream platforms and languages.		✓				✓		✓	✓		✓	

Partner	Expertise						Services					
	PCI	1394	1284	USB	IIC	ISA	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
SyncAccess, Inc. 5279 Folsom Blvd. Sacramento, CA 95819 Web. **http://www.syncaccess.com** Tel. (916) 457-4838 Fax. (916) 456-8505 **Offering:** Expertise in SCSI, fault tolerant buses, and RAID 0, 1, and 5.	✓				✓	✓	✓	✓	✓	✓	✓	✓
Szabo Electronic Systems 40 Purvis Street Watertown, MA 02472 Tel. (617) 924-0618			✓		✓	✓			✓	✓	✓	✓
Vulcan ASIC Ltd., Unit 6, The Maltings, Royston, Herts, SG8 5DY, England Tel. (44) 0 1763 248163 **Offering:** Can supply a wide range of bus interface IP.	✓	✓		✓	✓	✓	✓	✓	✓			

Processor & Peripheral

September 1999

Overview

Processor and peripheral megafunctions can improve the flexibility of microcontrollers by providing a larger address space memory for an unlimited combination of peripherals, e.g., I/O ports, timers, and universal asynchronous receiver/transmitters (UARTs).

The user can specify a wide range of parameters for each processor and create virtually an unlimited number of instructions, based on the instruction templates. Processor compilation and assembly are almost instantaneous so that the processor architecture, instruction set, and design can all be varied continuously for the best trade-offs in processor and design size/complexity.

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The processor and peripheral section contains the following functions:

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49410 Microprogram Controller

Vendor: CAST
Target Application:
High-speed bit slice designs
Additional Deliverables:
VHDL simulation files, user guide
ID Code: 2AA5-C002

- 16-bit data width that addresses up to 65,536 words
- Internal loop counter can be preset to a 16-bit down-counter for repeating instructions and counting loop interactions
- Four address sources—Microprogram address may be selected from microprogram counter branch address bus, 33-level push/pop stack, or internal holding register
- 16 powerful micro-instructions
- Output enable controls for three branch address sources
- Positive-edge-triggered registers
- Developed in VHDL and synthesized to approximately 9,500 gates, depending on the process used
- Functionally based on the Integrated Device Technology IDT49C410 device

General Description

The `49410` microprogram controller megafunction is an address sequencer that controls the execution sequence for micro-instructions stored in microprogram memory. The megafunction can sequentially access the micro-instructions and can provide conditional branching to any micro-instructions within the 65,536-microword range. In addition, a 33-deep last-in first-out (LIFO) stack provides a microsubroutine return linkage and looping capability.

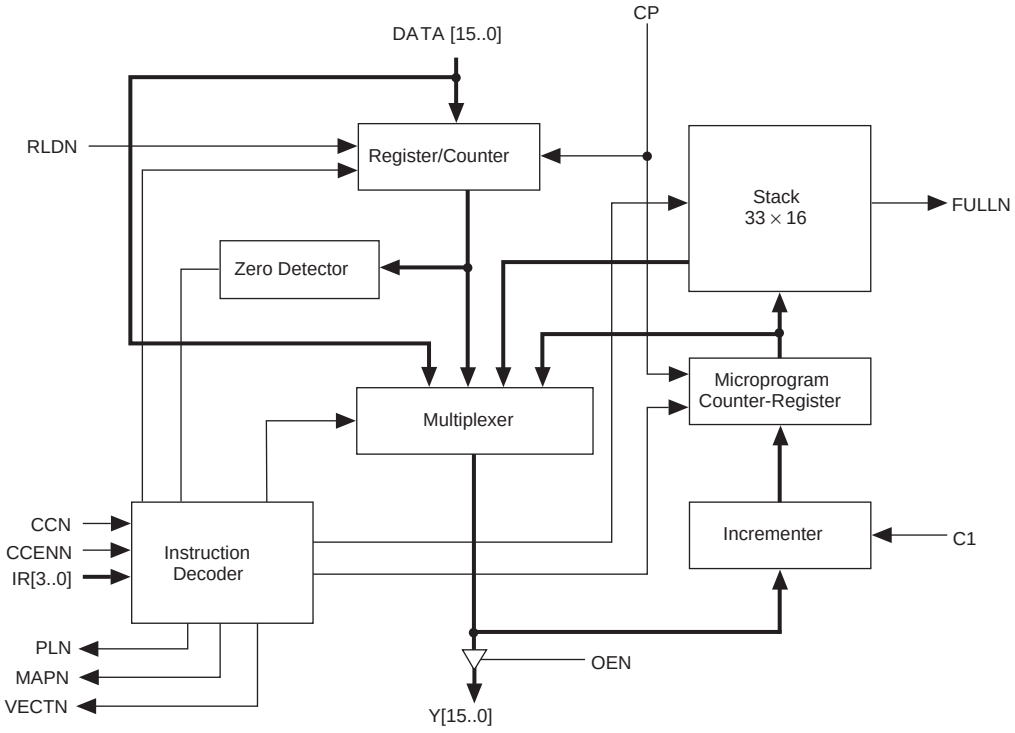
Modifiable Parameters

CAST can modify the megafunction's data width and stack depth to meet user specifications.

Block Diagram

Figure 1 shows the block diagram for the `49410` microprogram controller megafunction.

Figure 1. 49410 Microprogram Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	1,291	–	19 MHz	Contact CAST
EPF10K30A	-1	1,273	–	38 MHz	Contact CAST
EPF10K30E	-1	293	1	56 MHz	Contact CAST
EPF8150	-2	1,121	–	20 MHz	Contact CAST
EPF6016	-1	1,097	–	19.6 MHz	Contact CAST

8051 Microcontroller

Vendor: CAST
Target Application:
8-bit microcontroller
Additional Deliverables:
VHDL source code, synthesis scripts, testbench, assembler programs, modeling notes, compilation notes, simulation notes, synthesis notes
ID Code: 2AA5-C017

- 8-bit control unit
- 8-bit arithmetic logic unit (ALU) with 8 × 8-bit multiplication and division
- Instruction decoder
- Four 8-bit input/output ports
- Two 16-bit timers/counters
- Serial peripheral interface in full duplex mode
- Two-level priority interrupt system
- Five interrupt sources
- Internal clock prescaler and phase generator
- 256 bytes of read/write data memory
- 64 Kbytes of external program memory space
- 64 Kbytes of external data memory space

General Description

The `8051` microcontroller unit megafunction is a fast, single-chip, 8-bit microcontroller and is a derivative of the 80C51 microcontroller family. The megafunction is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C51. The `8051` megafunction accesses instructions from two kinds of program memory, serves software and hardware interrupts, and provides serial communications interface and timer systems.

The `8051` microcontroller unit megafunction is a high-performance, synthesizable 80C51 function specifically designed for reusability. It can operate at frequencies up to 14 MHz in FLEX® devices.

A superset of the `8051` megafunction is also available. The Super8051 consists of the following modules:

- *Functional core*—`8051` megafunction
- *Program memory*—Internal_Program_Memory
- *Data memory*—Internal_Data_Memory
- *Open-drain I/O pins*—OPNDRN

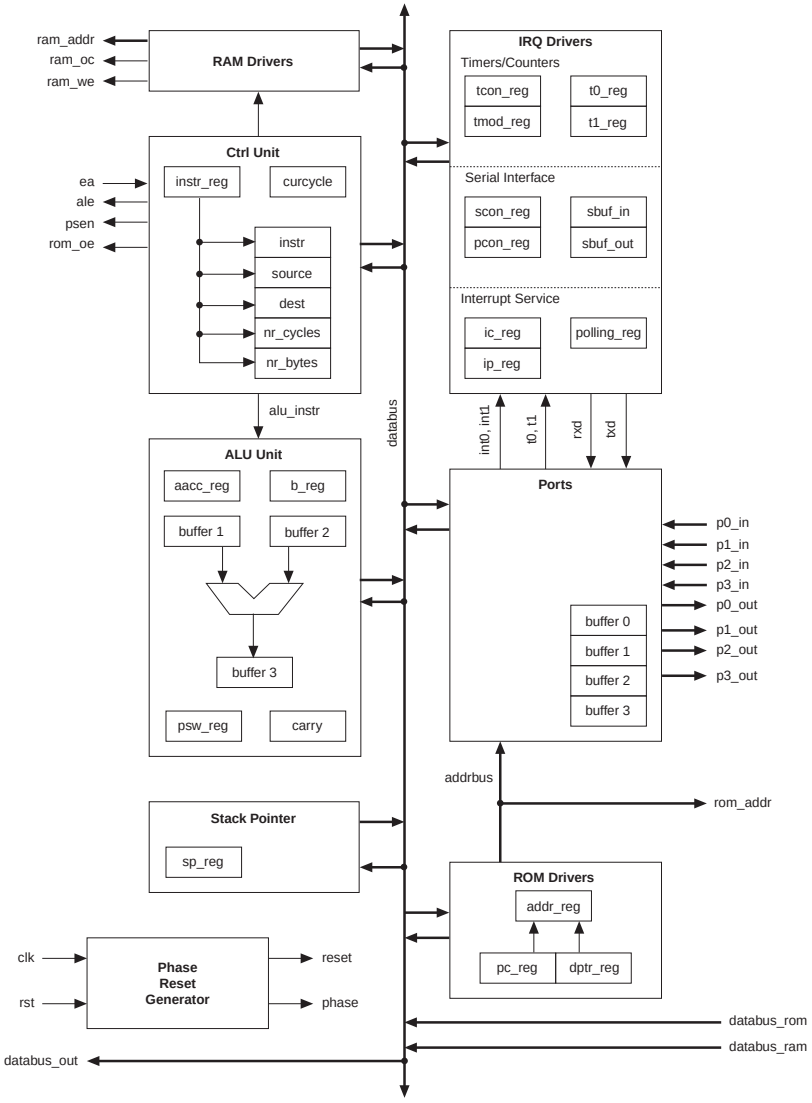
Modifiable Parameters

The `8051` megafunction can be customized to include different memory interface, additional timer/counter, and different RAM/ROM configurations. Contact CAST for any required modifications.

Block Diagram

Figure 2 shows the block diagram for the 8051 microcontroller megafunction.

Figure 2. 8051 Microcontroller Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-3	2,656	–	10 MHz	Contact CAST
EPF10K50V	-1	2,698	–	14 MHz	Contact CAST

RAW8051/8052

Vendor: Richard Watts Associates
Target Application: Low-power microcontroller
Additional Deliverables: Full user manual, VHDL design walkthrough
ID Code: DE73-8052

- Fast 8051/8052 CPU megafunction with 100% software code compatibility
- Three times faster than a standard 8052 at the same clock frequency
- Reduced instruction cycle time
- Optimized for Altera® programmable logic devices (PLDs), ASIC versions available for easy integration
- Available as CPU only, 8051, and 8052 variations
- Evaluation board available for prototyping

General Description

The RAW8051/8052 megafunction implements an enhanced industry-standard 805*X* microcontroller. On average, the megafunction executes software three times faster than a standard 805*X*, while maintaining 100% software code compatibility. In addition to the standard 805*X* peripherals, the megafunction implements an additional data pointer for faster memory copies and indexing. An extended memory version is also available for taking the addressing range up to 4 Mbytes.

The RAW8051/8052 megafunction is supported by a variety of standard EDA development tools.

Modifiable Parameters

The following megafunction parameters can be modified:

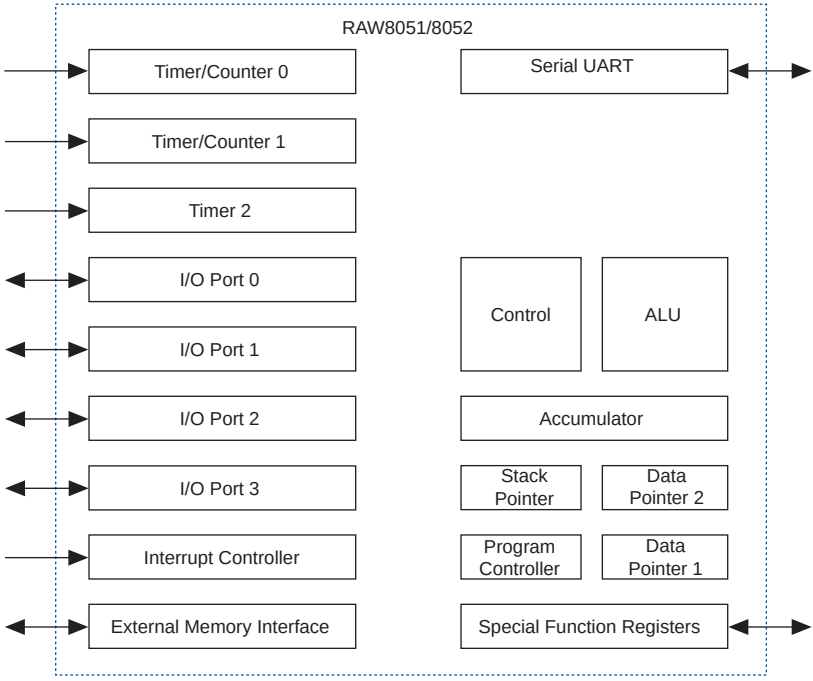
Modifiable Parameters

Parameter	Description
C	Number of counters
I	Number of I/O ports
SM	External memory size
T	Type of CPU function: 8051 or 8052
U	Number of UARTs

Block Diagram

Figure 3 shows the block diagram for the RAW8051/8052 megafunction.

Figure 3. RAW8051/8052 Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,177	1	21 MHz	C = 2, I = 6, SM = 644, T = 8052, U = 1
EPF10K40	-1	1,825	1	11 MHz	C = 2, I = 6, SM = 644, T = 8051, U = 1

BareCore 8052-X

Vendor: Richard Watts Associates
Target Application: 8-bit µcu
Additional Deliverables: Full user manual, VHDL design walkthrough
ID Code: DE73-8052

- Fast 8052/32 CPU with 100% software code compatibility
- Three times faster than a standard product 8052
- Reduced execution cycle time
- Evaluation board available for prototyping

General Description

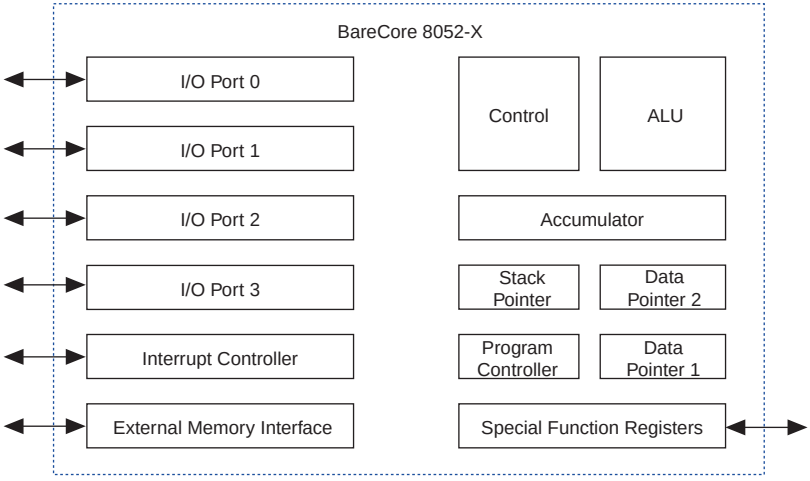
The BareCore `8052-X` megafunction implements an enhanced industry-standard, 8052 8-bit microcontroller. On average, the megafunction executes software three times faster than a standard 8052 device while maintaining 100% software code compatibility. A Philips-compatible extra data pointer is provided for faster memory copies and indexing.

The BareCore `8052-X` megafunction is supported by a wide variety of standard EDA development tools. The megafunction allows designers to use existing software code and achieve performance that is comparable to reduced instruction set computer (RISC) megafunctions.

Block Diagram

Figure 4 shows the block diagram for the BareCore `8052-X` megafunction.

Figure 4. BareCore 8052-X Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	1,400	1	11 MHz	Contact Richard Watts Associates

Note:
(1) This example is optimized for minimum area. Speed improvements are possible.

2901 Four-Bit Microprocessor Slice

Vendor: CAST
Target Application: Serial data communications applications, modem interface
Additional Deliverables: VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C001

- Independent and simultaneous access to two registers save machine cycles
- Eight-function ALU
- Expandable—Any number of devices can be connected for wider bus structures
- Four status flags for carry, overflow, zero, and negative
- Microprogrammable
- Developed in VHDL and synthesizes to approximately 1,300 gates
- Functionality based on the Advanced Micro Devices AM2901

General Description

The 2901 four-bit microprocessor slice megafunction is a cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The megafunction includes a dual-port RAM, ALU, shifter, register, and multiplexer. The microinstructions of the 2901 megafunction allow for easy modeling of various microcontrollers.

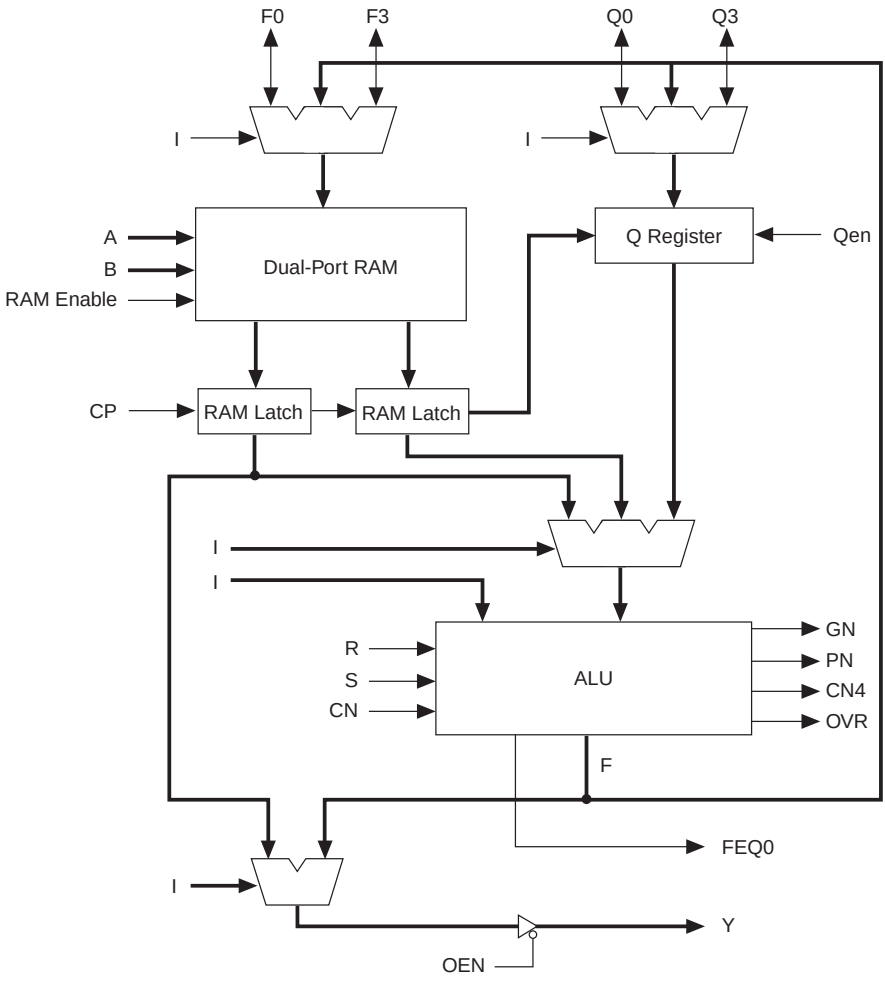
Modifiable Parameters

The 2901 four-bit microprocessor megafunction can be customized to include a larger data width. Contact CAST directly for any required modifications.

Block Diagram

Figure 5 shows the block diagram for the 2901 four-bit microprocessor slice megafunction.

Figure 5. 2901 Four-Bit Microprocessor Slice Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	297	–	39 MHz	Contact CAST
EPF10K30A	-1	297	–	54 MHz	Contact CAST
EPF8452	-3	301	–	27 MHz	Contact CAST
EPF6016	-2	303	–	27 MHz	Contact CAST

2910A Microprogram Controller

Vendor: CAST
Target Application: Serial data communications applications, modem interface
Additional Deliverables: VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C001

- 12-bit data width that addresses up to 4,096 words
- Internal loop counter—Pre-settable 12-bit down-counter for repeating instructions and counting loop interactions
- Four address sources—Microprogram address may be selected from microprogram counter, branch address bus, 9-level push/pop stack, or internal holding register
- 16 powerful micro-instructions
- Output enable controls for three branch address sources
- Positive-edge-triggered registers
- Functionality based on the AMD AM2910A device

General Description

The 2910A microprogram controller megafunction is an address sequencer that controls the execution sequence for the micro-instructions stored in microprogram memory. The megafunction can sequentially access the micro-instructions, and it provides conditional branching to any micro-instructions within the 4,096-microword range. In addition, a nine-deep LIFO stack provides a microsubroutine return linkage and looping capability.

Modifiable Parameters

CAST can modify the following megafunction parameters:

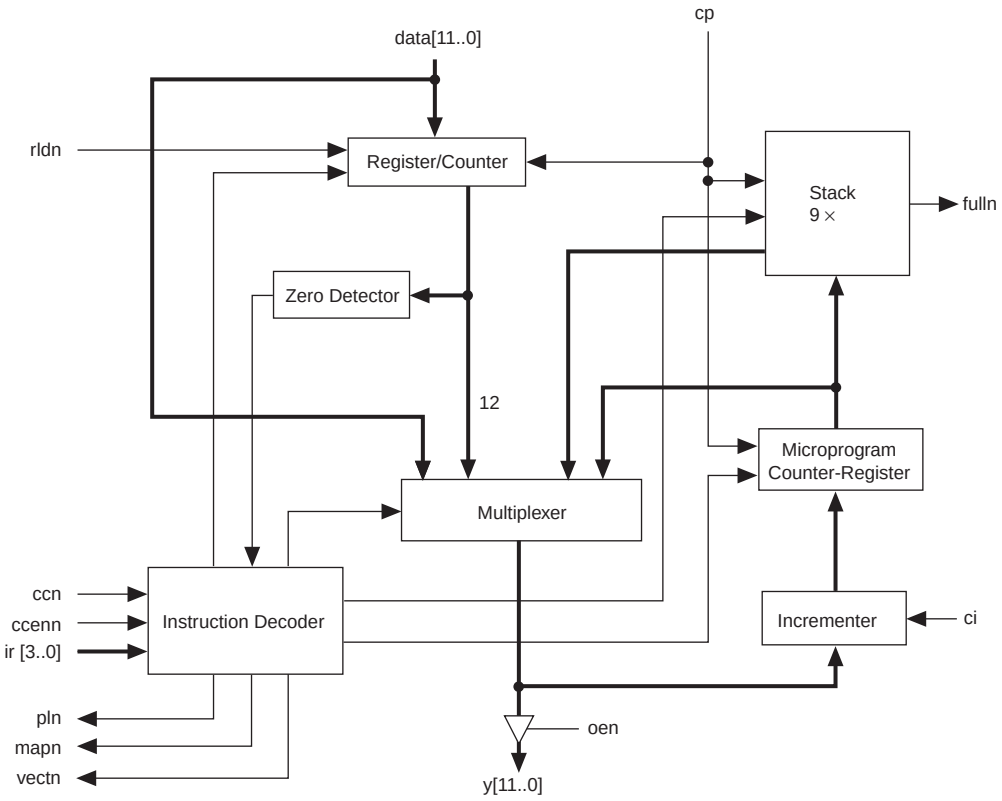
Modifiable Parameters

Parameter	Description
D	Data width
S	Stack width

Block Diagram

Figure 6 shows the block diagram for the 2910A microprogram controller.

Figure 6. 2910A Microprogram Controller Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	347	0	32 MHz	Contact CAST
EPF10K10A	-1	370	0	46 MHz	Contact CAST
EPF10K30E	-1	234	1	64 MHz	Contact CAST
EPF8636	-3	356	–	19 MHz	Contact CAST
EPF6016	-2	355	–	27 MHz	Contact CAST

6502 Microprocessor

Vendor: VAutomation
Target Application: General-purpose embedded computing and control
Additional Deliverables: Reference manual
ID Code: 3A0F-6502

- Code compatible with the Rockwell R65C02 device
- 70 instructions, 210 opcodes, 15 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

General Description

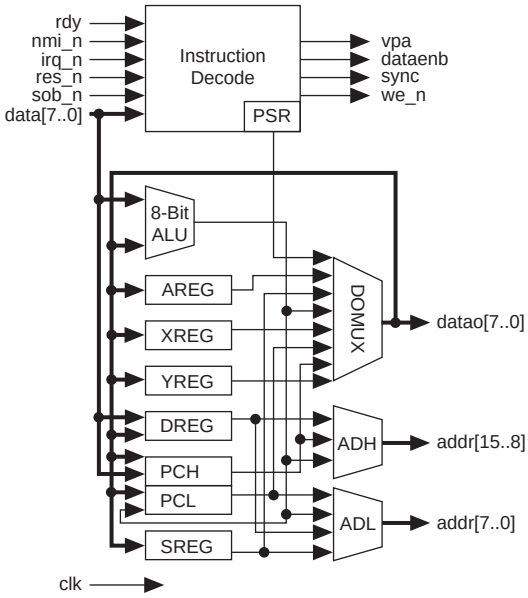
The 6502 microprocessor megafunction is a high-performance, 8-bit microprocessor. The megafunction is functionally based on and compatible with the Rockwell R65C02 device. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The 6502 microprocessor megafunction has been completely redesigned using the latest high-speed design techniques to produce a high-performance microprocessor with a minimal gate count. The megafunction is easily integrated with user-specified logic and other megafunctions.

Block Diagram

Figure 7 shows the block diagram for the 6502 microprocessor megafunction.

Figure 7. 6502 Microprocessor Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	920	0	14 MHz	Contact VAutomation

RISC805x Microcontroller

Vendor: Richard Watts Associates
Target Application: High-performance microcontroller, DSP alternative SoC solution
Additional Deliverables: Full user manual, example, test bench (VHDL versions)
ID Code: DE73-8052

- Fast performance 8051/8052 microcontroller with 100% software compatibility
- Up to eight times faster than a standard 8051/52 at the same clock frequency
- Eight data pointers/dual data pointers for faster data transfer
- Faster interrupt, multiply, and divide operations
- Optimized for Altera programmable logic devices (PLDs), with application-specific integrated circuit (ASIC) versions (in VHDL/Verilog HDL) available for easy migration
- Available as CPU (bare core) only, 8051, and 8052 variations
- Optional RISC805× extended 16-bit opcodes for faster 16-bit data operations
- Various options available for highest flexibility
- Supports full 64K program and data memory range
- Evaluation board available for prototyping and testing
- TRAP instruction, powerdown, and idle modes
- Fully static and synchronous design without internal tri-state buses

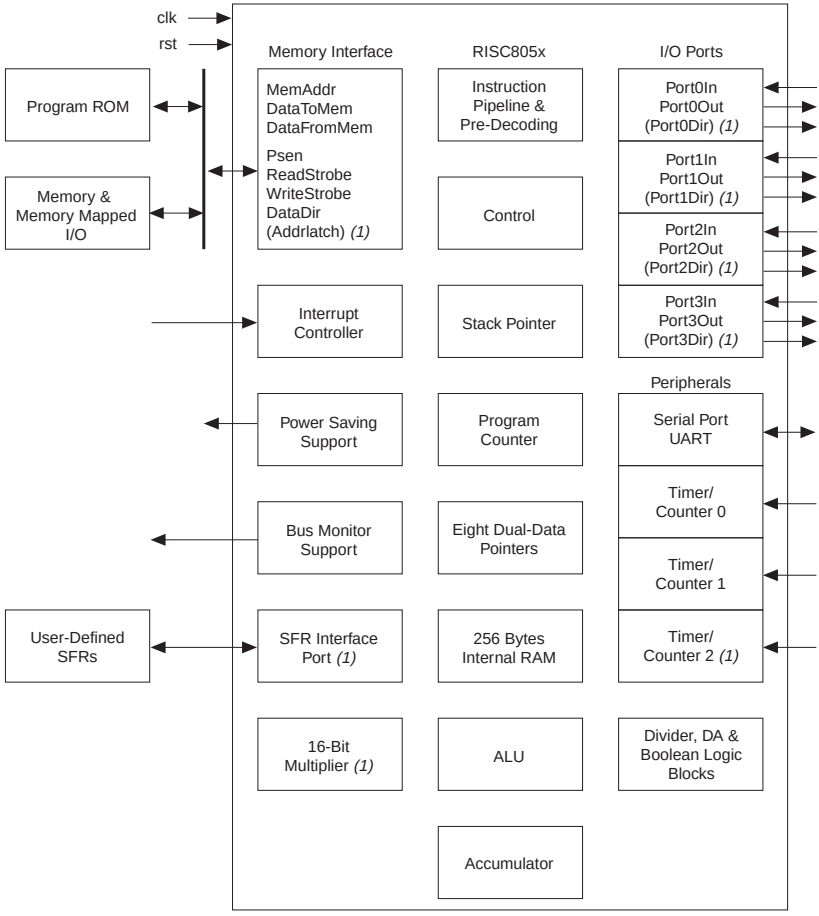
General Description

The RISC805x megafunction is a high performance 805× microcontroller using an optimized pipelined architecture so that most single byte instructions take only one clock cycle to execute. On average, the megafunction executes software eight times faster than a standard 805x, while maintaining 100% software code compatibility. Eight data pointers or dual data pointers are provided to speed up data transfer. Optional RISC805x 16-bit extended opcodes allow 16-bit data transfer and 16-bit calculation (e.g., ADD, MPY, MAC) by a single instruction. Users can also add their own special function registers (SFRs) with the optional SFR bus port. A memory extension option is also available for taking the addressing range up to 4 Mbytes by memory bank switching.

Block Diagram

Figure 8 shows the block diagram for the RISC805× microcontroller megafunction.

Figure 8. RISC805x Microcontroller Block Diagram



Note:
(1) These features may not exist in some options

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50E	-1	2,566	1	13.81 MHz	8051 barecore
EPF10K100	-1	3,056	1	12.46 MHz	8051 without extended opcode

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100E	-1	3,250	1	11.03 MHz	8052 without extended opcode
		4,162	1	12.50 MHz	8052 with extended opcode

8-µRISC

Vendor: VAutomation
Target Application: General-purpose embedded computing and control
Additional Deliverables: Reference manual
ID Code: 3A0F-B008

- RISC architecture for low gate count and high performance
- High code density, many opcodes are a single byte
- 33 opcodes and 4 addressing modes
- 8-bit ALU
- 64-Kbyte addressing capability
- Eight 8-bit general-purpose registers
- Multiple register banks that minimize interrupt latency
- 16-bit program counter and stack pointer
- Seven maskable interrupts, one non-maskable interrupt
- Assembler, C compiler, simulator, and on-chip, ice-like debugger available
- IntelliCore Prototyping System available for evaluation and rapid product development

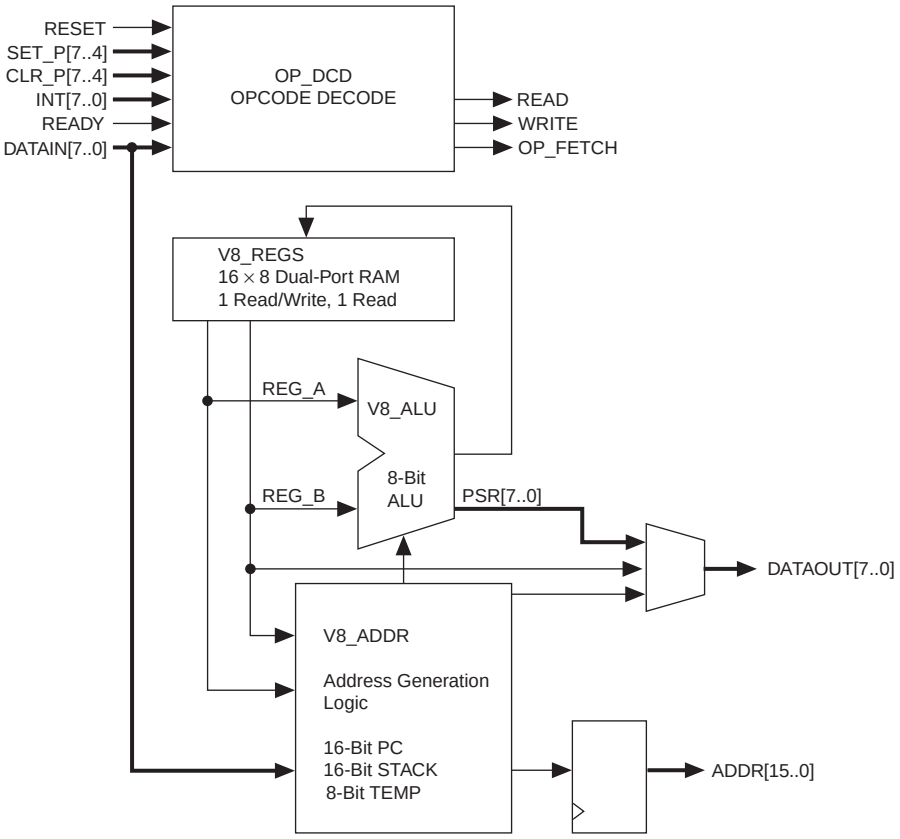
General Description

The 8-bit RISC microprocessor (8-µRISC) megafunction is a general-purpose processor function. It combines a small gate count with single clock cycle execution for many instructions to deliver a high-performance 8-bit microprocessor with a very small footprint. The 8-µRISC megafunction comes with a set of standard peripherals, including a timer, UART, power-save unit, IIC EEPROM interface, P1284 parallel interface, and page register design to expand the address space to 8 Mbytes. The megafunction and its peripherals allow high-performance custom microcontrollers to be implemented within Altera PLDs.

Block Diagram

Figure 9 shows the block diagram for the 8-µRISC megafunction.

Figure 9. 8-µRISC Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	827	0	12 MHz	Contact VAutomation

VZ80 Microprocessor

Vendor: VAutomation
Target Application: General-purpose embedded computing and control
Additional Deliverables: Reference manual
ID Code: 3A0F-BA80

- Code compatible with the Zilog Z80 device
- 158 instructions, 10 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

General Description

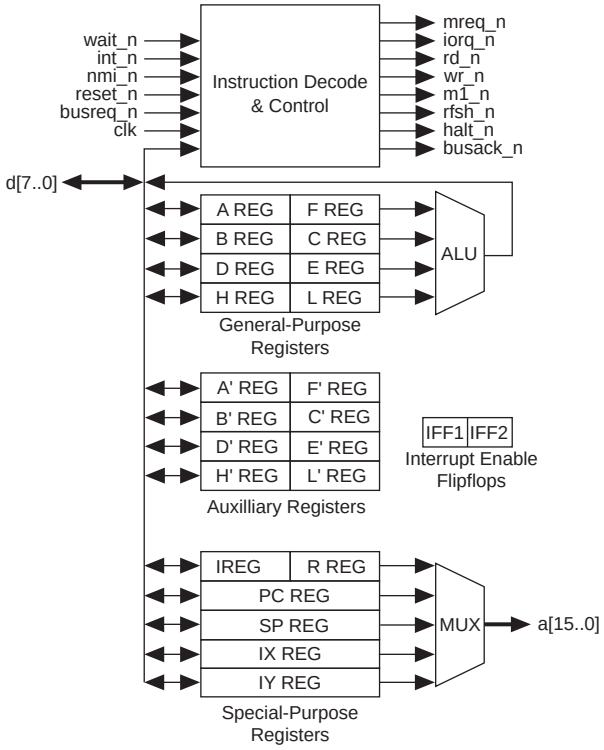
The VZ80 microprocessor megafunction is a powerful, medium-gate-count microprocessor that includes block transfers and bit test, set, and reset instructions. The megafunction is functionally based on and compatible with the Zilog Z80 device. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The megafunction has fast context switch capability with an entire auxiliary register set. The megafunction is easily integrated with user-specified logic and other megafunctions.

Block Diagram

Figure 10 shows the block diagram for the VZ80 microprocessor megafunction.

Figure 10. VZ80 Microprocessor Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40	-3	2,028	0	10 MHz	Contact VAutomation

Xtensa 32-Bit Microprocessor

Vendor: Tensilica, Inc.
Target Application: High-volume embedded applications
Additional Deliverables: Configured synthesizable RTL, ISS, on-chip debug, complete software development tools, EDA scripts
ID Code: 32A8XT15

- 32-bit processor
- 16/24-bit Xtensa instruction set architecture (ISA)
- 16-bit multiplier, MAC16
- Register file size of 32 or 64 entries
- On-chip debug
- Up to 16 Kbytes instruction cache and 16 Kbytes data cache
- On-chip ROM/RAM options
- System Support
- Prototyping board available with EPF10K200E or EP20K400 devices

General Description

The Xtensa 32-bit microprocessor megafunction is the first processor architecture designed specifically to address embedded application challenges. It was designed to be a configurable architecture so designers could tailor and adapt the implementation to match the specific embedded application requirements. The megafunction delivers major technologies to the system designers for building system-on-a-chip embedded designs.

This megafunction is a highly configurable and extensible 32-bit synthesizable processor. A family of processors can be built around the base ISA to target code size, performance, die size, and power dissipation.

The Xtensa Processor Generator is an easy to use browser-like interface used to select the various parameters for a wide variety of configurable options. The designer can select or add new instructions, co-processors, memory sub-system configurations, system exceptions, and debugging support. By entering the desired performance level, power dissipation, and area goals, the system designer can affect the final embedded system on-chip characteristics.

The Xtensa software development environment is a GNU-based software tool suite that is generated to match the configured processor architecture. This configuration includes a GNU C/C++ compiler, macro assembler, linker, debugger, diagnostics, reference test benches, cycle accurate instruction set simulator, and basic library. All tools are automatically generated to match the exact configuration as defined by user of the Processor Generator.

The Tensilica Instruction Extension language (TIE) allows the designer to describe the custom functions for each application. The resultant outputs of TIE implementation include: correct-by-construction hardware description language (HDL), compiler, assembler, simulator, and debugger. The TIE language can be used to describe extensions and new instructions to augment the Xtensa ISA.

Modifiable Parameters

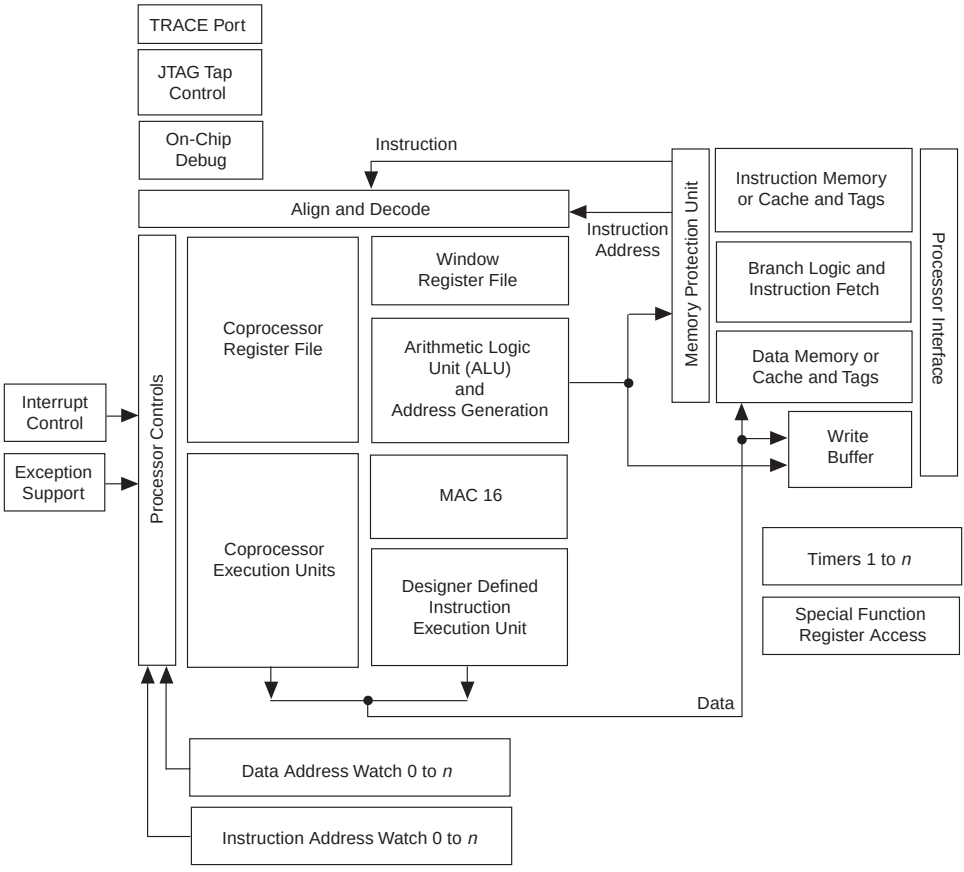
The Xtensa processor generator features the following configurable parameters:

- 16-bit multiplier
- MAC16
- Window register file option of 32 × 32-bit or 64 × 32-bit registers
- Memory subsystem:
  - Instruction cache 1 Kbytes to 16 Kbytes
  - Instruction cache line 16 bytes to 64 bytes
  - Data cache 1 Kbytes to 16 Kbytes
  - Data cache line 16 Bytes to 64 Bytes
  - Write buffer 4 to 32 entries
  - On-chip ROM, RAM up to 16 Kbytes
  - Big or little endien byte ordering
- Exceptions:
  - 0 to 32 external interrupts
  - NMI
  - Interrupt priority
  - 32-bit timers
- Address trace and pipeline port
- Instruction/data break point support
- Verification support
- Simulation model
- Silicon optimization goals

Block Diagram

Figure 11 shows the block diagram Xtensa 32-bit microprocessor megafunction.

Figure 11. Xtensa 32-Bit Microprocessor Block Diagram



Contact Tensilica for performance numbers.

DES-Core

Vendor: SICAN
Target Application: Secured communications, electronic commerce, WAN/LAN routers
Additional Deliverables: Documentation
ID Code: 18CD-4A76

- Altera-optimized implementation of the digital encryption standard
- Fast data encryption/decryption using the data encryption standard (DES) algorithm
- Triple-DES support
- 56-bit or 112-bit key length (using triple-DES)
- 64 Mbits/second encryption speed
- Key change within one clock cycle
- Electronic code block (ECB) mode
- Encryption/decryption performed in 16 clock cycles

General Description

The SICAN `DES-Core` megafunction provides high-speed data encryption/decryption using the industry-standard DES algorithm. With its high throughput of 64 Mbits/second, the `DES-Core` megafunction is a perfect choice for a variety of applications requiring secured communications. It accepts 64-bit parallel data input and processes one DES operation in 16 clock cycles. The output is 64 bits wide.

The `DES-Core` megafunction can be configured for either encryption or decryption operation and can be switched between normal DES mode and triple DES mode. It accepts a 56-bit key in DES mode or a 112-bit key in triple DES mode.

Due to export restrictions, this megafunction may not be available to customers located outside the United States and Canada, or to certain foreign nationals located in the United States. Customers should contact SICAN directly for further information regarding export restrictions.

It is the customer's responsibility to check with the relevant authorities regarding the re-export of components containing encryption technology.

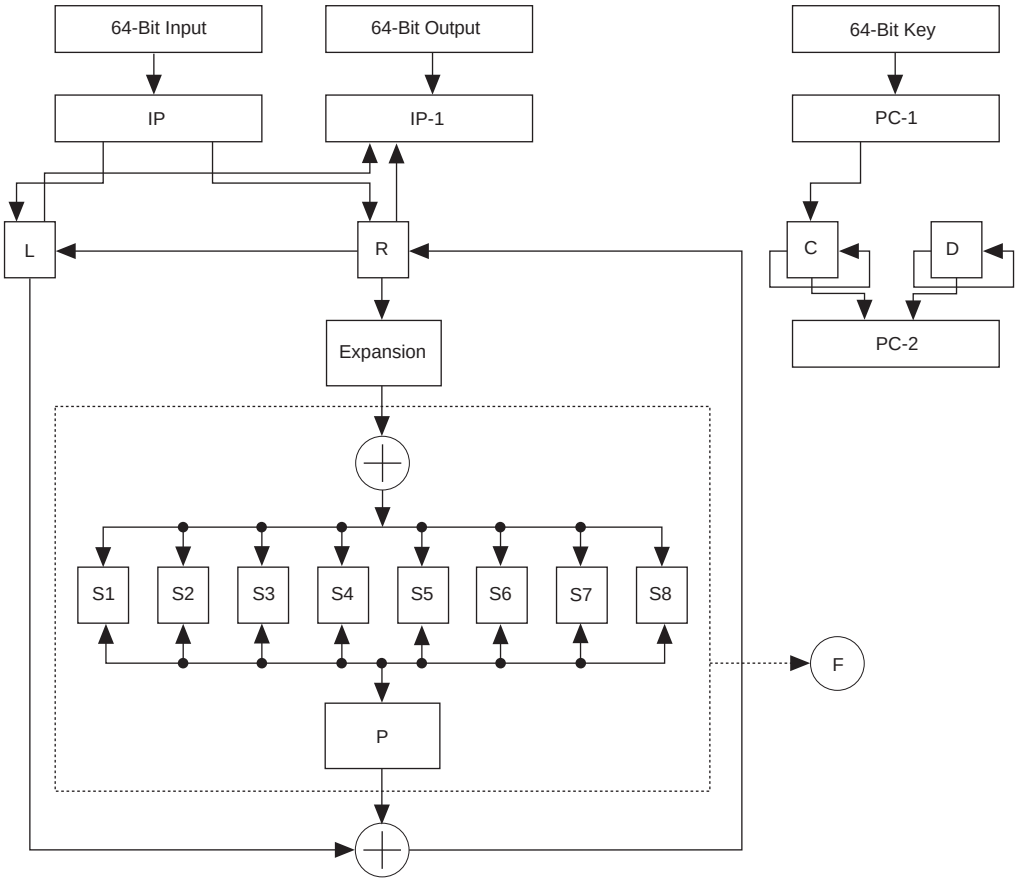
Modifiable Parameters

SICAN can modify the key length (`L`) and mode type (`M`) to meet user requirements.

Block Diagram

Figure 12 shows the block diagram of the `DES-Core` megafunction.

Figure 12. DES-Core Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K50V	-1	574	0	27 MHz	L = 56 bits

X_DES Cryptoprocessor

Vendor: CAST
Target Application: Secured communications, electronic commerce, wide-area network (WAN) and local-area network (LAN) routers
Additional Deliverables: VHDL testbench, user guide
ID Code: 2AA5-C019

- Fully compliant 56-bit DES implementation
- Supports encryption and decryption
- Encryption and decryption performed in 16 clock cycles
- No dead cycles for key loading or mode switching
- Suitable for triple DES implementations
- Suitable for electronic code block (ECB), cypher block coding (CBC), cypher feedback (CFB), and output feedback (OFB) implementations
- Sustained bit rate is 4× clock speed
- High clock speed and low gate count achieved
- Fully synchronous design
- Available as fully functional and synthesizable VHDL or Verilog HDL source code
- Test benches provided

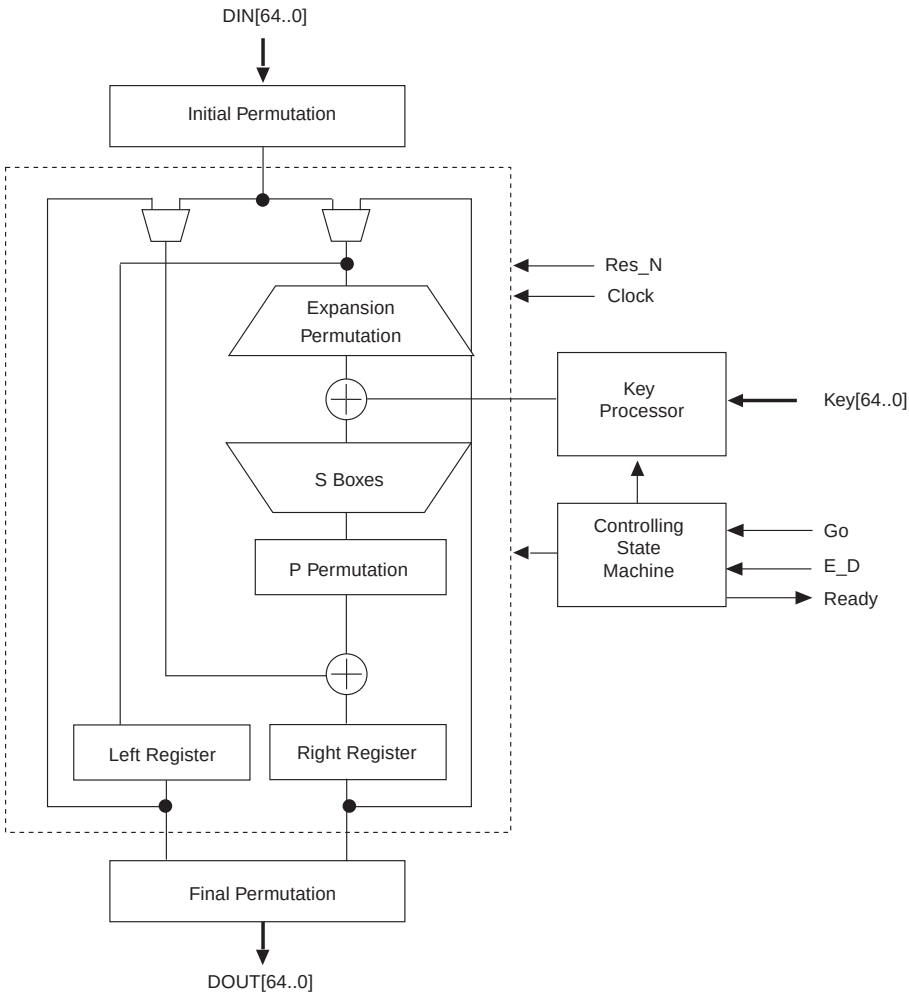
General Description

The X_DES megafunction is a fully compliant hardware implementation of the DES encryption algorithm, suitable for a variety of applications. The DES is a block cipher that encrypts and decrypts data in 64-bit blocks using a 56-bit key.

Block Diagram

Figure 13 shows the block diagram of the X_DES Cryptoprocessor megafunction.

Figure 13. X_DES Cryptoprocessor Block Diagram



Functional Description

After an initial permutation, the megafunction splits the input data into two 32-bit words, and directs the results left and right in 16 identical operation cycles.

The right word is processed with an expansion permutation, XORed with the processed key, and substituted using S boxes. The output of the S boxes is permuted and then XORed with the left word. At the end of each round, the resulting data updates the right word register, and the initial right word is stored in the left word register. The shift and permutation operations allow the processed key to change in every round.

After the last operation is completed, the left and right words are reassembled and passed through the inverse of the initial permutation. The X_DES megafunction determines whether to encrypt or decrypt by reading the level of the E_D signal input port. A rising input on the GO port triggers a cryptographic operation on the DIN signal using the KEY signal as the key. The DES algorithm allows only 56 of the 64 bits of the KEY input port to be read by the megafunction. One bit out of every eight bits is ignored from the KEY input, and after 16 clock cycles, the READY output indicates that the DOUT signal value is valid.

Device Utilization Example

Device	Speed Grade	Utilization		Performance (f_{MAX})	Parameter Settings
		Logic Cells	EABs		
EPF6016	-2	540	–	37 MHz	Contact CAST
EPF81500	-2	540	–	35 MHz	Contact CAST
EPF10K20	-3	540	–	44 MHz	Contact CAST
EPF10K30A	-1	570	–	73 MHz	Contact CAST

Availability

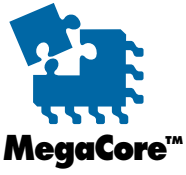
The X_DES megafunction, licensed from Xentec Inc., is available for export to the countries listed below:

- Belgium-Luxemburg
- Brazil
- Canada
- China
- Denmark
- Germany
- Finland
- France
- Italy
- Japan
- Netherlands
- Norway
- South Korea
- Singapore
- Spain
- Sweden
- Taiwan
- UK
- USA

It is the customer's responsibility to check with the relevant authorities regarding the re-export of components containing encryption technology.

a6402 Universal Asynchronous Receiver/Transmitter

Vendor: Altera
Target Application: Microprocessor peripherals, serial data communications applications, modem interface
Additional Deliverables: a6402 Universal Asynchronous Receiver/Transmitter Data Sheet
Ordering Code: PLSM-6402



- a6402 MegaCore function implementing a universal asynchronous receiver/transmitter (UART)
- Optimized for APEX™, FLEX®, and MAX® architectures
- Programmable word length, stop bits, and parity
- Full duplex operation
- Includes status flags for parity, framing, and overrun errors

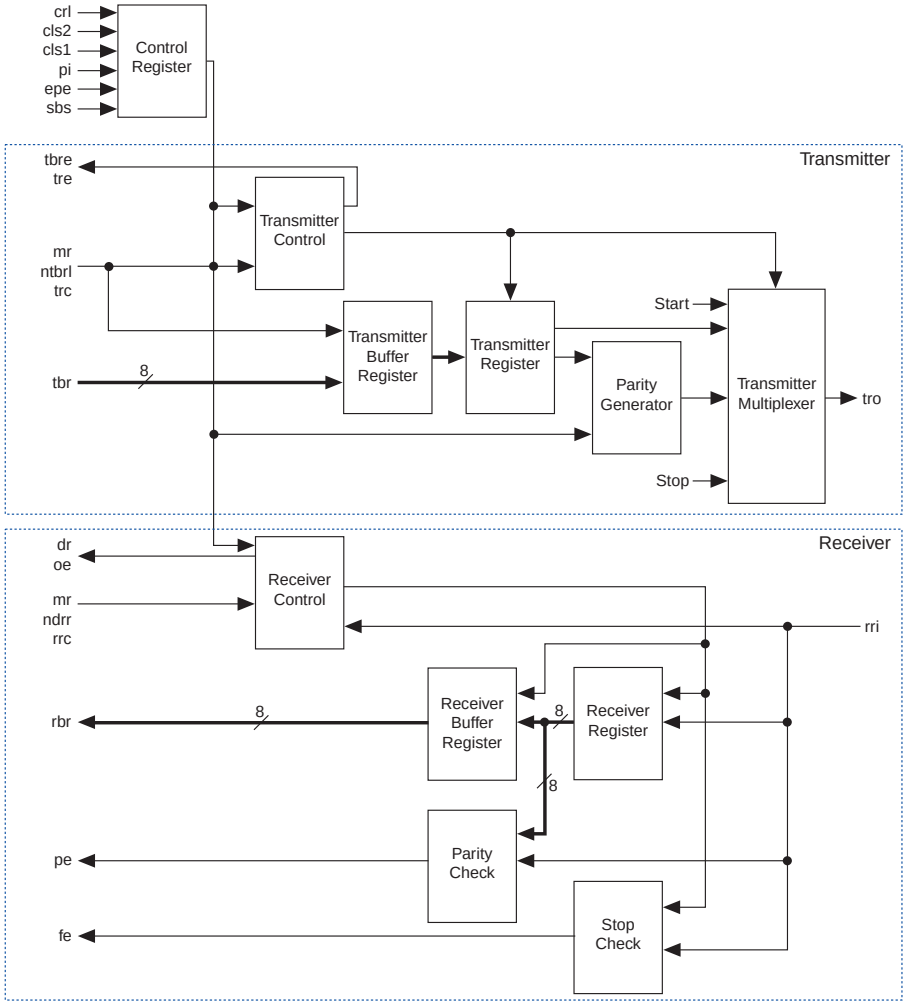
General Description

The a6402 MegaCore function implements a universal asynchronous receiver/transmitter (UART), which provides an interface between a microprocessor and a serial communications channel.

Block Diagram

Figure 14 shows the block diagram for the a6402 ACIA megafunction.

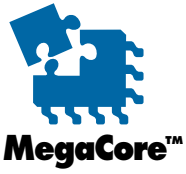
Figure 14. a6402 Universal Asynchronous Receiver/Transmitter Block Diagram



For more information, see the *a6402 Universal Asynchronous Receiver/Transmitter Data Sheet*.

a6850 Asynchronous Communications Interface Adapter

Vendor: Altera
Target Application: Microprocessor peripherals, serial data communications applications, modem interface
Additional Deliverables: a6850 Asynchronous Communications Interface Adapter Data Sheet
Ordering Code: PLSM-6850



- a6850 MegaCore function implementing an asychronous communications interface adapter (ACIA)
- Optimized for APEX, FLEX, and MAX architectures
- Programmable word lengths, stop bits, and parity
- Offers divide-by-1, -16, or -64 mode
- Includes error detection

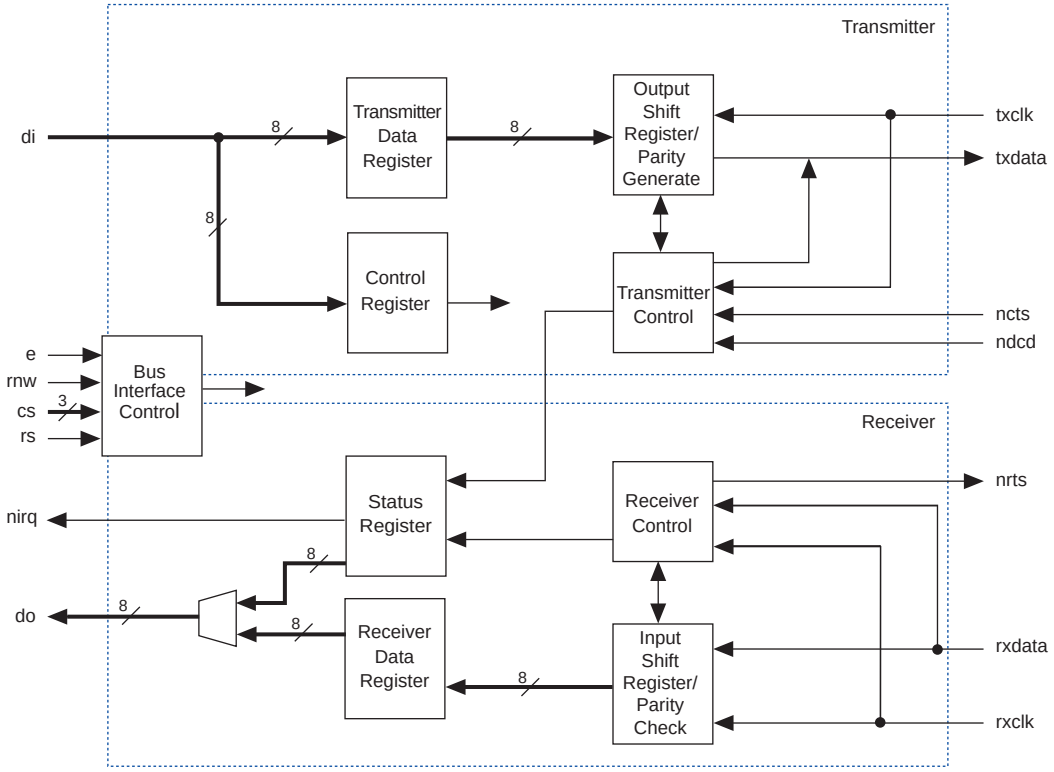
General Description

The a6850 MegaCore function implements an ACIA, which is a universal asynchronous receiver/transmitter (UART). The a6850 provides an interface between a microprocessor and a serial communications channel. The a6850 receives and transmits data in a variety of configurations, including 7- or 8-bit data words, with odd, even, or no parity, and 1 or 2 stop bits.

Block Diagram

Figure 15 shows the block diagram for the a6850 asynchronous communications interface adapter megafunction.

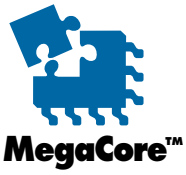
Figure 15. a6850 Asynchronous Communications Interface Adapter Block Diagram



For more information, see the *a6850 Asynchronous Communications Interface Adapter Data Sheet*.

a8237 Programmable DMA Controller

Vendor: Altera
Target Application: Microprocessor peripherals, memory controllers, bus controllers, serial data communications applications, modem interface
Additional Deliverables: a8237 Programmable DMA Controller Data Sheet
Ordering Code: PLSM-8237



- a8237 MegaCore function implementing a programmable direct memory access (DMA) controller
- Optimized for APEX and FLEX architectures
- Provides four independent channels
- Offers static read/write or handshaking modes
- Includes direct bit set/reset capability
- Functionally based on the Intel 8237A and Harris 82C37A devices,

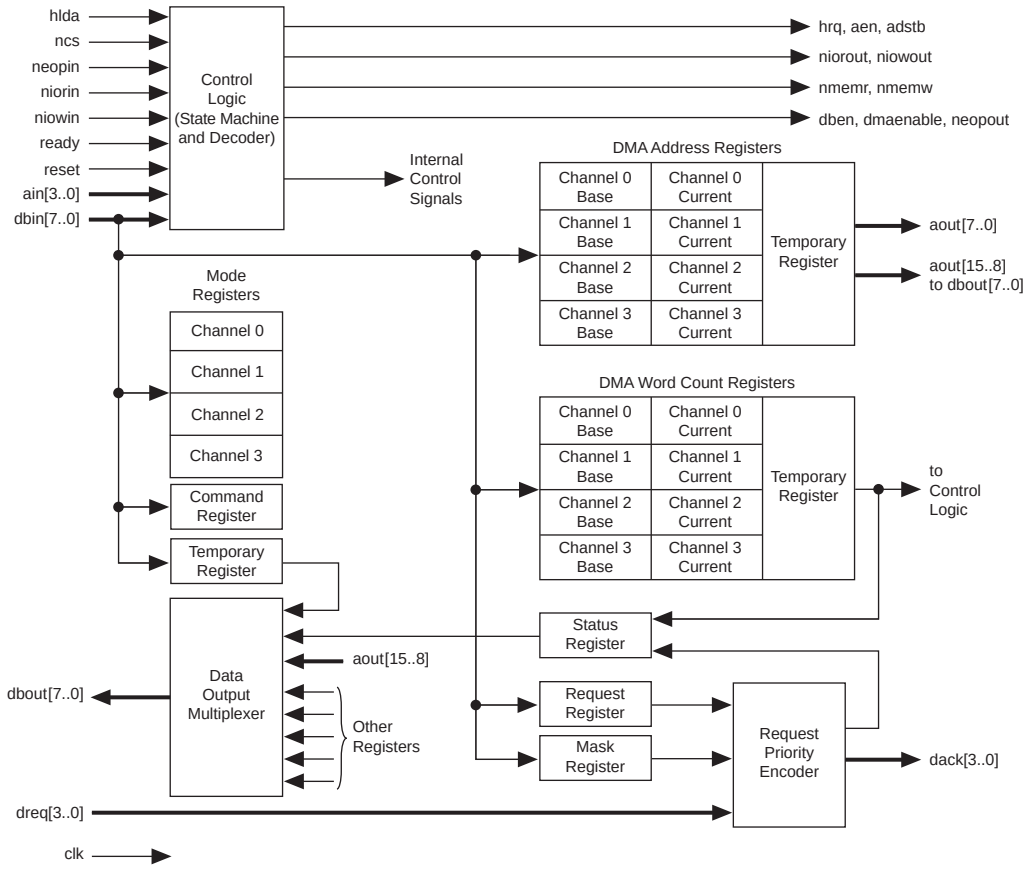
General Description

The a8237 MegaCore function implements a programmable DMA controller, which controls memory-to-peripheral and memory-to-memory data transfers and provides block memory initialization capability. Four independently programmable channels are available in the a8237, and DMA requests can be made via hardware or software.

Block Diagram

Figure 16 shows the block diagram for the a8237 programmable DMA controller megafunction.

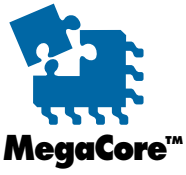
Figure 16. a8237 Programmable DMA Controller Megafunction Block Diagram



For more information, see the *a8237 Programmable DMA Controller Data Sheet*.

a8251 Programmable Communications Interface

Vendor: Altera
Target Application: Microprocessor peripherals, serial data communications applications, modem interface
Additional Deliverables: a8251 Programmable Communications Interface Data Sheet
Ordering Code: PLSM-8251



- a8251 MegaCore function that provides an interface between a microprocessor and a serial communication channel
- Optimized for APEX and FLEX architectures
- Programmable word length, stop bits, and parity
- Offers divide-by-1, -16, or -64 mode
- Supports synchronous and asynchronous operation
- Includes:
  - Error detection
  - False start bit detection
  - Automatic break detection
  - Internal and external sync character detection

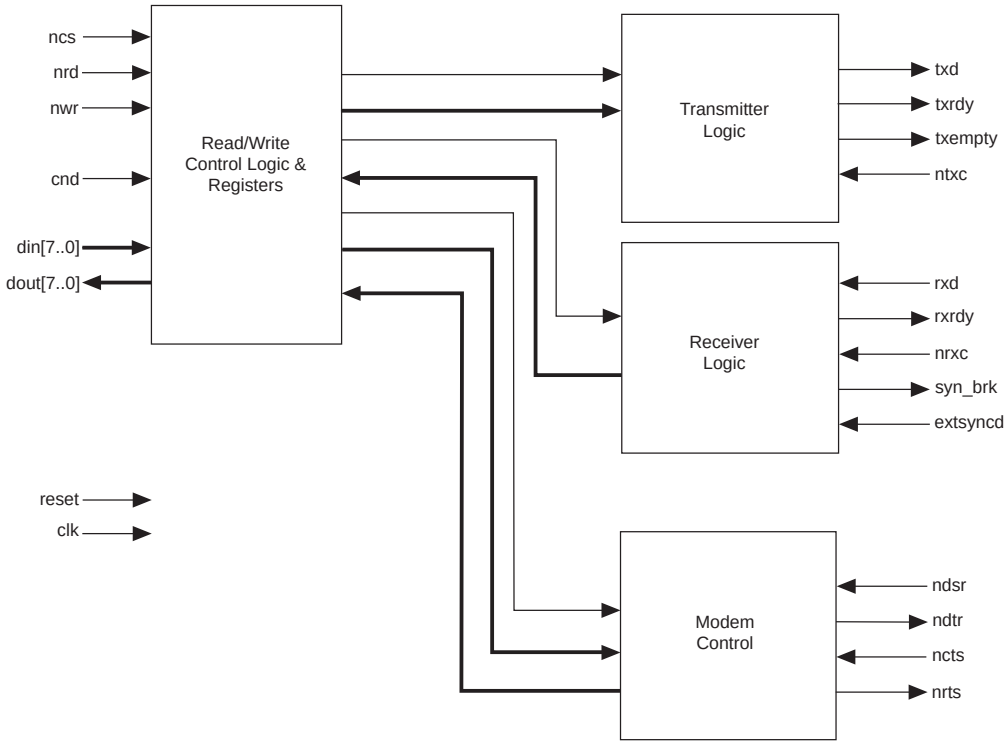
General Description

The a8251 MegaCore function provides an interface between a microprocessor and a serial communications channel. The a8251 receives and transmits data in a variety of configurations including 7- or 8-bit data words, with odd, even, or no parity, and 1 or 2 stop bits. The transmitter and receiver can be designed for synchronous or asynchronous operation.

Block Diagram

Figure 17 shows the block diagram for the a8251 programmable communications interface megafunction.

Figure 17. a8251 Programmable Communications Interface Block Diagram



For more information, see the *a8251 Programmable Communications Interface Data Sheet*.

8251 Programmable Communications Interface

Vendor: CAST
Target Application: Serial data communications applications, modem interface
Additional Deliverables: VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C012

- Synchronous and asynchronous operation
- Programmable data word length, parity, and stop bits
- Parity, overrun, and framing error checking instructions and counting loop interactions
- Supports transmission rates up to 1.750 Mbps
- Divide-by-1, -16, and -64 mode
- False start bit deletion
- Automatic break detection
- Internal and external synchronous character detection
- Peripheral modem control functions
- Developed in VHDL and synthesizes to approximately 2,300 gates
- Functionality based on the Intel 8251A device

General Description

The 8251 programmable communications interface megafunction provides data formatting and control to a serial communications channel.

The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting both synchronous and asynchronous operation.

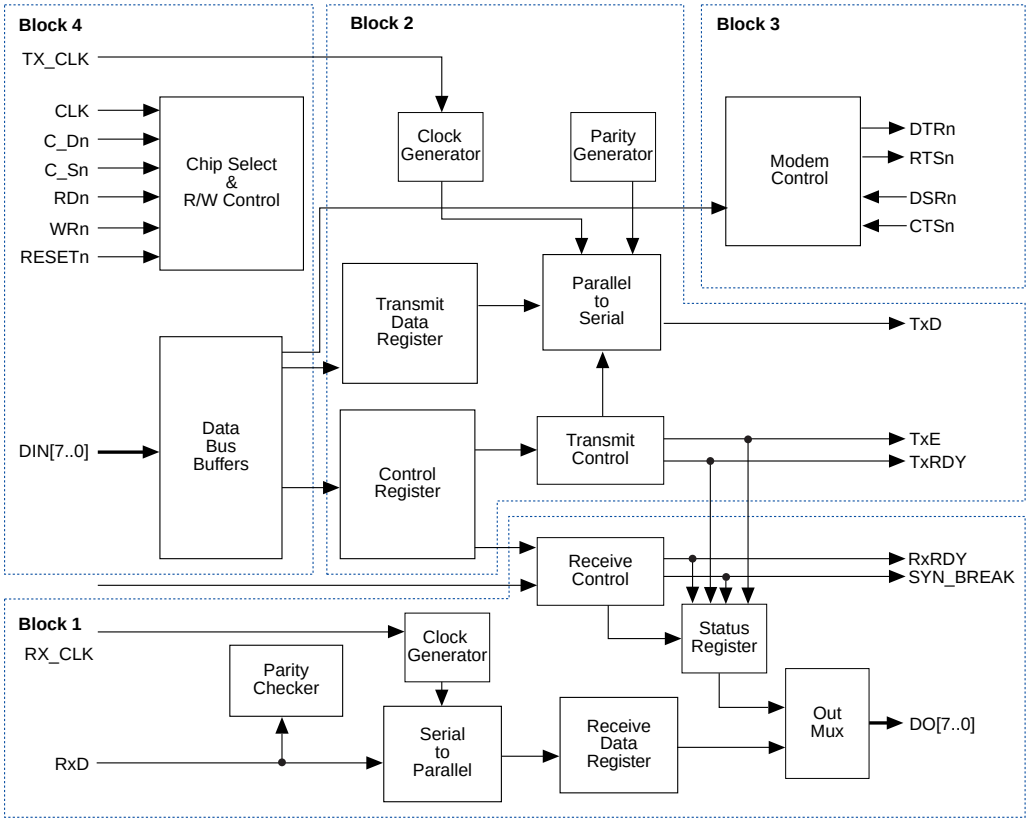
Modifiable Parameters

The 8251 megafunction can be customized to include a 16-bit internal baud rate generator. Either the synchronous or asynchronous sections can be removed to reduce the overall logic utilization. Contact CAST directly for any required modifications.

Block Diagram

Figure 18 shows the block diagram for the 8251 programmable communications interface megafunction.

Figure 18. 8251 Programmable Communications Interface Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	533	–	16 MHz	Contact CAST
EPF10K10A	-1	533	–	25 MHz	Contact CAST
EPF8220A	-2	533	–	12 MHz	Contact CAST
EPF6010A	-1	533	–	19 MHz	Contact CAST

8254 Programmable Interval Timer/Counter

Vendor: CAST
Target Application:
Event counters, elapsed-time indicators, programmable one-shots
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C016

- Status read-back command
- Counter latch command
- Read/write least significant bit (LSB) only, most significant bit (MSB) only, or LSB first then MSB
- Six programmable counter modes
  - Interrupt on terminal count
  - Hardware retriggerable one-shot
  - Rate generator
  - Square wave mode
  - Software-triggered strobe
  - Hardware-triggered strobe (retriggerable)
- Binary or binary coded decimal (BCD) strobe
- Developed in VHDL and synthesizes to approximately 5,000 gates
- Functionally based on the Intel 82C54 device

General Description

The 8254 programmable interval time/counter megafunction is a high-performance function that is designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, and each counter may operate in a different mode. All modes are software programmable. The 8254 megafunction solves one of the most common problems in any microcomputer system: the generation of accurate time delays under software control. Instead of setting up timing loops in software, the 8254 megafunction can be programmed to match requirements by programming one of the counters for the desired delay.

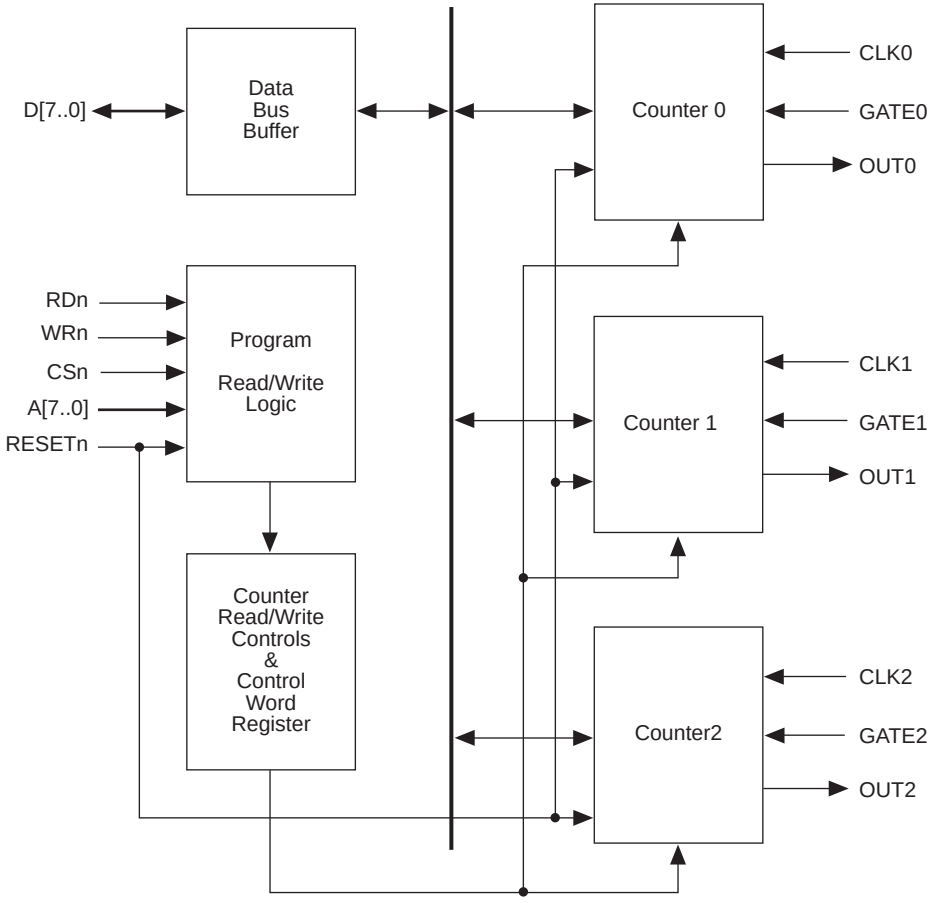
Modifiable Parameters

The 8254 megafunction can be customized to include additional counters. Contact CAST for any required modifications.

Block Diagram

Figure 19 shows the block diagram for the 8254 programmable interval timer/counter megafunction.

Figure 19. 8254 Programmable Interval Timer/Counter Block Diagram

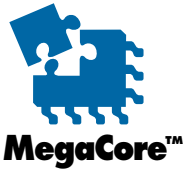


Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	720	–	24 MHz	Contact CAST
EPF10K30A	-1	727	–	31 MHz	Contact CAST

a8255 Programmable Peripheral Interface Adapter

Vendor: Altera
Target Application: Microprocessor peripherals, bus controllers, peripheral interfaces, serial data communications applications, modem interface
Additional Deliverables: a8255 Programmable Peripheral Interface Adapter Data Sheet
Ordering Code: PLSM-8255



- a8255 MegaCore function implementing a programmable peripheral interface adapter
- Optimized for APEX, FLEX, and MAX architectures
- 24 programmable inputs/outputs
- Static read/write or handshaking modes
- Direct bit set/reset capability
- Synchronous design

General Description

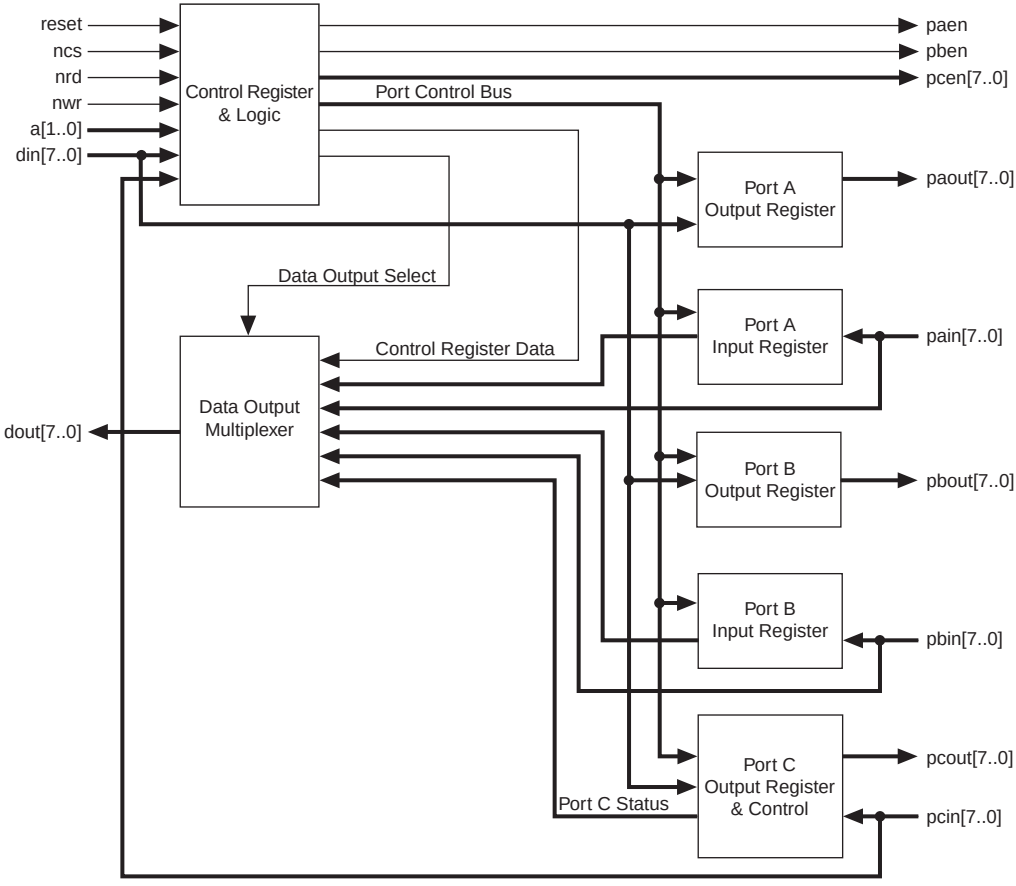
The a8255 MegaCore function implements a programmable peripheral interface adapter. The a8255 function has 24 I/O signals that can be programmed in two groups of 12. This MegaCore function operates in the following three modes:

- *Mode 0: Basic Input/Output*—Port A, port B, and port C (upper and lower) can be independently configured as inputs or outputs to read or hold static data. Outputs are registered; inputs are not registered.
- *Mode 1: Strobed Input/Output*—Port A and port B can be independently configured as strobed input or output buses. Signals from port C are dedicated as control signals for data handshaking.
- *Mode 2: Bidirectional Bus*—Port A can be configured as a bidirectional bus with the majority of port C providing the control signals. In this configuration, port B can still implement mode 0 or mode 1.

Block Diagram

Figure 20 shows the block diagram for the a8255 programmable peripheral interface adapter megafunction.

Figure 20. a8255 Programmable Peripheral Interface Adapter Block Diagram



For more information, see the *a8255 Programmable Peripheral Interface Adapter Data Sheet*.

8255A Programmable Peripheral Interface

Vendor: CAST
Target Application: Printers, keyboards, displays, floppy disk controllers, cathode ray tube (CRT) controllers, machine tools, D/A and A/D converters
Additional Deliverables: VHDL testbench
ID Code: 2AA5-C007

- Three 8-bit peripheral ports: A, B, C
- Three programming modes for peripheral ports
  - Mode 0 (basic input/output)
  - Mode 1 (strobed input/output)
  - Mode 2 (bidirectional)
- All ports are set to input after reset
- Total of 24 programmable I/O lines
- Eight-bit bidirectional system data bus with standard microprocessor interface controls
- Developed in VHDL and synthesized up to 1,000 gates, depending on the process used
- Functionally based on the Intel 8255A device

General Description

The 8255A programmable peripheral interface megafunction implements a general-purpose I/O interface to connect peripheral equipment to a microcomputer system bus. The megafunction's functional configuration is programmed by the system software so that external logic is not required to interface peripheral devices.

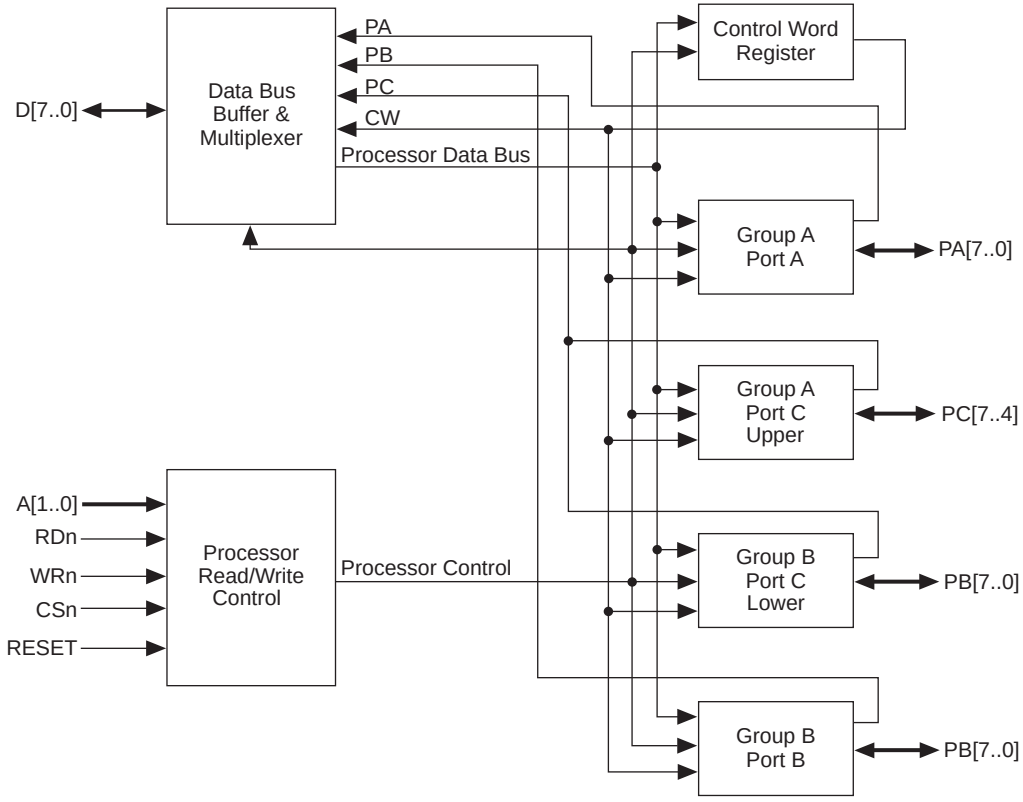
Modifiable Parameters

The 8255A megafunction can be customized to include additional ports. Contact CAST for any required modifications.

Block Diagram

Figure 21 shows the block diagram for the 8255A programmable peripheral interface megafunction.

Figure 21. 8255A Programmable Peripheral Interface Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	178	–	81 MHz	Contact CAST
EPF10K10A	-1	177	–	138 MHz	Contact CAST

a8259 Programmable Interrupt Controller

Vendor: Altera
Target Application: Microprocessor peripherals, bus controllers, interrupt processing, serial data communications applications, modem interface
Additional Deliverables: a8259 Programmable Interrupt Controller Data Sheet
Ordering Code: PLSM-8259

- Optimized for APEX, FLEX, and MAX architectures
- Offers eight levels of individually maskable interrupts
- Expandable to 64 interrupts
- Offers a flexible priority resolution scheme
- Provides programmable interrupt modes and vectors

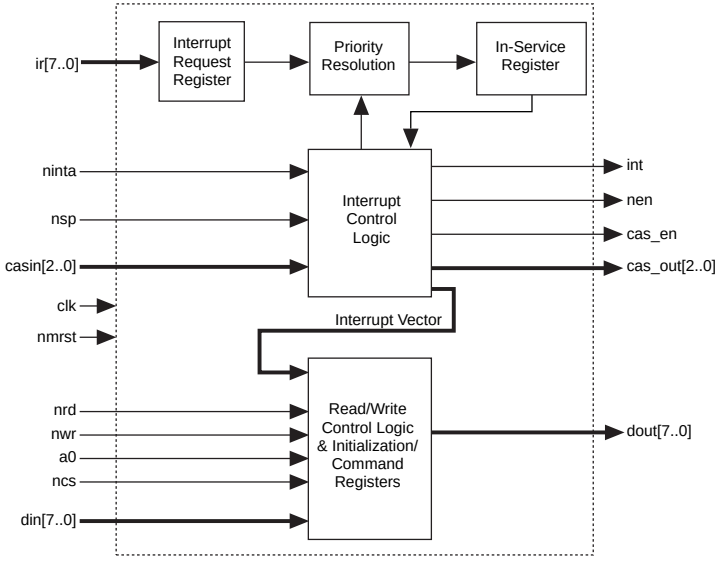
General Description

The Altera® a8259 MegaCore™ function is a programmable interrupt controller. The a8259 can be initialized by the microprocessor through eight data bus lines (din[7..0] and dout[7..0]), and the ncs, nrd, nwr, int, and ninta control signals.

Block Diagram

Figure 22 shows the block diagram for the a8259 programmable interrupt controller megafunction.

Figure 22. a8259 Programmable Interrupt Controller Block Diagram



For more information, see the *a8259 Programmable Interrupt Controller Data Sheet*.

8259 Programmable Interrupt Controller

Vendor: Innocor
Target Application: Interrupt-driven microcomputer
Additional Deliverables: User manual, simulation files
ID Code: 5911

- Eight-level priority controller
- Individual request mask capability
- Edge triggered detection
- Can be cascaded to allow more requests
- Automatic end of interrupt
- Read of interrupt and interrupt in-service
- Developed in Verilog HDL

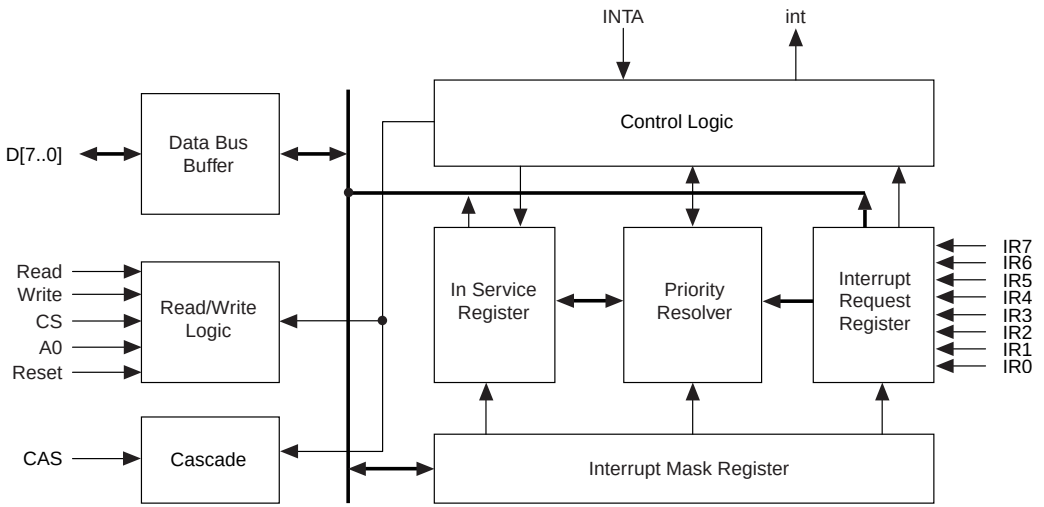
General Description

The 8259 programmable interrupt controller (PIC) is functionally based on the Intel 8259A. Eight interrupt requests are prioritized for a processor. To minimize size and maximize performance, Innocor's PIC has only selected functionality of the Intel 8259A.

Block Diagram

Figure 23 shows the block diagram of the 8259 PIC megafunction.

Figure 23. 8259 PIC Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	173	0	86 MHz	Contact Innocor
EPF10K30E	-1	173	0	135 MHz	Contact Innocor
EPF6010A	-1	185	0	64 MHz	Contact Innocor

8259A Programmable Interrupt Controller

Vendor: CAST
Target Application:
Real-time, interrupt-driven microcomputer designs
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C013

- Eight vectored priority interrupts per megafunction. Up to 64 vectored priority interrupts with cascading
- Programming for all 8259A modes and operational features
  - MCS-80/85 and 8088/8086 processor modes
  - Fully nested mode and special fully nested mode
  - Special mask mode
  - Buffered mode
  - Pool command mode
  - Cascade mode with master or slave selection
  - Automatic end-of-interrupt mode
  - Specific and non-specific end-of-interrupt commands
  - Automatic rotation
  - Specific rotation
  - Edge- and level-triggered interrupt input modes
  - Reading of interrupt request register (IRR) and in-service register (ISR) through data bus
  - Writing and reading of interrupt mask register (IMR) through data bus
- Developed in VHDL and synthesizes up to 2,000 gates
- Functionally based on the Intel 8259A and Harris 82C59A devices

General Description

The 8259A programmable interrupt controller megafunction manages up to eight vectored priority interrupts for a processor. Using multiple instantiations of the megafunction and programming it to cascade mode allows up to 64 vectored interrupts. More than 64 vectored interrupts can be accomplished by programming the megafunction to poll command mode.

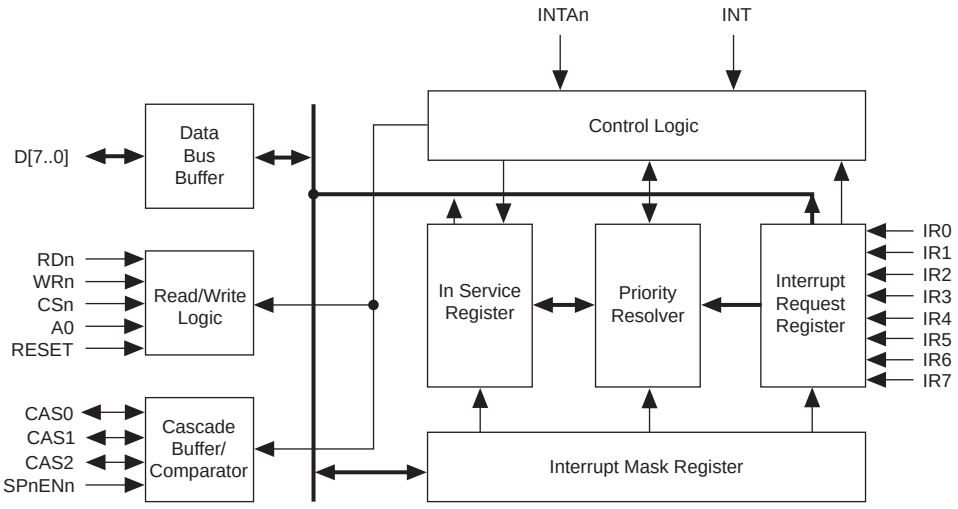
Modifiable Parameters

The 8259A megafunction can be customized to include a greater number of interrupts. Contact CAST for any required modifications.

Block Diagram

Figure 24 shows the block diagram for the 8259A programmable interrupt controller megafunction.

Figure 24. 8259A Programmable Interrupt Controller Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	453	–	17 MHz	Contact CAST
EPF10K10A	-1	454	–	24 MHz	Contact CAST
EPF8820A	-2	425	–	14 MHz	Contact CAST
EPF6010A	-1	424	–	24 MHz	Contact CAST

29116A 16-Bit Microprocessor

Vendor: CAST
Target Application:
16-bit microprocessor unit
Additional Deliverables:
VHDL testbench, simulation files
ID Code: 2AA5-5007

- 8- or 16-bit data width
- Powerful field insertion/extraction and bit manipulation instructions rotate and merge, or rotate and compare; bit manipulation instructions provided for complex bit control
- 32 working 16-bit registers
- 16-bit barrel shifter
- Immediate instruction capability may be used for storing constants in microcode or for configuring a second data port
- Developed in VHDL and synthesizes to approximately 3,800 gates (excluding RAM), depending on the process used
- Functionally based on the AMD AM29116A device

General Description

The 29116A 16-bit microprocessor megafunction is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set is optimized for high-performance peripheral controllers, such as graphics controllers, disk controllers, communications controllers, front-end concentrators, and modems. The device also performs well in microprogrammed processor applications. In addition to its complete arithmetic and logic instruction set, the megafunction's instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic redundancy code (CRC) generation.

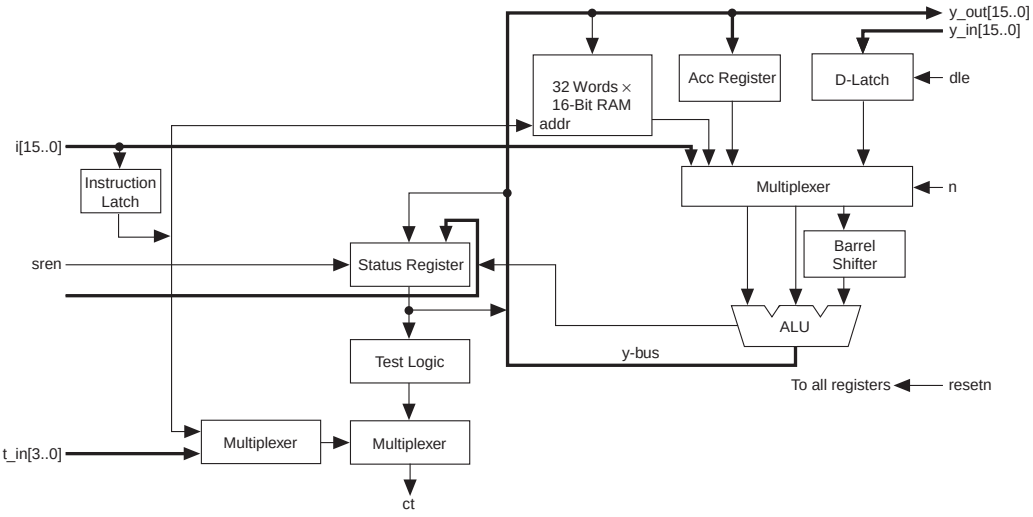
Modifiable Parameters

The 29116A 16-bit microprocessor megafunction can be customized to include a larger data width. Contact CAST directly for any required modifications.

Block Diagram

Figure 25 shows the block diagram for the 29116A 16-bit microprocessor.

Figure 25. 29116A 16-Bit Microprocessor Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,119	3	22 MHz	Data width = 16 bits
EPF10K20	-3	1,131	3	10 MHz	Data width = 16 bits
EPF6024	-2	1,948	–	9 MHz	Data width = 16 bits

SDRAM Controller

Vendor: Northwest Logic Design
Target Application: Networks, hard disk arrays, high-speed embedded applications, PowerPC systems, HDTV
Target Application: User's Guide, simulation files

- Clock speeds up to 100 MHz
- 32- or 64-bit wide data bus
- Full byte enable support
- Burst access with burst lengths of four or eight words
- Efficient bank hit management
- Supports four simultaneously open banks
- Error correction/detection
- Memory depth up to 64 MBytes
- Supports standard memory modules such as 168-pin DIMM and 144-pin SO-DIMM
- Parameterized timing specifications
- Pipelined access to maximize throughput
- Automatic SDRAM initialization at power-up
- Serial presence detect EPROM support
- Automatic refresh

General Description

The synchronous dynamic random access memory (SDRAM) controller megafunction has been designed for use in high-speed, memory-intensive designs. The megafunction is intended to be used as a stand-alone field programmable gate array (FPGA) or as a functional block incorporated within a larger design. The megafunction is sold as a synchronous interface between a SDRAM and a generic local bus or as a bundled solution with an interface module (IFM).

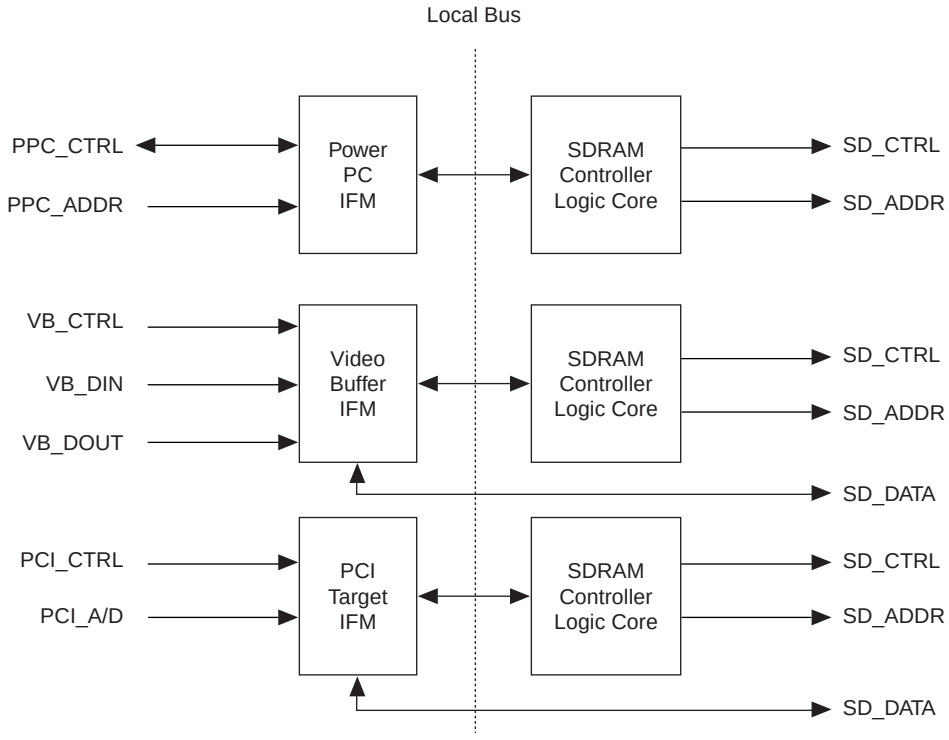
The first interface module forms an interface between a standard synchronous PowerPC 60×/750 series memory bus and the SDRAM controller's local bus. This version targets Altera® EPF10K200E-1 PLDs and has achieved 106 MHz internal operation with the Altera MAX+PLUS II version 9.2 software.

The second interface module is intended for high-speed video frame/field buffering applications. The module supports standard definition and high rates.

Block Diagram

Figure 26 shows the block diagram for the SDRAM controller megafunction.

Figure 26. SDRAM Controller Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50E	-1	2,041	5	66 MHz	IFM = PCI target

SDRAM Controller

Vendor: Eureka Technology
Target Application:
SDRAM memory system
Additional Deliverables:
Source code, testbenches and test vectors, top-level design template, documentation
ID Code: 2107-D520

- Supports industry-standard SDRAM and standard PC SDRAM DIMM
- Designed for PLD and ASIC implementations
- Efficient design to provide SDRAM access for different types of user devices
- Programmable memory size and SDRAM characteristics
- Supports zero-wait state burst data transfer to maximize data bandwidth
- Programmable burst length controlled by user
- Automatic refresh generation with programmable refresh intervals
- Designed for high-speed processor and DMA access to SDRAM
- Supports external data buffer between user device and SDRAM data bus
- Supports both registered and buffered PC SDRAM DIMM

General Description

The SDRAM controller megafunction interfaces between a processor or DMA device and SDRAM. It performs SDRAM read and write access based on processor or DMA requests.

SDRAM timing such as row and column latency, pre-charge timing, and row access length are automatically handled by the SDRAM controller. All timing parameters are set by the SDRAM controller on system reset and can be programmed by the user during run time to optimize system performance.

Zero-wait state data bursting is supported by the SDRAM controller to maximize data throughput. The back-end interface to user device such as a CPU or DMA controller is a standard microprocessor bus with wait-state control. It can be optimized easily to meet different application requirements.

This megafunction is available in AHDL, Verilog HDL, and VHDL as well as netlist format. Megafunction sizes vary with features and customization. Please contact Eureka Technology or visit their web site for a complete data sheet.

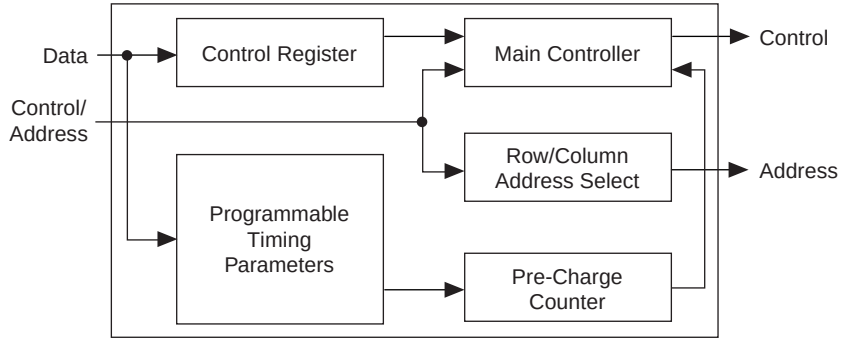
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 27 shows the block diagram for the SDRAM controller megafunction.

Figure 27. SDRAM Controller Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10K	–	400	0	75 MHz	Contact Eureka Technology
FLEX 6000	–	400	0	75 MHz	Contact Eureka Technology

SDRAM Controller

Vendor: Stargate Solutions
Target Application:
Buses and interfaces
ID Code: 6B8A-423C

- Fully synchronous design
- All signals are registered on the rising edge of the system clock
- Simple request/acknowledge interface to the application
- Standard interface to synchronous dynamic random access memory (SDRAM) side, compatible with typical SDRAMs
- Tracks SDRAM refreshes
- Option to power down the SDRAM for low-power applications

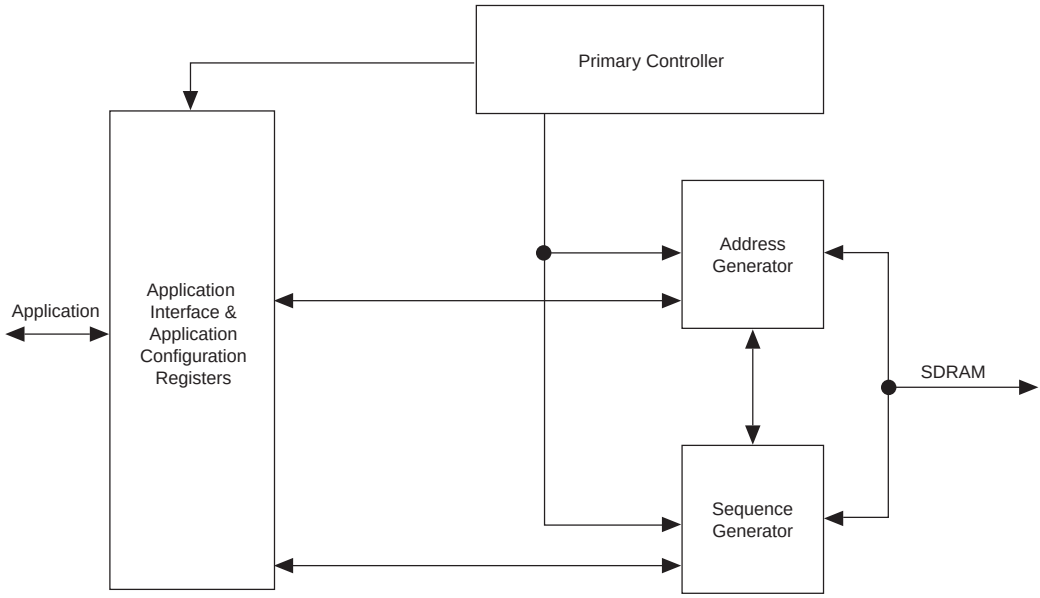
General Description

The SDRAM controller provides a simple request/handshake interface on the application side and a standard interface on the SDRAM side. The megafunction handles all SDRAM-related command generations and data transfers, including refresh generation. Thus, the megafunction hides all protocol-related complexities from the application.

Block Diagram

Figure 28 shows the block diagram for the SDRAM controller megafunction.

Figure 28. SDRAM Controller Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100E	-1	433	0	66 MHz	Contact Stargate Solutions

Multi-Function Memory Controller

Vendor: Eureka Technology
Target Application:
All memory systems
Additional Deliverables:
Source code, testbenches and test vectors, top-level design template, documentation
ID Code: 2107-MFMC

- Designed with synthesizable HDL for PLD and ASIC synthesis
- Supports multiple memory devices including SDRAM, DRAM, EDO, Flash EPROM, and ROM
- Highly programmable for different memory characteristics
- Dual-request port design to support host CPU and system bus requests
- One to four banks of DRAM/EDO with variable size
- Supports multiple banks of Flash EPROM with variable size
- Shared data path between memory devices to reduce pin count
- Error correction coding (ECC) with single-bit data correction
- Programmable page retention for DRAM
- Programmable memory configuration registers
- Programmable memory timing parameters
- Write buffer to support posted write from both ports
- Supports discrete SDRAM and PC-compatible SDRAM DIMM

General Description

The multi-function memory controller is designed for system memory control with the main memory consisting of SDRAM, DRAM, Flash EPROM, and ROM. The memory system is accessible from two ports. Typically, one port is used for the CPU and one is used for the secondary system bus such as the PCI bus.

The main data path is a 64-bit (72 bits including ECC) data bus which can be used by DRAM/EDO, Flash EPROM, or both. The memory controller is highly programmable such that the memory system can consist of any combination of DRAM/EDO, Flash EPROM or ROM, or all of the above.

The memory controller supports high-data bandwidth with burst data access, hidden pre-charge, and automatic refresh of DRAM/EDO.

ECC for single-bit error correction and double-bit error detection is provided by the memory controller. The memory controller performs read-modify-write to the memory to preserve ECC data integrity when less than 64-bit data is written.

System configuration and timing parameters are programmable by the system. A separate configuration port is included for this purpose.

This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with features and customization.

Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10K	–	*(1)*	*(1)*	50 MHz	Contact Eureka Technology
FLEX 6000	–	*(1)*	*(1)*	50 MHz	Contact Eureka Technology

Note:
(1) Logic cell and EAB numbers vary based on the number of memory banks supported.

DMA Controller

Vendor: CAST
Target Application: PCI-based or CPU-based systems
Additional Deliverables: VHDL RTL source code, testbench and test vectors, synthesis and simulation scripts
ID Code: 2AA5-C018

- Two independent fully programmed DMA channels
- Memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfers
- Single- or dual-address transfers, 8 or 16 transfers
- 16-bit data bus, 24-bit address bus
- Flexible request generation: Internal maximum rate or limited rate, external cycle steal or burst
- Two 16-bit transfer counters
- Operand packing and unpacking for dual-address transfers
- Supports all M68000 bus termination modes (DTACK, BERR, HALT)
- Provides full DMA handshake for burst and cycle steal transfers
- Allows M68000 devices to supersede DMA activity

General Description

The two-channel DMA controller megafunction is designed to complement the performance and architectural capabilities of the M68000 family of microprocessors by moving blocks of data in a quick, efficient manner with minimum intervention from a processor.

The bus interface of the DMA controller megafunction was designed in accordance with the M68000 bus specification.

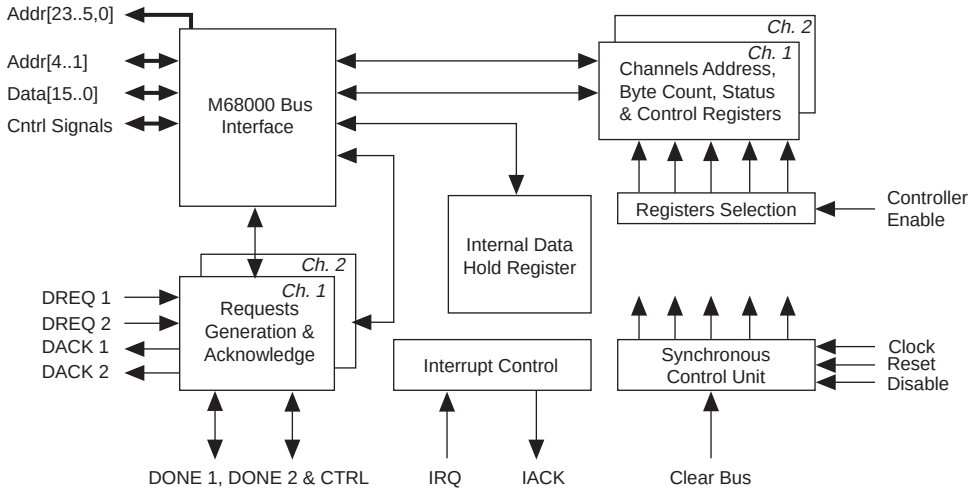
Modifiable Parameters

The DMA controller megafunction can be customized to include additional channels. Contact CAST for any required modifications.

Block Diagram

Figure 29 shows the block diagram for the DMA controller megafunction.

Figure 29. DMA Controller Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,353	0	24 MHz	2 channels
EPF10K30	-3	1,353	0	14 MHz	2 channels
EPF6024	-2	1,510	–	13 MHz	2 channels

DMA Controller

Vendor: Eureka Technology
Target Application: Embedded systems
Additional Deliverables: Source code, testbenches and test vectors, top-level design template, documentation
ID Code: 2107-0661

- General-purpose DMA controller
- Up to 16 DMA channels
- Supports both synchronous and asynchronous DMA transfers
- Designed for PCI and other CPU bus systems

General Description

The DMA controller megafunction is designed for data transfer in different system environments. Two module types—type 0 and type 1—are provided, and the user can choose the number of each module type. Type 0 modules are designed to transfer data residing on the same bus, and Type 1 modules are designed to transfer data between two different buses. Each module can support up to 4 DMA channels; the megafunction supports up to 16 total DMA channels.

Each DMA channel can be programmed for various features, such as transfer size, synchronized and unsynchronized transfer control, transfer priority, interrupt generation, memory and I/O address space, and address change direction. This megafunction is designed to work with 32-bit and 64-bit bus systems, including the PCI bus, PowerPC bus, and other CPU host buses. It can also be integrated with other megafunctions to form a complete functional block.

This megafunction is available in Altera Hardware Description Language (AHDL), Verilog HDL, VHDL, and netlist format.

Modifiable Parameters

Eureka Technology can customize the parameters shown in the following table according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

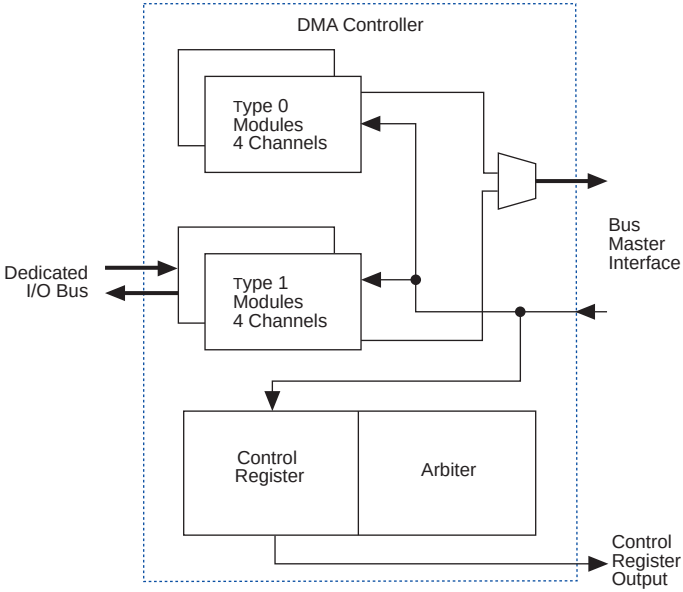
Modifiable Parameters

Parameter	Description
N	Number of channels
WIDTH	Width of the I/O bus

Block Diagram

Figure 30 shows the block diagram for the DMA controller megafunction.

Figure 30. DMA Controller Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	100	0	50 MHz	N = 1, WIDTH = 32 bits
EPF6016	-3	100	–	50 MHz	

PowerPC Bus Arbiter

Vendor: Eureka Technology
Target Application:
All PowerPC-based systems
Additional Deliverables:
Source code, testbenches and test vectors, top-level design template, documentation
ID Code: 2107-0300

- Compatible with all PowerPC bus architectures
- Manages up to 8 bus masters
- Supports address pipelining, address only transaction, address retry, and separate address and data bus tenure
- Fixed and rotating priority

General Description

The PowerPC bus arbiter megafunction arbitrates the PowerPC address and data buses to allow multiple bus masters or processors to co-exist on the host bus. The megafunction is designed for the PowerPC host bus and works with all PowerPC CPU families and embedded controllers. The megafunction can be used as a stand-alone function or it can be incorporated in the same device with the bus master or slaves. Both fixed and round-robin priority schemes can be implemented with the arbiter.

To maximize system performance, the megafunction supports advanced features of the PowerPC bus, such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and with feature changes. Contact Eureka Technology directly for an LE count that is based on user specifications.

Modifiable Parameters

Eureka Technology can customize the parameters shown in the following table according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

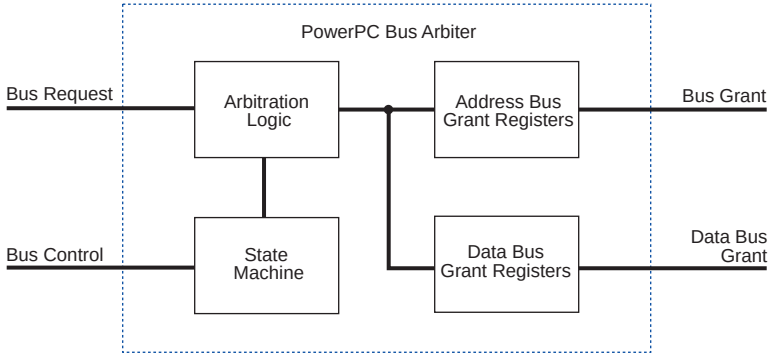
Modifiable Parameters

Parameter	Description
N	Number of ports: 4 or 8
AS	Architecture scheme: fixed priority, rotating priority, or user-specific priority
BP	Bus parking: highest priority or most recently used priority

Block Diagram

Figure 31 shows the block diagram for the PowerPC bus arbiter megafunction.

Figure 31. PowerPC Bus Arbiter Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	110	0	50 MHz	8 ports, fixed-priority architecture scheme, and highest-priority bus parking
EPF6016	-2	110	–	50 MHz	
EPM7128	-1	70	–	66 MHz	

PowerPC Bus Master

Vendor: Eureka Technology
Target Application:
All PowerPC-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training

- Compatible with all PowerPC bus architectures
- Interfaces with bus mastering or bus snooping devices such as DMA controllers
- Supports address pipelining and separate address and data tenure

General Description

The PowerPC bus master megafunction is a bus master that executes bus transactions on the PowerPC host bus. A simple and efficient user interface allows the user logic to reside directly on the PowerPC bus for high-performance data transfer. Together with the PowerPC bus slave, PowerPC bus arbiter, and PCI host bridge megafunctions, this megafunction provides the complete system function logic function of a PowerPC-based system.

To maximize system performance, the PowerPC bus master megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. This megafunction also supports both single beat and burst data transfers, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and with feature changes. Contact Eureka Technology directly for a logic cell count that is based on user specifications.

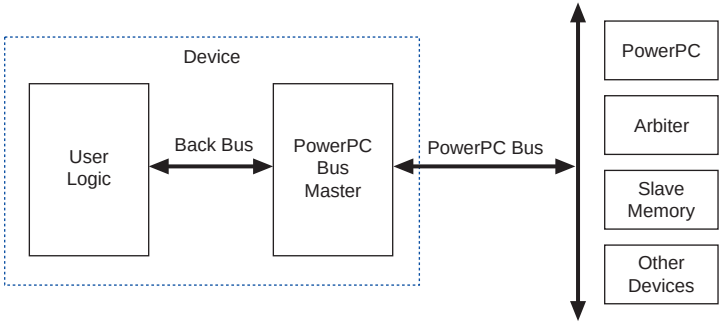
Modifiable Parameters

Eureka Technology can customize the megafunction according to specific user requirements, such as adding pipelining or using either snoop-only or regular data transfer. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 32 shows the block diagram for the PowerPC bus master megafunction.

Figure 32. PowerPC Bus Master Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	160	0	50 MHz	160: With snoop only and pipelining 320: With regular data transfer and pipelining
EPF6016	-2	160	–	50 MHz	
EPM7128	-7	80	–	66 MHz	Contact Eureka Technology

PowerPC Bus Slave

Vendor: Eureka Technology
Target Application:
All PowerPC-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 1207-0108

- Compatible with all PowerPC bus architectures
- Interfaces with SRAM, SBRAM, FLASH, and user local buses
- Supports data bursting with standard asynchronous SRAM
- Supports address pipelining and separate address and data tenure

General Description

The PowerPC bus slave megafunction is a multi-function interface between the PowerPC bus and user devices such as asynchronous SRAM, synchronous burst SRAM, FLASH, and user local buses. Together with the PowerPC bus master, PowerPC bus arbiter, and PCI host bridge megafunctions, this megafunction provides the complete system function logic function of a PowerPC-based system.

To maximize system performance, the megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction also supports both single beat and burst data transfer, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and feature changes. Contact Eureka Technology for a logic cell count that is based on user specifications.

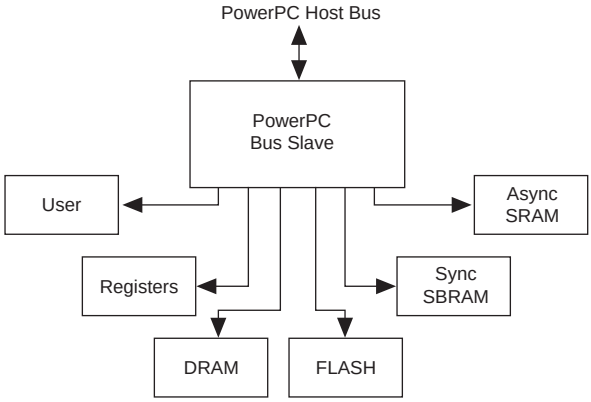
Modifiable Parameters

Eureka Technology can customize the megafunction according to specific user requirements, such as 32- or 64-bit data, pipelining, type of back-end device, adren mapping, and amount of memory mapped by the slave. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 33 shows the block diagram for the PowerPC bus slave megafunction.

Figure 33. PowerPC Bus Slave Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	170	0	50 MHz	32-bit data, pipelined, back-end burst, and two memory spaces
EPF6016	-2	170	–	50 MHz	

PowerPC to PCI Host Bridge

Vendor: Eureka Technology
Target Application:
All PowerPC-based systems
Additional Deliverables:
Source code, testbenches and test vectors, top-level design templates, documentation
ID Code: 2107-D430

- Compliant with ***PCI Local Bus Specification, Revision 2.2***
- Designed for PLD and ASIC implementations in various system environments
- Interface directly with a PowerPC microprocessor
- Combined host bridge, bus master, and bus target functions in one megafunction
- 32-bit bus master and target support
- Supports burst transfer to maximize memory bandwidth
- Zero-wait state PCI data transfer
- Supports target retry, disconnect, and target abort
- Automatic transfer restart on target retry and disconnect
- Concurrent bus master and target function
- Generate standard peripheral component interconnect (PCI) type 0 and type 1 configuration access
- High-speed bus request and arbitration
- Supports all PCI-specific configuration registers

General Description

The PowerPC to PCI Host Bridge is a bus interface unit designed for efficient interface between the PowerPC microprocessor and the PCI bus. It contains the functions of a bus master, bus target, and the ability to initiate configuration access all in one megafunction. It performs all the data transfer functions necessary for the PowerPC CPU to access data on the PCI bus. It supports burst data transfer to maximize data bandwidth. The target function allows other PCI masters to access system resources on the CPU local bus. It supports high-speed bus request and arbitration to minimize transfer latency.

Single and burst data transfer are supported both as bus master and bus target. All data transfers on the PCI bus can be accessed through the CPU local bus. Many design options are possible on the host bridge.

This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with features and customization. Eureka Technology can customize the design according to specific user requirements.

Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Typical modification includes:

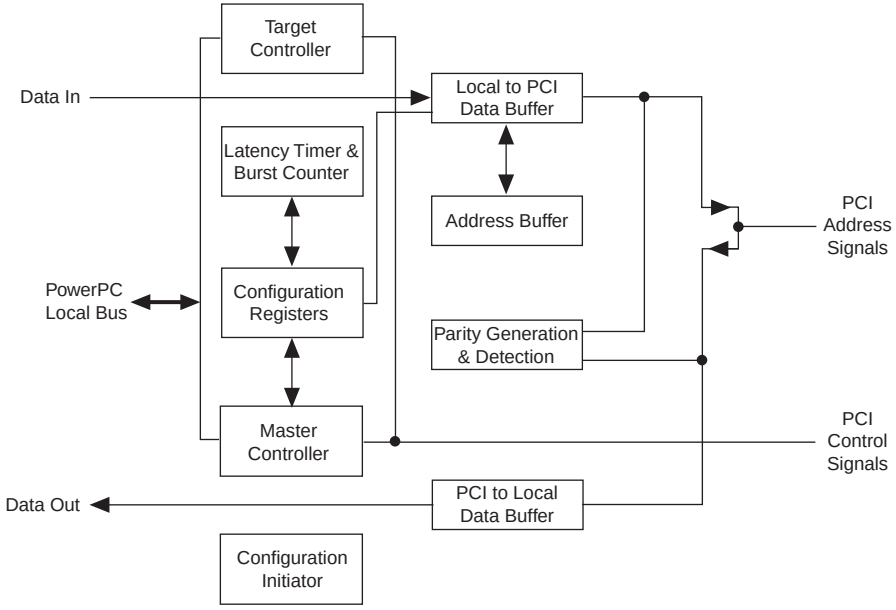
- 2× clock on PowerPC bus
- Asynchronous PowerPC and PCI clock
- 64-bit PCI bus
- 32-bit PowerPC bus

Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 34 shows the block diagram for the PowerPC to PCI host bridge megafunction.

Figure 34. PowerPC to PCI Host Bridge Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
FLEX 10K	–	1,000	0	33 MHz	Contact Eureka Technology
FLEX 6000	–	1,000	0	33 MHz	Contact Eureka Technology

Counter/Timer

Vendor: Innocor
Target Application:
Event counters, programmable square wave, software timing
Additional Deliverables:
User manual, simulation files
ID Code:
5931

- 16-bit counter/timer
- Selectable outputs: pulse, one shot, and square wave
- Edge-triggered hardware or software start
- Optional restart on re-trigger
- Gate input to hold current count value
- Single or continuous count down

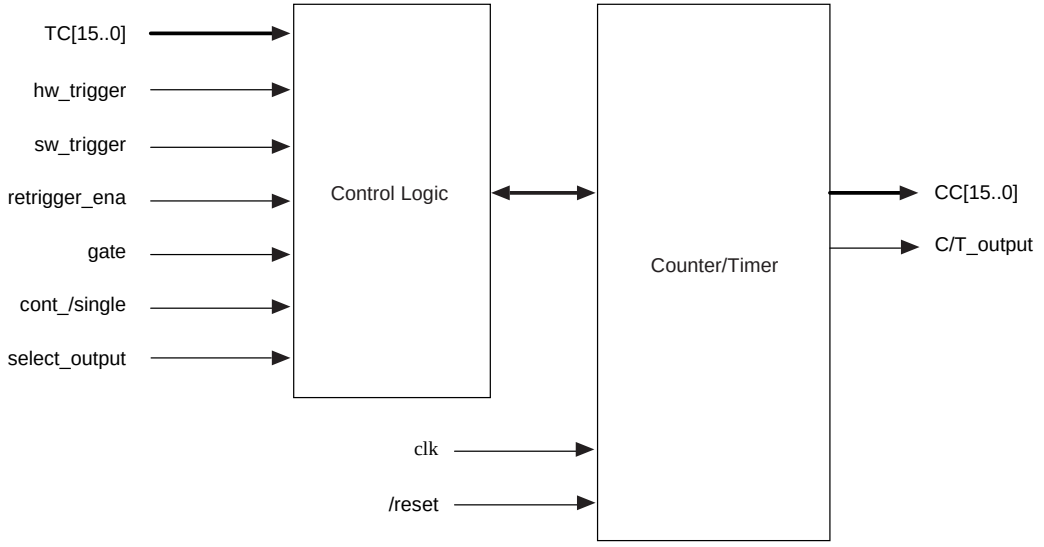
General Description

The counter/timer megafunction provides a selectable down-count output. It can be used to accurately give time delays for software, as well as any other microcomputer timing applications. The counter–timer megafunction can easily be scaled to higher count values by routing the output of one instance of the megafunction back into another instance.

Block Diagram

Figure 35 shows the block diagram of the counter-timer megafunction.

Figure 35. Counter-Timer Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	88	0	66 MHz	Contact Innocor
EPF6010A	-2	88	0	37 MHz	Contact Innocor

a16450p Universal Asynchronous Receiver/Transmitter

Vendor: Altera
Target Application: Serial data communications applications, modem interface
Additional Deliverables: a16450 Universal Asynchronous Receiver/Transmitter Data Sheet
Ordering Code: PLSM-16450

MegaCore™

- a16450p MegaCore function implementing a universal asynchronous receiver/transmitter (UART)
- Optimized for APEX, FLEX, and MAX architectures
- Programmable word length, stop bits, and parity
- Full duplex operation
- Programmable baud rate generator
- Prioritized interrupt control
- Internal diagnostic/loopback capabilities
- Functionally based on the National Semiconductor Corporation NS16450 device

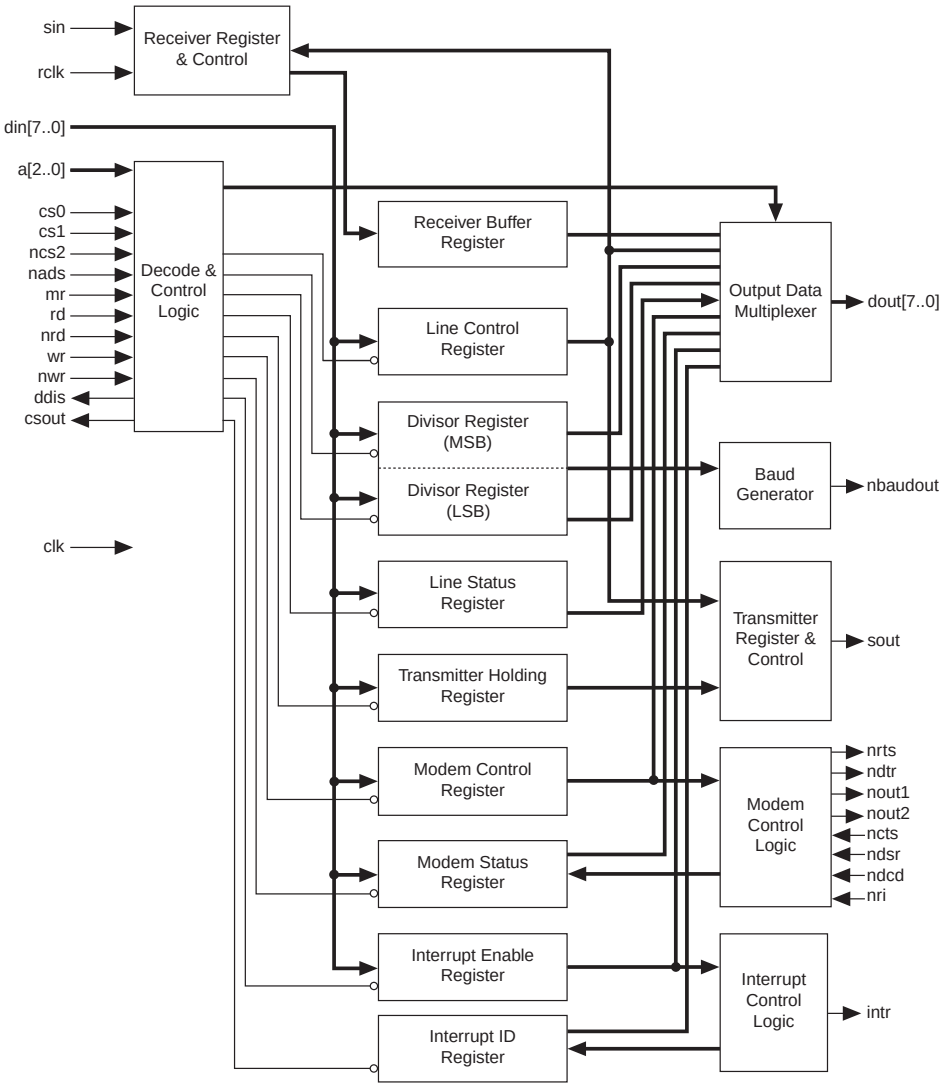
General Description

The a16450p MegaCore function implements a UART, which provides an interface between a microprocessor and a serial communications channel. The a16450p receives and transmits data in a variety of configurations, including 5-, 6-, 7-, or 8-bit data words; odd, even, or no parity; and 1, 1.5, or 2 stop bits. The a16450p includes an internal baud rate generator and interrupt control.

Block Diagram

Figure 36 shows the block diagram for the a16450p UART megafunction.

Figure 36. a16450p UART Block Diagram



For more information, see the *a16450 Universal Asynchronous Receiver/Transmitter Data Sheet*.

16450 UART

Vendor: CAST
Target Application: Serial data communications applications, modem interface
Additional Deliverables: VHDL testbench, VHDL model, user guide
ID Code: 2AA5-C011

- Full double buffering
- Independently controlled transmit, line status, receive, and data set interrupts
- Programmable data word length (5 to 8 bits), parity, and stop bits
- Parity, overrun, and framing error checking
- Supports transmission rates up to 1.5 Mbps
- Programmable baud rate generator allows division of any reference clock by 1 to ($2^{16} - 1$) and generates an internal 16× clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions

General Description

The `16450` programmable UART megafunction provides data formatting and control to a serial communications channel.

The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

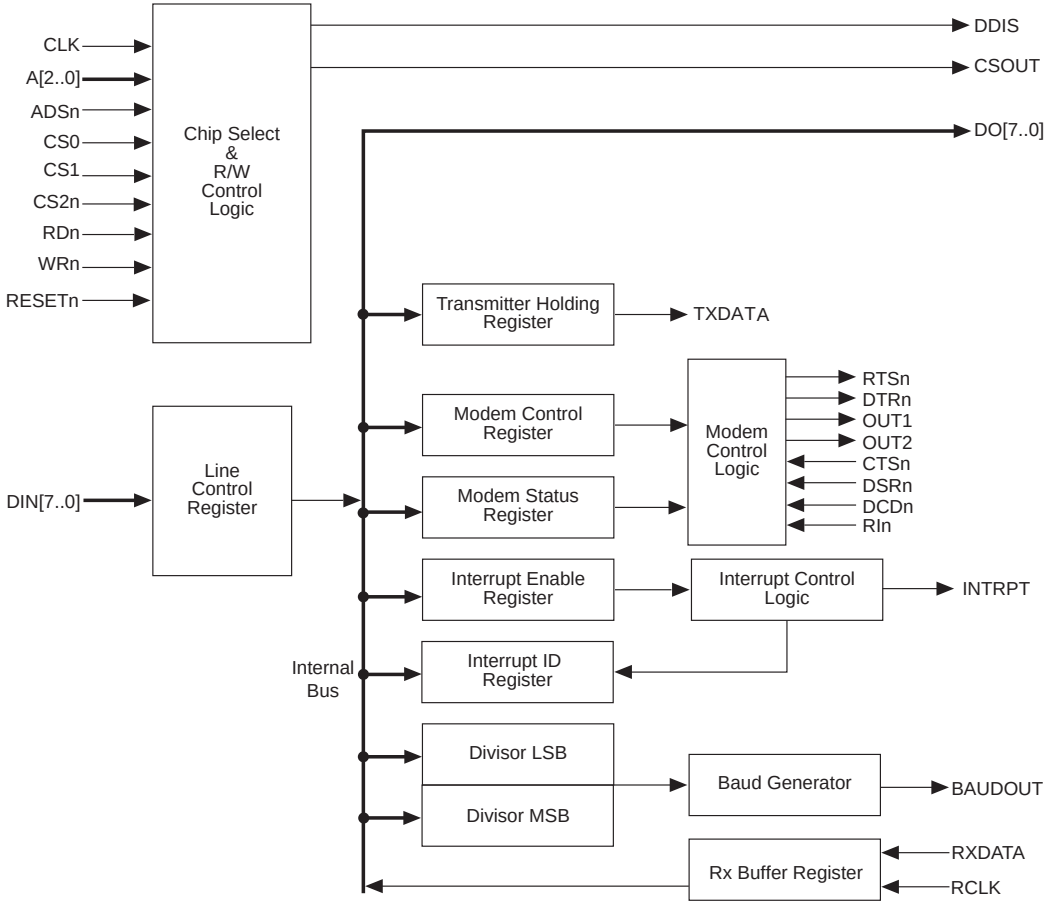
Modifiable Parameters

The `16450` megafunction can be customized to include a different CPU interface and to remove the internal baud rate generator.

Block Diagram

Figure 37 shows the block diagram for the `16450` UART megafunction.

Figure 37. 16450 UART Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPM9320	-15	284	–	26 MHz	Contact CAST
EPF6016	-2	388	–	32 MHz	Contact CAST
EPF8636	-3	382	–	25 MHz	Contact CAST
EPF10K10	-3	358	–	38 MHz	Contact CAST
EPF10K30A	-1	358	–	58 MHz	Contact CAST

16550 UART

Vendor: CAST
Target Application: Serial data communications, modem interface
Additional Deliverables: VHDL testbench, VHDL model
ID Code: 2AA5-C010

- Capable of running with all existing 16450 and 16550A software
- Asynchronous operation
- In first-in-first-out (FIFO) mode, the transmitter and receiver are each buffered with 16-byte FIFO buffers to reduce the number of CPU interrupts
- Programmable data word length (5 to 8 bits), parity, and stop bits
- Parity, overrun, and framing error checking
- Supports transmission rates up to 1.5 Mbps
- Programmable baud rate generator allows division of any reference clock by 1 to ($2^{16} - 1$) and generates an internal 16× clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions

General Description

The `16550` UART megafunction provides data formatting and control to a serial communications channel.

The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

Modifiable Parameters

The `16550` megafunction can be customized to include:

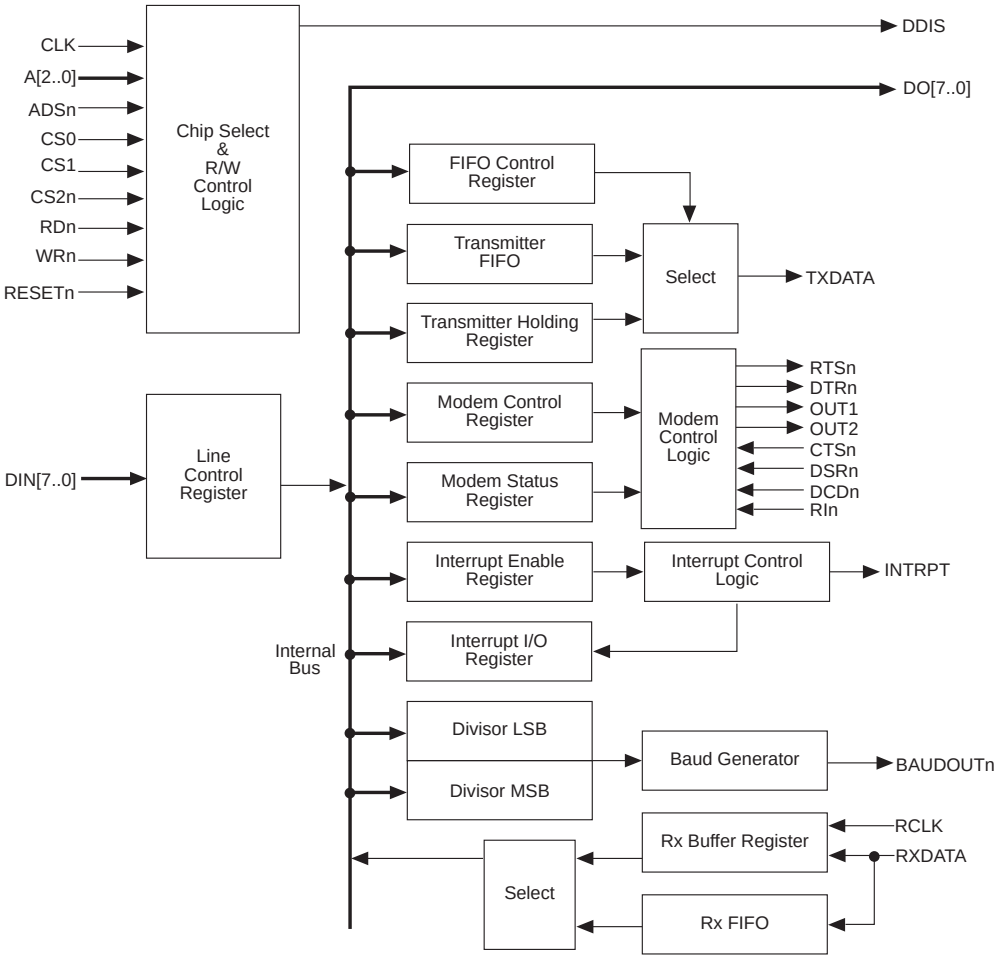
- Different FIFO sizes (separately for transmitter and receiver)
- Removal of internal baud rate generator
- Different CPU interface

Contact CAST directly for any required modifications.

Block Diagrams

Figure 38 shows the block diagram for the `16550` UART megafunction.

Figure 38. 16550 UART Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-1	1,079	–	25 MHz	Contact CAST
EPF10K30A	-1	1,079	–	35 MHz	Contact CAST
EPF10K30E	-1	656	2	47 MHz	Contact CAST
EPF10K100B	-1	1,079	–	40 MHz	Contact CAST

6850 ACIA

Vendor: CAST
Target Application:
Serial data communications applications, modem interface
Additional Deliverables:
VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C005

- Programmable data word length, parity, and stop bits
- Parity, overrun, and framing error checking instructions and counting loop interactions
- Supports transmission rates over the 1.0 Mbps specification
- False start bit deletion
- Peripheral modem control functions
- Developed in VHDL and synthesizes to approximately 1,100 gates
- Functionally based on the Motorola MC6850

General Description

The 6850 asynchronous communications interface adapter (ACIA) megafunction provides data formatting and control to the asynchronous data communications of data bus systems.

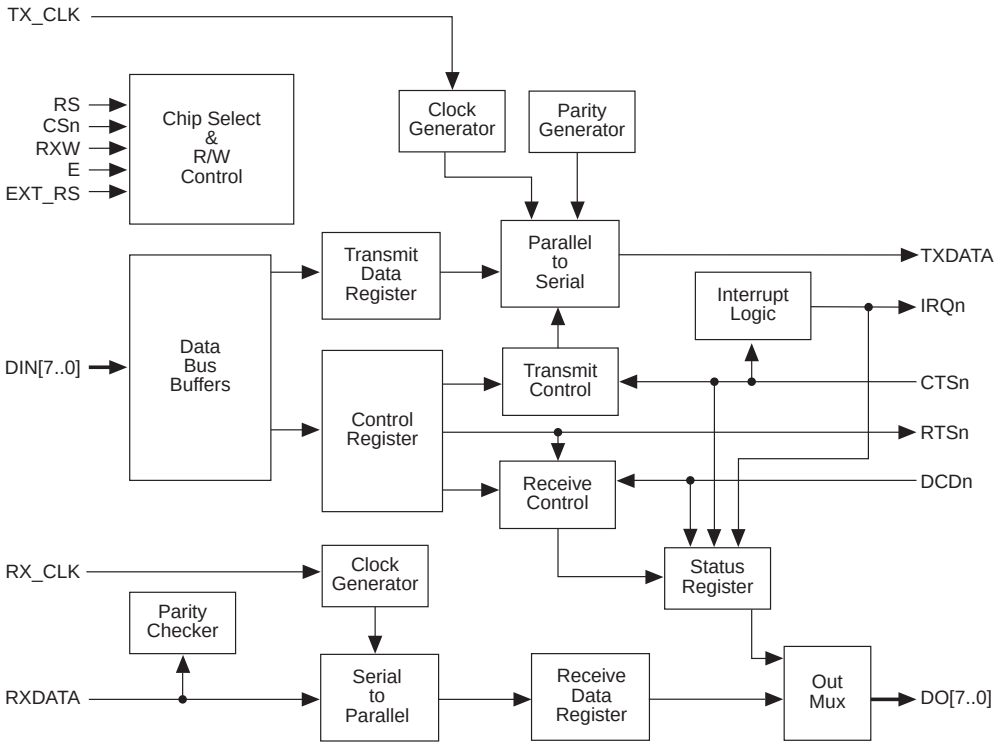
The megafunction has select, enable, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data.

In addition, a programmable control register provides the megafunction with a transmit control, a receive control, an interrupt control, variable word lengths, and clock division ratios. Three control lines are provided for peripheral or modem operation.

Block Diagram

Figure 39 shows the block diagram for the 6850 ACIA megafunction.

Figure 39. 6850 ACIA Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	185	–	37 MHz	Contact CAST
EPF10K10A	-1	185	–	54 MHz	Contact CAST
EPM9320	-15	153	–	29 MHz	Contact CAST
EPF8282	-2	185	–	25 MHz	Contact CAST
EPM7160	-10	118	–	29 MHz	Contact CAST
EPF6016	-2	185	–	38 MHz	Contact CAST

UART

Vendor: CAST
Target Application: Serial data communications applications
Additional Deliverables: VHDL testbench
ID Code: 2AA5-C004

- 8-bit characters
- (T × C)/(R × C) 16 times the desired output baud rate
- One start bit and one stop bit
- Polling and interrupt modes
- Flexibility for adding other features
- Developed in VHDL

General Description

The UART megafunction is a generic UART that can be used to implement a peripheral data communication device. The designer can program the megafunction with an 8-bit CPU.

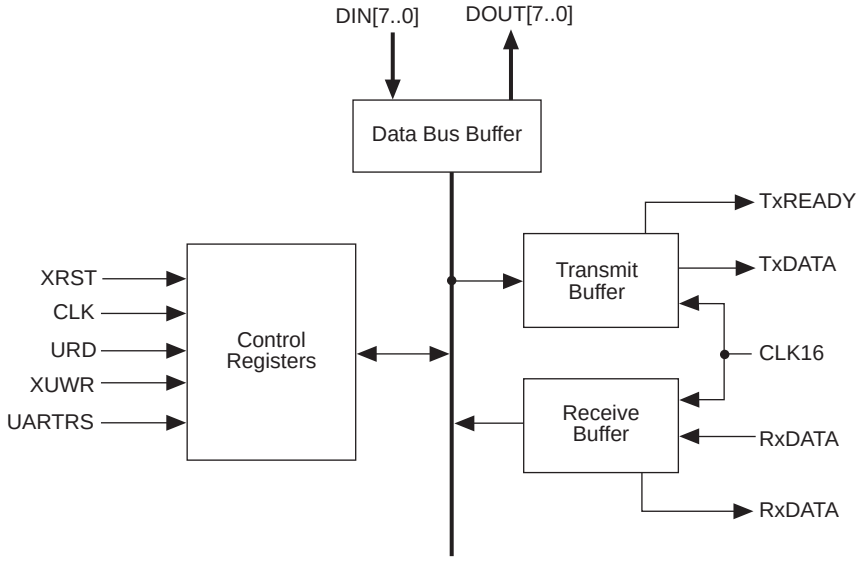
Modifiable Parameters

CAST can modify the megafunction's character length, parity, and number of start and stop bits to meet user specifications.

Block Diagram

Figure 40 shows the block diagram for the UART megafunction.

Figure 40. UART Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	87	–	84 MHz	Contact CAST
EPF10K10A	-1	87	–	172 MHz	Contact CAST
EPM9320	-15	68	–	40 MHz	Contact CAST
EPF8282	-2	96	–	67 MHz	Contact CAST
EPM7096	-7	68	–	62 MHz	Contact CAST
EPF6016	-2	112	–	76 MHz	Contact CAST

Processor & Peripheral Design Services (ACAP Partners)

The following table lists ACAP partners who offer design services for processors and peripherals.

Partner	Expertise				Services					
	Embedded Processors	RISC-Based Architecture	Microcontrollers	Peripherals/UARTS	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
Advanced Logical Design, Inc. 12280 Saratoga-Sunnyvale Rd. Suite 201 Saratoga, CA 95070 Tel. (408) 446-1004	✓	✓	✓	✓				✓	✓	✓
Applied Computing Technology, Inc. 1020F Commerce Park Drive Oak Ridge, TN 37830 Tel. (423) 220-0777	✓	✓	✓	✓	✓	✓	✓	✓	✓	
Applied Microelectronics Inc. 1046 Barrington Street, Halifax Nova Scotia, Canada, B3H 2R1 Tel. (902) 421-1250					✓	✓	✓	✓	✓	✓
BARCO SILEX Rue du Bosquet 7 1348 Louvain La Neuve Belgium Tel. (32) 10-45 49 04	✓	✓	✓	✓	✓	✓				
Coded Solutions Pty Ltd 65 Johnston Street Annandale, NSW 2038 Australia Tel. (61) 2 9518 7011	✓	✓	✓	✓			✓	✓	✓	
Digital Design Solutions 6696 Fossil Creek Dr. Memphis, TN 38120 Tel. (901) 759-1802	✓		✓	✓				✓	✓	✓

Partner	Expertise				Services					
	Embedded Processors	RISC-Based Architecture	Microcontrollers	Peripherals/UARTS	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
DMC Manufacturing, Inc. 7025 Central Highway Pennsauken, NJ 08109 Tel. (609) 665-5400								✓	✓	✓
Eberwein & Associates, Inc. 9449 Briar Forest, #507 Houston, TX 77063 Tel. (713)-784-1226	✓	✓	✓	✓			✓	✓	✓	✓
Innovative Configuration, Inc. (ICI) 712 via Palo Alto Aptos, CA 95003 Tel. (831) 688-6917	✓	✓	✓		✓			✓	✓	
I/O Consulting A/S Gaaseagervej 6 DK-8250 Egaa Tel. (45) 87 43 80 74	✓				✓	✓	✓	✓	✓	
Lewis Innovative Technologies, Inc. 11405 Alabama Highway 33 (P.O. Box 624) Moulton, AL 35650 Tel. (256) 974-8931				✓				✓	✓	
Mettrix Technology Corporation 25 Corporate Park Drive, Suite C Hopewell Junction, NY 12533 Tel. (914) 897-4960	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Northwest Logic Design, Inc. 1905 NW 169th Place, Suite 121 Beaverton, OR 97006 Tel. (503) 533-5800	✓	✓	✓	✓	✓		✓	✓	✓	
Nova Electronic Design and Analysis Corporation 459B Carlisle Drive Herndon, VA 20170 Tel. (703) 618-2877	✓	✓	✓	✓				✓	✓	✓

Partner	Expertise				Services					
	Embedded Processors	RISC-Based Architecture	Microcontrollers	Peripherals/UARTS	IP Integration	ASIC Conversion	Software Development	Board Design	Prototype Development	Board Products
RPA Electronics Design, LLC 1285 Chenango Street Binghamton, NY 13901 Tel. (607) 771-0393	✓	✓	✓	✓			✓	✓	✓	✓
RTI 10560 Main St., Ste. 417 Fairfax, VA Web. **http://www.rti-world.com** Tel. (703) 293-9662	✓	✓	✓	✓		✓	✓		✓	
Szabo Electronic Systems 40 Purvis Street Watertown, MA 02472 Tel. (617) 924-0618	✓	✓	✓	✓			✓	✓	✓	✓
Vulcan ASIC Ltd., Unit 6, The Maltings, Royston, Herts, SG8 5DY, England Tel. (44) 0 1763 248163	✓	✓	✓	✓	✓	✓	✓		✓	
Tantau Australia P.O. Box1232, Lave Cove 1595 Sydney, Australia Tel. (61) 02 9555 9375	✓		✓	✓			✓	✓	✓	✓

Development Boards

September 1999

Overview

To support the development and verification of System-on-a-Programmable-Chip™ designs, Altera and its partners have made a variety of development and prototyping boards available. The various boards accommodate system design by allowing application software development to begin earlier in the design flow. Also, hardware designers can verify intellectual property (IP) functionality quickly and effectively. Table 1 lists the development boards offered by Altera Corporation, Altera Megafunction Partners Program (AMPP℠) partners, and Altera Consultants Alliance Program (ACAP℠) partners.

Table 1. Development Boards Available

Vendor	Partner Program	Board Name	Application	Target Device Family
Altera Corporation	–	FLEX® 10KE PCI development board	PCI	FLEX 10K
Gid'el Limited	ACAP	PROC10K	Prototyping	FLEX 10K
Nova Engineering	AMPP	Constellation	Prototyping	FLEX 10K
PLD Applications	Premiere AMPP	CPCI_GEN10K	PCI	FLEX 10K
		PCI_GEN10K		
		PCI_GEN6K		FLEX 6000
Tensilica	AMPP	XT-1000	Prototyping	FLEX 10K
Princeton Technology Group	ACAP	Megalogic System 100	Prototyping	FLEX 10K

Contents

The development boards section contains the following functions:

Altera

FLEX 10KE PCI Development Board 325

Gid'El Limited

PROC Prototype Boards 327

Nova Engineering

Constellation Prototype Board 333

PLD Applications

CPCI10K-PROD Prototyping Board 336
PCI_GEN10K Prototype Board 338
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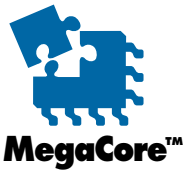
Princeton Technology Group

Megalogic System 100 Development Board 343

FLEX 10KE PCI Development Board

Vendor: Altera
Target Application:
PCI
Ordering Code:
PCI-BOARD2



- Universal 64-bit, 66-MHz peripheral component interconnect (PCI) expansion card
- Includes the FLEX 10KE EPF10K100EFC484-1 device
- On-board 144-pin small outline DIMM 32-Mbyte SDRAM module
- On-board standard PCI Mezzanine card (PMC) connector
- I/O prototype area
- RS-232 port
- On-board voltage regulator automatically generates 2.5 V and 3.3 V from a 5.0-V power supply
- Flexible clocking options for the local-side logic, including PCI clock, on-board crystal oscillator, or external clock input
- Supports in-circuit reconfigurability (ICR) with an EPC2 configuration device and a MasterBlaster™, ByteBlasterMV™, ByteBlaster™, or BitBlaster™ download cable. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable.)
- Designed to accept the following devices:
  - EPF10K30EFC484
  - EPF10K50EFC484
  - EPF10K50SFC484
  - EPF10K100EFC484
  - EPF10K130EFC484
  - EPF10K130EFC672
  - EPF10K200EFC672
  - EPF10K200SFC672

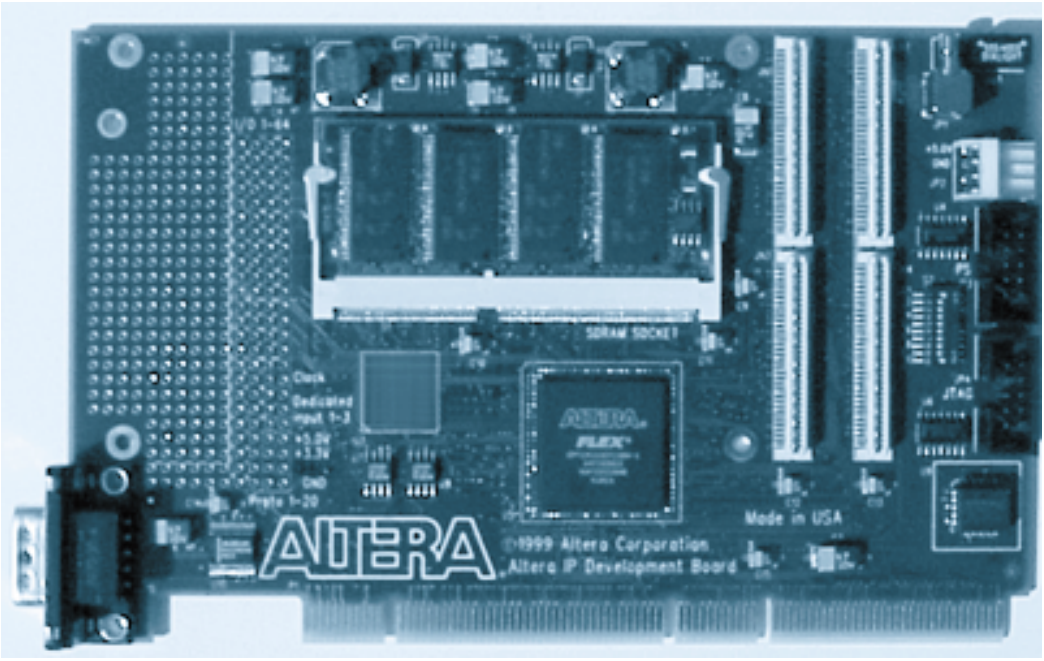
General Description

The PCI development board works with all Altera PCI MegaCore™ functions, including `pci_a`, `pci_b`, `pci_c`, and `pcit1` (a back-end reference design for each megafunction is required). Users can implement custom local-side functions to interface the Altera PCI MegaCore function with the on-board SDRAM socket, the on-board PMC connector, the RS-232 port, or any custom logic implemented in the prototype area or PMC. The PCI development board provides a flexible clock network distribution and in-circuit configuration options. It supports a wide range of FLEX 10KE devices so users can tailor the development board to meet I/O pin and area requirements.

Development Board

Figure 1 shows the FLEX 10KE PCI development board.

Figure 1. FLEX 10KE PCI Development Board



☞ For more information, refer to the *FLEX 10KE PCI Development Board Data Sheet*.

PROC Prototype Boards

Vendor: Gid'el Limited
Target Application: Prototyping, ASIC emulation, algorithm development, DSP, imaging, image recognition, networking, communications, 33-bit/33-MHz PCI

- Variable clock up to 100 MHz
- User application-specific integrated circuit (ASIC)/programmable logic device (PLD) design using 20,000 to 2 million gates
- Dozens of Giga operations per second (GOPS)
- Up to 80 Gbytes/second access to dual-port RAM blocks
- 16 to 128 Mbytes SDRAM
- 0 to 1 Mbytes pipelined SRAM with up to 400 Mbytes/second access
- Over 250 logic probes with quick hooks
- Connection to Mezzanine board
- Connection to other boards

Altera Devices on Board

Table 2 lists the Altera devices on the PROC20K and PROC10K prototype boards.

Table 2. Altera Devices On Board

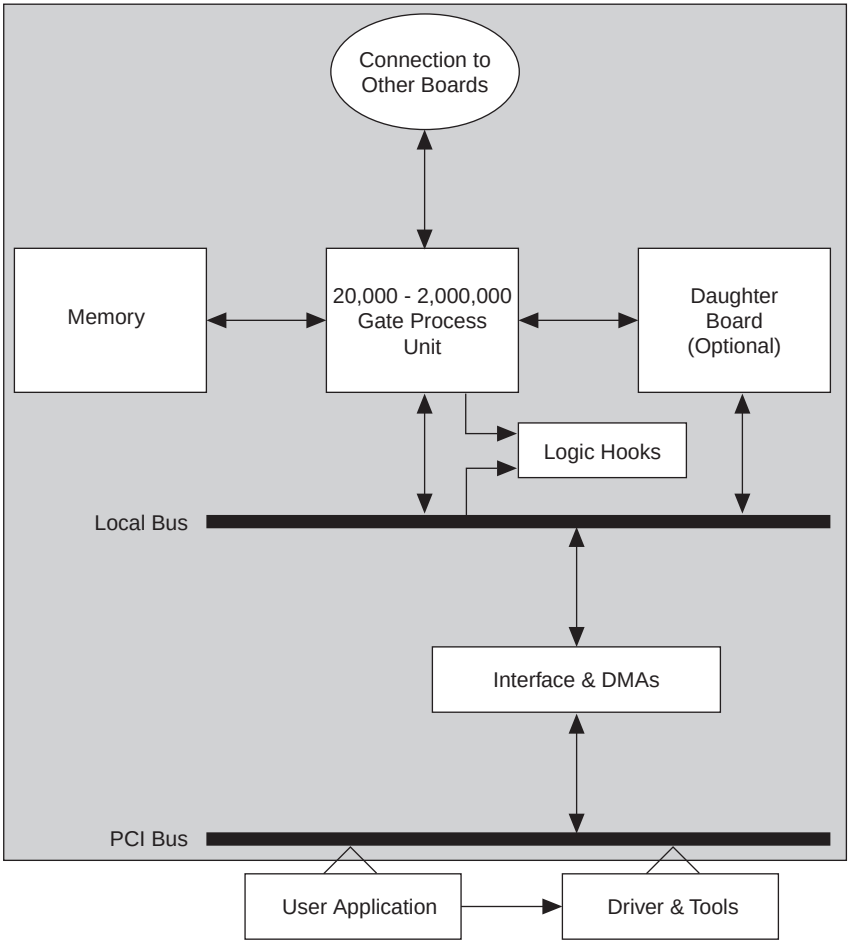
Board Model	Altera Device
PROC20K-1 (7 Altera devices on board)	EPM7128A, EP20K400
PROC20K-2 (2 Altera devices on board)	EPM7128A, EP20K400
PROC20K-5 (5 Altera devices on board)	EPM7128A, EP20K400
PROC10K-1 (7 Altera devices on board)	EPM7128A, EPF10K50E
PROC10K-5 (5 Altera devices on board)	EPM7128A, EPF10K50E
PROC10K-2F (2 Altera devices on board)	EPM7128A, EPF10K130E
PROC10K-F (5 Altera devices on board)	EPM7128A, EPF10K130E

General Description

The PROC prototype board series is a general-purpose hardware development platform based on Gid'el's experience as an outsource supplier for complex hardware accelerators. The PROC boards contain the hardware acceleration, PCI, and other standard connectivity typically used for prototyping. If needed, a daughter board with the user's specific needs may be added (e.g., Low-Voltage Differential Signaling (LVDS) I/O, video DAC, and RF front-end extension).

Figure 2 shows the PROC boards block diagram.

Figure 2. PROC Boards Block Diagram



Functional Description

PROC cards consist of three main components:

- Processing unit
- Memory blocks
- Connectors for testing and other cards

Processing Unit

The processing unit is the heart of the system. The function of this unit, together with external memory, is to write user algorithms. The unit is composed of one or more reconfigurable PLDs that include logic and wide bandwidth dual-port RAM. Memory can be implemented as dual-port RAM, look-up table (LUT) logic, line delay for action on matrices, first-in-first-out (FIFO) buffers, and stacks.

The PLD contents are automatically loaded from the hard disk, making it possible to change the functionality of the processing unit as often as needed.

Clock System of the Processing Unit

The clock system consists of the following three clocks:

- The main clock is a programmable clock with speeds up to 50 MHz in the PROC20K board and up to 100 MHz in the PROC10K board. The appropriate frequency can be chosen for each application.
- A local bus clock (synchronized to the main clock) that connects the PCI to the logic components.
- A clock (portion of the main clock) that is used for work at relatively low frequencies. Optionally, all the logic components can use the same external clock. Data that arrives from an outside source can be received with a synchronized external clock and can be synchronized with the system by internal FIFO buffers.

Memory

The memory subsystem consists of on-chip memory and off-chip memory, including dual-port RAM, synchronous SRAM for high-speed random accesses, and SDRAM. Also, on PROC cards—in addition to dual-port RAM in the logic components—there are synchronous SRAM and SDRAM components.

Currently, the memory for SDRAM can be up to 128 Mbytes. When divided into four sections, each section can be activated separately. The total width of all SDRAM memory buses is 128 bits for the PROC20K board and 64 bits for the PROC10K board. Designers can create a wider bus logic band through time multiplexing.

SRAM is another memory block with fast random access. It has two memory units of 128K × 16 with two additional attached buses. If needed, designers can order a special model with more memory.

Connectors

The PROC20K board contains hundreds of connections between the different logic units, while the PROC10K board contains approximately 40 connections between different logic units. In addition, over 200 pins allow connection to a logic analyzer, a daughter adapter card, and/or other cards. The PROC boards provide a voltage of 2.5 V, 3.3 V, 5.0 V, +72 V, or –72 V to daughter boards that are connected together with the local bus.

The PROC boards are 32-bit, 33-MHz PCI cards. After initialization, a PCI-memory address space is allocated for the board's memory and registers. Direct access to all logic components is possible from the PCI via the board's bridge, and access to memory is possible through the logic components.

There are LEDs that can be set to indicate various states, depending on the user configuration.

Additional Support Features

The PROC boards come with the following support features:

- Automatic generation of a hardware/software interface
- Automatic loading of configurable logic from the disk
- Debugging tool
- SDRAM controller megafunction
- Additional megafunctions
- Support provided up to turnkey project

Automatic Code Production

Code production can be divided into three parts:

- Documentation—The production of a well organized, detailed document that describes the aspects of implementing the user application over the PROC board.
- Software—A class representing the application over the PROC card. There is fast access to all registers and memory that were defined by the user according to the specific application. Memory, registers, and all other specifications are data members of the class. Closing the open class and opening a new class executes the exchange of the PROC implementation logic. When the configuration of the PROC card is changed, the program is not able to access previous registers and memory.
- Hardware description language (HDL)—The production of HDL files that contain all of the mode register's logic, memory selects, and status reads. For easy use, there is a file per device.

SDRAM Controller

The controller receives an address and select, and generates all of the control signals. The controller is built for optimum operation at the working frequency. This function works through either single access or burst access. Burst mode is not restricted to page size.

In this framework, the controller also produces refresh cycles; the controller performs refreshes during periods of inactivity.

Debugging Tools

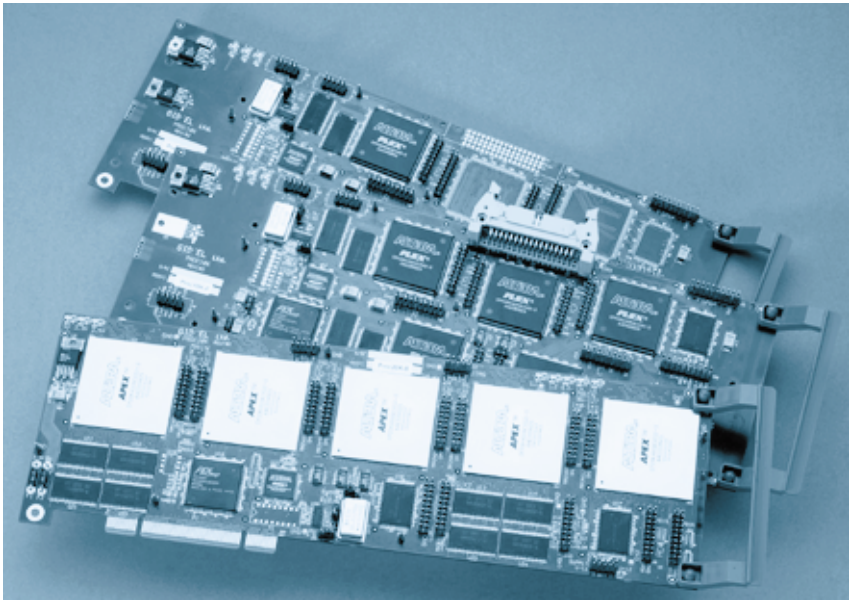
The easy-to-use debugging tools allow the programmer direct access to the PROC board implementation memory and registers. Using the debugger, the programmer can access the memory and registers by name and does not have to remember details such as the address registers. In addition, the designer can record a series of activities and activate them at a later stage. The designer can write a program without the need for writing software.

☞ For more information, contact Gid'el at **w_reuven@gidel.co.il.**

Prototype Board

Figure 3 shows the PROC prototype boards.

Figure 3. PROC Prototype Boards



Constellation Prototype Board

Vendor: Nova Engineering
Target Application: Prototyping, DSP

- Modular architecture and flexible design for rapid prototyping
- PC/104 form factor supports stand-alone or embedded operation
- Accommodates 3.3-V to 5.0-V EPF10K20 to EPF10K100 devices
- Configuration options include EPROM, ISA Bus, Joint Test Action Group (JTAG)
- ISA-compatible for reconfigurable computing and accelerators

Altera Devices on Board

- FLEX 10K, FLEX 10KA, and FLEX 10KE devices

General Description

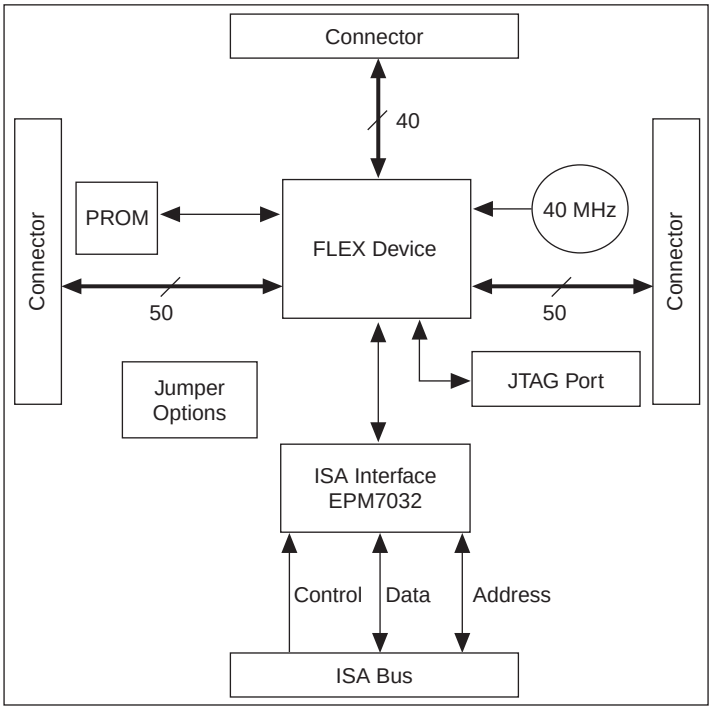
Constellation is Nova Engineering's PLD-based, hardware development system with a modular architecture that can be easily molded into virtually any prototype configuration.

Constellation is a powerful hardware development system that delivers the flexibility and ease of use necessary for rapid prototype development. It is a low cost, off-the-shelf product that provides support for a wide range of Altera's FLEX 10K devices, including 3.3-V and 5.0-V parts. The FLEX 10K prototype board can operate in a stand-alone configuration, or it can be easily expanded to include additional PLDs and analog subsystems. Modular interconnects provide plug-n-play access to high speed A/D and D/A converters, creating a base development system for communication, signal processing, data acquisition, control, automatic test equipment (ATE), and graphics products.

Constellation products are fabricated in the industry standard, compact PC/104 form factor. The system is fully compatible with the ISA standard and can be inserted into any 16-bit ISA slot using an adapter. It can be reconfigured directly from the host computer to accelerate applications or to process data directly with supercomputer performance.

Figure 4 shows the Constellation board block diagram.

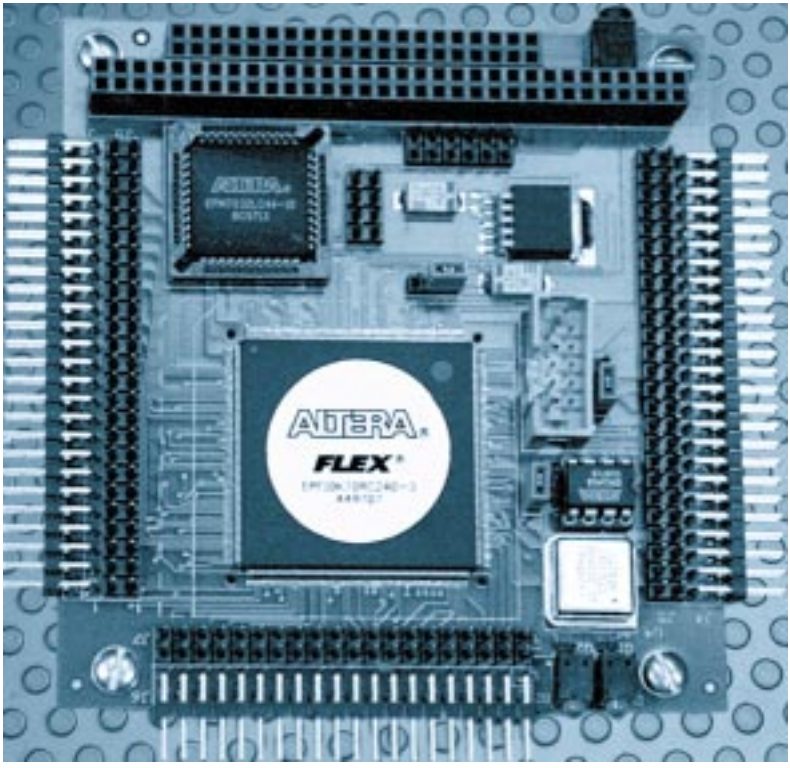
Figure 4. Constellation Board Block Diagram



Prototype Board

Figure 5 shows the Constellation prototype board.

Figure 5. Constellation Prototype Board



CPCI10K-PROD Prototyping Board

Vendor: PLD Applications
Target Application:
PCI

- Universal 5.0-V and 3.3-V CompactPCI board
- 32-bit and 64-bit PCI operation
- Operates on 33-MHz and 66-MHz CompactPCI bus
- Exists in two versions:
  - CompactPCI, full hot-swap compliant (PICMG, 2.1-R1.0) CPCI10K-PROD
  - Base version (cannot perform hot-swapping) CPCI10KNS-PROD
- Exists in two formats:
  - 3U
  - 6U
- One slot thick for each format and version
- Altera FLEX 10K device family (EPF10K30 to EPF10K200 devices) support, including independent power supply for device I/O pins (3.3 V) and core (2.5 V)
- Altera FLEX devices are available in 256-pin and 484-pin FineLine BGA™ packages
- Supports PLD Applications 32-bit and 64-bit PCI target and master/target interfaces
- All device I/O pins are available through four PMC connectors (176 I/O pins)
- PCI interface device configuration via two chained EPC2 devices or the Altera BitBlaster™ or ByteBlaster™ download cables (through the JTAG chain)
- External power supply connector for stand-alone use (off-CompactPCI)
- Power supply and configuration light-emitting diodes (LEDs)
- 2 x 7 segments LED displays
- Access up to 128 x 512 Kbits on board (optional) SRAM
- Supports basic, full- and high-availability hot swap models
- Injector/extractor micro switch
- Blue LED support
- Hot-swap register and ENUM# support
- Direct utilization of the 64EN# signal
- Customizable daughter board for additional D/A processes

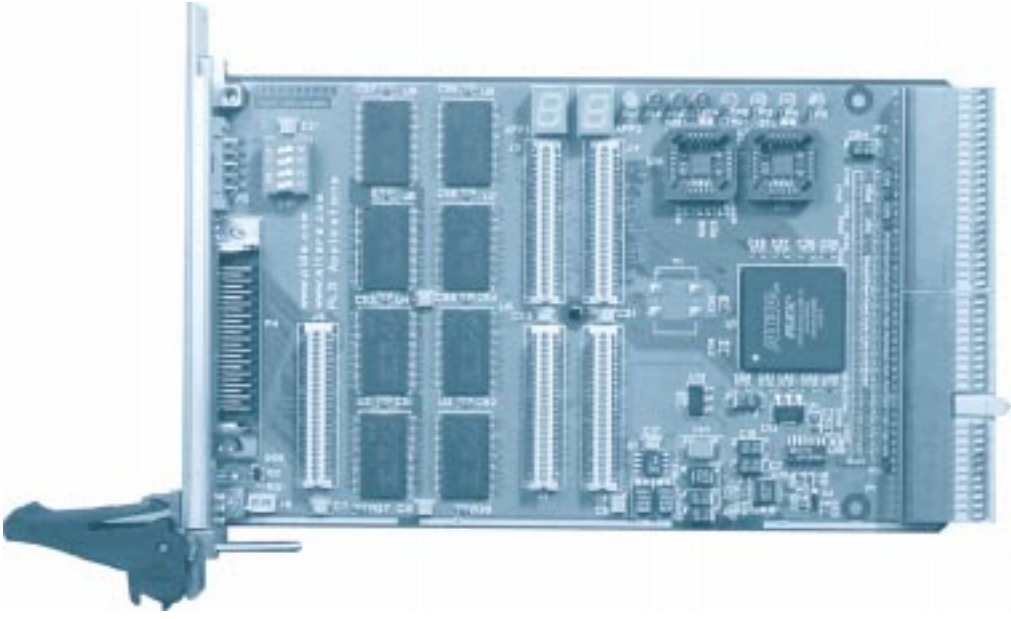
General Description

The CPCI10K-PROD prototyping board is used as a 5.0-V or 3.3-V, 32-bit or 64-bit, 33-MHz or 66-MHz CompactPCI development board, CompactPCI bus analyzer, data acquisition board, or full hot-swap CompactPCI platform design. The CPCI10K-PROD prototyping board refers to the standard full hot-swap capable version of the PLD Applications' CompactPCI boards, while the CPCI10KNS-PROD board refers to the base version of the CPCI10K-PROD board without hot-swap capability.

Prototype Board

Figure 6 shows the CPCI10K-PROD prototype board.

Figure 6. CPCI10K-PROD Prototype Board



PCI_GEN10K Prototype Board

Vendor: PLD Applications
Target Application:
PCI

- Universal 5.0-V/3.3-V, 32-bit/64-bit PCI board
- MultiVolt™ FLEX 10K device family-based (including FLEX 10KE devices), including independent power supply for device I/O pins and megafunction
- Supports PLD Applications' 32-bit/64-bit PCI target and master/target interfaces
- Additional FLEX 10K family print (QC240) on back-end side
- All device I/O pins available through side connectors
- PCI bus signals also available on side connector, allowing for PCI interfacing on daughter board
- PCI interface device configuration via two chained EPC2 devices per FLEX device or the Altera BitBlaster or ByteBlaster download cables (through JTAG chain)
- Back-end FLEX 10K device configurable from PCI interface device
- Access to two 72-pin SIMM connectors from PCI interface device
- External power supply connector for stand-alone use (off-PCI)
- Rear panel 50-pin connector print
- Power, configuration, and user LEDs

Altera Devices on Board

- FLEX 10K devices

General Description

The PCI_GEN10K MultiVolt prototyping board is used as a 5.0-V or 3.3-V, 32-bit or 64-bit PCI development board, or used as a generic development platform.

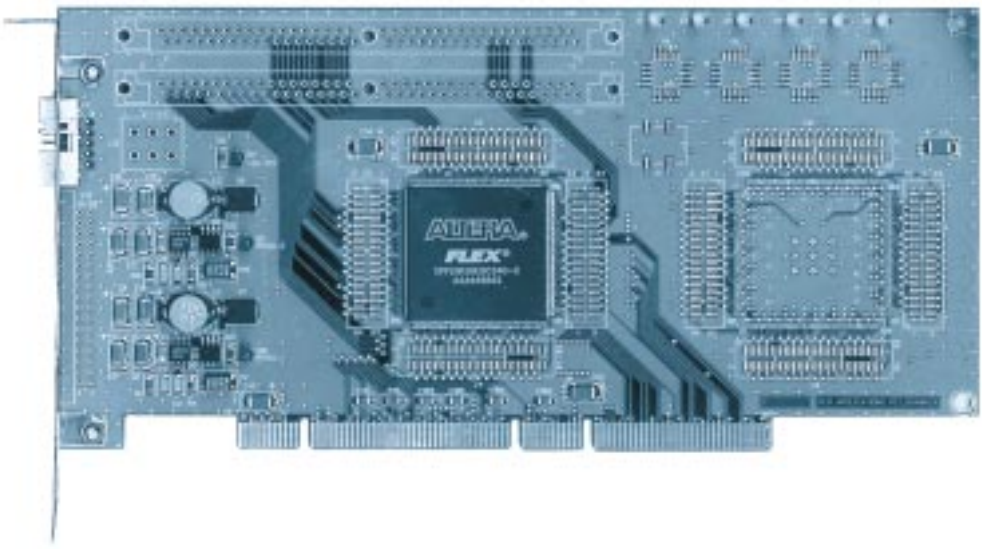
The PCI_GEN10K board is shipped with an evaluation version of PLD Applications' PCI target or master/target encrypted PCI megafunction. The user cannot modify the PCI megafunction high-level parameters but can still compile and simulate the megafunction along with its custom back-end application. The user can also configure the on-board device for immediate hardware testing. An auto-test back-end application is provided with the card. This application uses the FLEX 10K embedded array blocks (EABs) to implement an internal SRAM buffer.

A DOS, Windows 95, and WindowsNT driver and graphical user interface is also provided to easily access and monitor the card' s PCI resources.

Prototype Board

Figure 7 shows the PCI_GEN10K prototype board.

Figure 7. PCI_GEN10K Prototype Board



PCI_GEN6K Prototype Board

Vendor: PLD Applications
Target Application:
PCI

- Supports PLD Applications' PCI master/target interface megafunction
- Fully compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***
- Dual-device print (accepts 208-pin and 240-pin quad flat pack (QFP) packages)
- Two workspaces to implement user applications
- Two 93-pin connector prints to access all available I/O pins
- 144 user I/O pins (240-pin QFP packages) and 116 user I/O pins (208-pin QFP packages)
- PCI interface configuration via Altera EPC1/EPC1441 devices or the Altera BitBlaster or ByteBlaster download cables
- External power supply for stand-alone utilization
- One 50-pin rear panel connector print
- EMC compliant (ground plane, power plane, two signal planes)

Altera Devices on Board

- FLEX 6000 devices

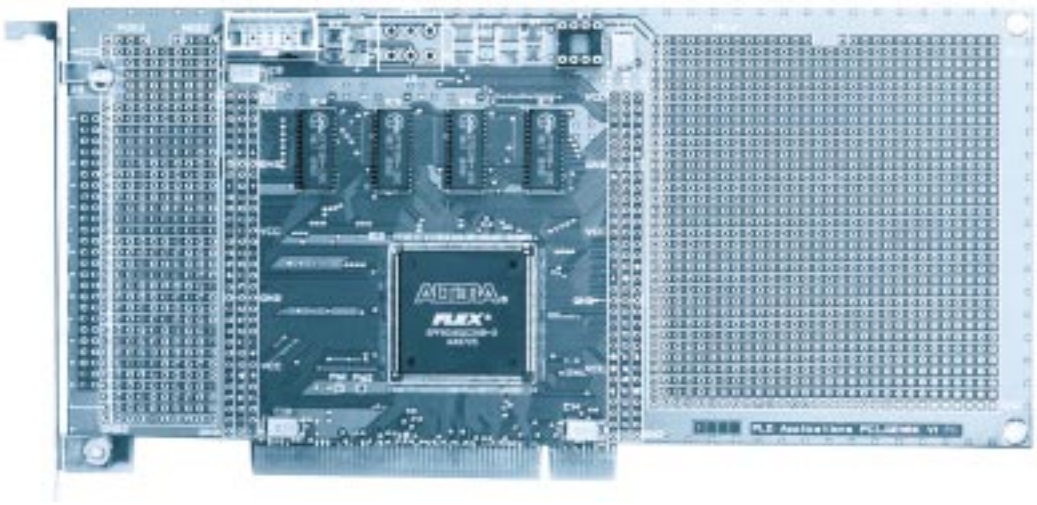
General Description

The PCI_GEN6K is a PCI prototyping board that allows rapid implementation of any PCI-based or PLD-based application. The PCI_GEN6K board is shipped with an evaluation version of PLD Applications' PCI target or master/target encrypted megafunction. The user cannot modify the PCI megafunction high-level parameters but can compile and simulate the megafunction along with its back-end application as well as configure the on-board device for immediate hardware testing. An auto-test back-end application is provided with the card. This application uses 4 × 32 Kbytes of on-board SRAM to implement an external 128-Kbyte buffer. A DOS, Windows 95, and WindowsNT driver and graphical user interface is also provided to easily access and monitor the card's PCI resources.

Prototype Board

Figure 8 shows the PCI_GEN6K prototype board.

Figure 8. CPCI_GEN6K Prototype Board



XT-1000 Device Emulation Kit

Vendor: Tensilica
Target Application: Prototyping, embedded systems

- One Altera EPF10K200E complex programmable logic device (CPLD)
- 256 Kbytes EPROM
- 1 Mbyte SRAM
- 2 Mbytes FLASH memory
- 2 Mbytes synchronous SRAM
- 2 RS-232 serial channels

Altera Devices On Board

- EPF10K200E device

General Description

The XT-1000 device emulation kit is a comprehensive, low-cost development tool developed jointly by Tensilica and Altera. It uses a CPLD to emulate (in hardware) a specific Xtensa processor configuration. This product enables you to evaluate various processor configuration options and start application software development and debugging on silicon early in the development cycle of your system-on-a-programmable-chip-based design. The XT-1000 allows the user to specify, implement, and debug a new processor configuration, including designer-defined instructions, in just hours.

A predefined external bus interface connects the Xtensa megafunction in the CPLD to the other emulation kit resources. The CPLD is configured by downloading the configuration data from programmable ROM located on the emulation board. Software development is supported by a resident monitor program (X-MON) that provides communications and debugging facilities. A serial port provides a communication link to a host computer for downloading and debugging programs.

Megalogic System 100 Development Board

Vendor: Princeton Technology Group
Target Application: Prototyping

Altera Devices On Board

- FLEX 10K devices

General Description

Princeton Technology Group announces the Megalogic System 100 development board, the first in a series of products created to facilitate the implementation and rapid prototyping of complex electronic systems. The board supports up to four Altera FLEX 10K CPLDs having a combined capacity of more than 1,000,000 usable gates, and the interconnectivity to allow them to perform as a single logic array.

In addition to its gate count, this product has other features including a PCI interface, a wealth of both I/O and functional expansion options, and software support. PCI bus compatibility allows configuration data to be downloaded to FLEX 10K devices on the board without any additional cables or programmers. The PCI bus can also transfer data to and from the board at 133 Mbps, making the System 100 ideal for use as a computer co-processor or real-time simulator.

The I/O ports on the Megalogic board include 80 general-purpose user-defined bits made available on four headers, allowing designers the means to communicate with or control external electronics. A separate set of I/O connectors is dedicated to application specific modules (ASMs). These modules are located on daughter cards attached to the System 100 board and are used to integrate A/D and D/A converters, memory, video interfaces, or other specialized analog or digital circuitry to the CPLDs. The ASMs extend the capability of the Megalogic system to completely implement a wide range of applications.

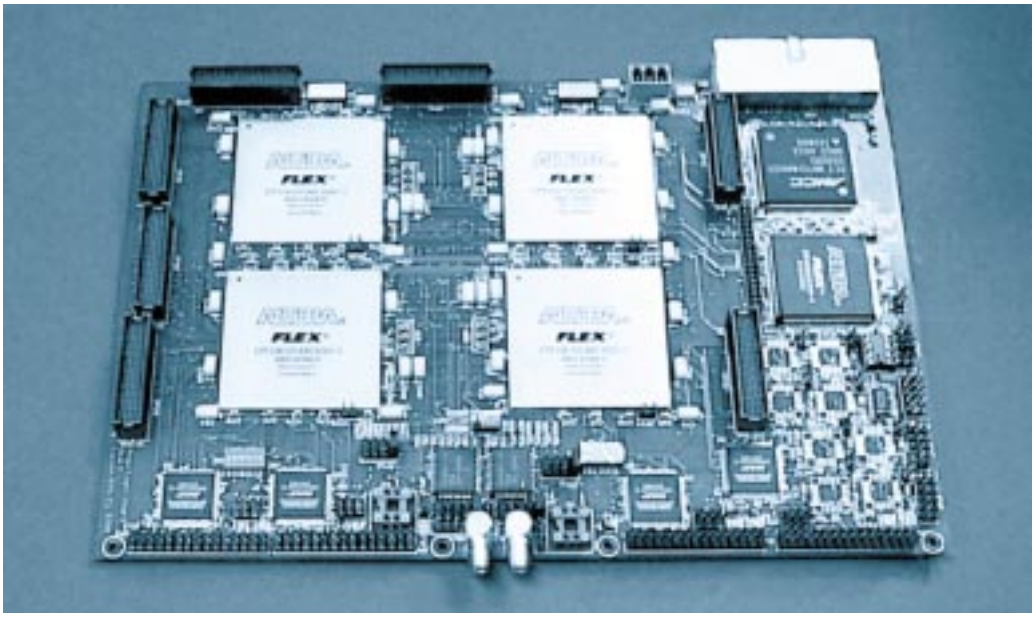
The software provided with the Megalogic board includes programs to support design partitioning into multiple CPLDs and downloading configuration data as well as AHDL libraries for high-speed PCI bus data transfers.

Overall, the Megalogic System 100 board can be an invaluable tool for system designers when used alone or in combination with standard or custom ASMs. Contact Princeton Technology to discuss how the System 100 development board can be used to your advantage.

Development Board

Figure 9 shows the Megalogic System 100 development board.

Figure 9. Megalogic System 100 Development Board



AMPP Partner Profiles

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Simple Silicon, Inc. 370
SIS Microelectronics, Inc. 371
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VAutomation 374

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Overview

An established leader in the design and development of embedded systems applications, Applied Microelectronics' technology and project management expertise help clients bring quality products to market quickly and cost effectively. Over the last 18 years, Applied Microelectronics has developed a wide variety of embedded systems incorporating field-programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), application-specific integrated circuits (ASICs), microcontrollers, multi-tasking real-time operating systems, digital signal processing (DSP) technology and high-performance digital boards. These systems have enabled companies such as AlliedSignal Corporation, Lockheed Martin Canada, General Dynamics, Nortel Networks, Newbridge Networks, Spar Aerospace, Com Dev Canada Ltd., and DY4 Systems to improve their product or service time-to-market.

Applied Microelectronics' design and development services incorporate FPGAs and CPLDs covering a broad range of applications such as:

- Telecommunications (ATM, UTOPIA, T1, E1)
- Communications (Reed-Solomon, Viterbi, FIR, IIR)
- Bus controllers (VME, VSB, PCI)
- Memory controller (DRAM, VRAM, SRAM, FIFO)
- Slave execution units (DMA, interrupt controllers, RTC, UART)
- Video (video effects, windowing, overlays)

Products

Applied Microelectronics provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	UTOPIA level 2: slave transmitter/receiver	124	_	Now
	UTOPIA level 2: master receiver	129	_	Now

Additional Services & Features

Applied Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore™ evaluation available
- ✓ Prototype/evaluation board

CAST, Inc.

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Overview

CAST, Inc. focuses on maximizing the success of programmable logic designs by supplying high-quality, high-value megafunctions for simulation and synthesis. CAST provides a total modeling solution for PLD design by delivering and supporting HDL libraries with thousands of accurate, reliable, and affordable functions ready for use by designers worldwide. CAST delivers the best available combination of up-front economy, long-term value, and personalized support.

Altera® MegaCore™ functions provide affordable VHDL and Verilog HDL megafunctions such as processors, peripherals, DSP functions, encryption, and specialized devices.

Products

CAST provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Viterbi decoder	33	Solution Brief 33	Now
Communications	High-level data link controller (HDLC)	104	–	Now

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor & peripheral	49410 microprogram controller	233	–	Now
	8051 microcontroller unit	235	–	Now
	2901 four-bit microprocessor slice	242	–	Now
	2910A microprogram controller	244	–	Now
	X_DES Cryptoprocessor	260	–	Now
	8251 programmable communications interface	271	–	Now
	8254 programmable interval timer/counter	273	–	Now
	8255A programmable peripheral interface	277	–	Now
	8259A programmable interrupt controller	282	–	Now
	29116A 16-bit microprocessor	284	–	Now
	16450 UART	311	–	Now
	16550 UART	313	–	Now
	6850 ACIA	315	–	Now
	UART	317	–	Now

Additional Services & Features

CAST provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board
- ✓ MegaWizard™ Plug-In

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http://www.coreel.com

Overview

CoreEl MicroSystems, Inc. is a leading provider of intellectual property (IP) in the areas of networking and telecommunications. The company has operations in Fremont, California and Pune, India, with over 80 employees. CoreEl provides feature-rich implementations that reduce overall system cost and greatly reduce time-to-market. CoreEl can provide a building block's register transfer language (RTL) code, along with its respective testbenches and synthesis scripts. Low-cost support for CoreCell customization, integration, integrated system validation, and turnkey solutions are also available. CoreEl takes pride in the quality of its design process, which includes RTL documentation, strict adherence of internal coding standards, bug tracking, and version control.

Products

CoreEl MicroSystems provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	UTOPIA level 2: master receiver	127	–	Now
	UTOPIA level 2: master transmitter	131	–	Now
	UTOPIA level 2: slave receiver	133	–	Now
	UTOPIA level 2: slave transmitter	135	–	Now
	10/100 Mbits fast ethernet media access controller receiver	137	–	Now
	10/100 Mbits fast ethernet media access controller transmitter	140	–	Now
	Cell delineation A	146	–	Now

Additional Services & Features

CoreEl MicroSystems provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board
- ✓ Hardware and software tools to host and monitor megafunctions

Eureka Technology, Inc.

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Los Altos, CA 94022
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Fax (650) 960-3805

info@eurekatech.com
http://www.eurekatech.com

Overview

Eureka Technology provides reusable IP cores for peripheral component interconnect (PCI) bus controllers, PowerPC bus controllers, and system core logic functions. Our reusable IP cores are silicon proven and pre-verified to meet and exceed customer requirements. They are designed to shorten time-to-market, eliminate design risks, and reduce development costs for our customers. Founded in 1993, Eureka Technology has been a design partner to many market leaders in the industry and has established a customer base in the United States, Japan, and Europe.

Products

Eureka Technology provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI & other bus interfaces	32-bit peripheral component interconnect (PCI) bus target interface	175	Solution Brief 6	Now
	32-bit PCI bus master/target interface	177	Solution Brief 19	Now
	64-bit PCI bus target interface	188	Solution Brief 6	Now
	64-bit PCI master/target interface	190	Solution Brief 19	Now
	PCI host bridge	192	–	Now
	PCI bus arbiter	194	–	Now
Processor & peripheral	SDRAM controller	288	–	Now
	Multi-function memory controller	292	–	Now
	DMA controller	296	–	Now
	PowerPC bus arbiter	298	–	Now
	PowerPC bus master	300	–	Now
	PowerPC bus slave	302	–	Now
	PowerPC to PCI host bridge	304	–	Now

Additional Services & Features

Eureka Technology provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board
- ✓ MegaWizard Plug-In

Innocor Ltd.

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info@innocor.com
http://www.innocor.com

Overview

Innocor Ltd. is a licenser and original equipment manufacturer (OEM) of datacom products. Innocor's IP solutions are easily tailored to fit their customers' embedded systems. Included in the Innocor portfolio are megafunctions which are designed, optimized, and marketed exclusively for Altera PLDs. Innocor also provides complete customer support and design consultation services.

Products

Innocor Ltd. provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	HDLC bit-oriented controller	108	–	Now
	Data encoder/decoder	110	–	Now
	Packet over SONET controller	112	–	Now
	ATM receive processor	114	–	Now
	SONET byte telecom bus interface	116	–	Now
Processor and peripheral	8259 programmable interrupt controller	280	–	Now
	Counter/timer	307	–	Now

Additional Services & Features

Contact Innocor, Inc. for additional services and features.

Integrated Silicon Systems

50 Malone Road
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Northern Ireland
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Fax +44 28 9050-4001
Sales:
Tel. (408) 441-1248
Fax (408) 441-1239

doug@iss-dsp.com
http://www.isp-dsp.com

Overview

Integrated Silicon Systems Ltd. (ISS) provides application-specific virtual components (ASVCs) for multimedia and communications System-on-a-Programmable-Chip™ integrated circuits. Using proprietary techniques for direct-mapped implementations of DSP functions and algorithms in hardware, ISS delivers solutions for wireless and wired communications, digital video, and digital imaging applications that realize 10× to 1,000× improvements in performance compared to conventional implementations using software-programmable DSP microprocessors.

Products

ISS provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Convolutional encoder	12	–	Now
	Reed-Solomon encoder	18	–	Now
	Reed-Solomon decoder	22	–	Now
	Viterbi decoder	35	–	Now
	DVB FEC codec	37	–	Now
	Cascadable adaptive finite impulse response (FIR) filter	49	–	Now
	FIR filter library	52	–	Now
	Infinite impulse response (IIR) filter library	53	Solution Brief 3	Now
	Rank order filter	55	–	Now
	Laplacian edge detector	57	–	Now
	QPSK equalizer	65	–	Now
	Fast Fourier transform/inverse fast Fourier transform (FFT/IFFT) high performance 64-point	78	–	Now
	FFT/IFFT low latency 64-point	80	–	Now
	Discrete cosine transform	87	Solution Brief 9	Now
	Multi-standard adaptive differential pulse code modulation (ADPCM)	89	Solution Brief 8	Now
	Image processing library	92	–	Now
	Floating-point operator library	93	–	Now

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	HDLC controller	106	–	Now
	Intermediate data rate (IDR) framer/deframer	149	Solution Brief 34	Now

Additional Services & Features

ISS provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board
- MegaWizard Plug-In

KTech Telecommunications, Inc.

15501 SF Mission Blvd.
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Mission Hills, CA 91345
Tel. (818) 361-2248
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skuh@ktechtelecom.com
http://www.ktechtelecom.com

Overview

KTech Telecommunications, Inc. is a design service company with experience in DSP functions designed for use in PLDs.

Products

KTech Telecommunications provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Convolutional interleaver	14	Solution Brief 16	Now

Additional Services & Features

KTech Telecommunications provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

NComm, Inc.

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Suite 204
Salem, NH 03079
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Fax (603) 893-6534

info@ncomm.com

Overview

NComm, Inc. (NCI) specializes in product development for telecommunications equipment. In addition to software technology, NCI offers a growing family of telecommunications products, including megafunctions optimized for Altera PLDs. NCI's PLD solutions provide high-quality telecommunication building blocks that accelerate product development and reduce overall system costs. NCI supplies maintenance and support programs as well as consulting services.

NCI's staff has developed telecommunication functions used in switching systems, transmission equipment, private branch exchanges (PBXs), intelligent peripherals, and video equipment.

If a telecom megafunction is not currently available, NCI can create custom megafunctions upon request. The experts at NCI can work closely with the design engineers to produce the exact megafunctions required.

Products

NComm provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	Telephony tone generation	118	Solution Brief 32	Now

Additional Services & Features

NComm provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Northwest Logic Design, Inc.

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Beaverton, OR 97006
Tel. (503) 533-5800
Fax (503) 533-5900

ip@nwlogic.com
http://www.nwlogic.com

Overview

Northwest Logic Design is a contract engineering design firm. Solid engineering practices and a focus on customer satisfaction allows Northwest Logic Design to achieve rapid growth throughout the Pacific Northwest and the Bay Area.

Northwest Logic Design specializes in high-speed and high-density programmable logic devices (PLDs), intellectual property (IP), board-level design, and embedded software. Their engineering team has successfully applied their expertise to a wide variety of applications including digital communications, telecommunications, digital video, and DSP.

Products

Northwest Logic Design provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor & peripheral	SDRAM controller	286	–	Now

Additional Services & Features

Northwest Logic Design provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Nova Engineering, Inc.

5 Circle Freeway Drive
Cincinnati, OH 45246-1105
Tel. (513) 860-3456
Fax (513) 860-3535

Info@nova-eng.com
http://www.nova-eng.com

Overview

Nova Engineering, Inc. specializes in the design and development of leading-edge communications and signal processing systems. Nova has comprehensive experience in military, government, and commercial electronics, with an emphasis on state-of-the-art digital communications systems. Nova's innovative solutions have resulted in numerous patents and a series of successfully deployed communications and signal processing systems.

Embedded real-time signal processing in PLDs plays a major role in virtually every Nova product. The signal processing techniques are as diverse as forward error correction (e.g., Base-Chadhuri-Hocquenghem (BCH), Reed-Solomon, and Nadler functions), Kalman filters, digital modulation/demodulation, and low-rate, toll-quality vocoders. Nova's experience in communication product design has led to rapid prototyping using VHDL and PLDs to take advantage of the value provided by PLDs and module re-use.

Products

Nova Engineering provides the functions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Dual-constraint length Viterbi decoder	31	–	Now
	Linear feedback shift register	42	Solution Brief 11	Now
	Binary pattern correlator	59	Solution Brief 18	Now
	Numerically controlled oscillator (NCO)	63	Solution Brief 5	Now
	Digital modulator	67	Solution Brief 10	Now
	Complex multiplier/mixer	70	Solution Brief 4	Now
	Early/late-gate symbol synchronizer	72	Solution Brief 17	Now
	Digital intermediate frequency (IF) receiver	95	–	Now

Additional Services & Features

Nova Engineering provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board
- MegaWizard Plug-In

Phoenix Technologies. Ltd.

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sales@vchips.com
http://www.phoenix.com

Overview

Phoenix Technologies is one of the original pioneers of standards-based semiconductor IP, and is the leading independent developer of silicon-proven connectivity cores and simulation models. Our standards-based, silicon-proven IP solutions for Ethernet, IEEE 1394, universal serial bus (USB), PCI, AGP, and IrDA deliver right-the-first-time performance. Phoenix's parameterized IP cores are architecture and technology independent, providing designers with maximum flexibility while ensuring OS compatibility and easy integration, and implement the VSIA's virtual component interface.

Cores from Phoenix Technologies are provided as heavily annotated synthesizable Verilog or VHDL RTL source code, which is configurable using the RapidScript parameterization interface. Phoenix's software stacks and drivers are modular by design to support OEM-specific requirements. The development of RTL source code of an IP core is only 20% of the total task. Phoenix's design validation methodology, firmware, documentation, training, interoperability testing, and user support provide a complete and robust solution.

Phoenix validates its cores to the company's proprietary test methodology, a CPU-intensive verification suite that tests at the system, random, and board level using millions of vectors. These pre-verified cores allow design teams to quickly incorporate standards-based connectivity functions that deliver right-the-first-time performance. Development cost and risk are reduced, design reliability is improved, and more time can be focused on the design's custom logic. Hardware development boards and interoperability confirmation provides additional validation.

Phoenix Technologies has over 300 customers and our cores have been silicon-proven in over 20 leading fabs, down to the 0.18-micron process geometry. IP solutions from Phoenix Technologies reduce product development costs, improve design reliability, ensure interoperability, and accelerate time-to-market.

Additional Services & Features

Phoenix provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

PLD Applications

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Overview

PLD Applications is an engineering company specialized in programmable logic-based electronic systems. As a member of the Premiere Altera Megafunctions Partners Program (AMPP℠), PLD Applications' main activity is the development of intellectual property (IP).

Over the past years, PLD Applications has focused on the PCI market, and has developed a strong competence in this field. Because PCI is still such a challenge for IP developers and EPLD/FPGA manufacturers, PLD Applications provides highly efficient, off-the-shelf PCI megafunctions that users can easily interface to and integrate into their designs. To make it even easier, PLD Applications also provides the hardware and software tools to host and monitor its megafunctions.

The key features for using PLD Applications PCI solutions are:

- Gate-level description of megafunctions ensuring maximum efficiency and full PCI compliance
- Easy-to-use and powerful PCI cores, allowing user-access to the PCI cores internal logic
- Complete PCI solution including megafunctions, hardware, software and consulting
- Full support exclusively from the IP designers
- Long permanence of PCI cores, through standard or custom license and maintenance agreements

PLD Applications megafunctions are implemented in working applications worldwide. The projects involved are of various types and sizes, including:

- Entirely new PCI designs
- Migration from old bus-based designs to PCI
- Migration of existing PCI designs to Altera PLD technology

Products

PLD Applications provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	Universal digital data acquisition megafunction	152	–	Now
PCI & other bus interfaces	32/64-bit PCI bus master/target interface	179	–	Now
	32/64-bit PCI bus target interface	184	–	Now

Additional Services & Features

PLD Applications provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Richard Watts Associates, Ltd.

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England
Tel. (44) 0 1525 372621
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coreinfo@evolution.co.uk
http://www.evolution-uk.com/rwa

Overview

Richard Watts Associates (RWA) specializes in designing MegaCell functions for PLDs, which help designers meet the goals of high performance, lower cost, and faster time-to-market. RWA has ten years of design experience with real-time embedded system software for many different processors and DSP devices, including the 8052 device. The company can also support customers in any form of product development.

RWA's functions are designed in VHDL, which makes them independent of EDA tools and processes. Individual functions are available as behavioral VHDL, dataflow VHDL, dataflow Verilog HDL, and process-optimized blocks. MegaCell functions are supplied with high-fault coverage test vectors.

All of RWA's MegaCell functions are fully synchronous and static designs. Modern design techniques have been used to enhance performance and reduce area. Many functions are supported with extra models to aid system design, such as in hardware and software co-simulation debuggers. All MegaCell designs can be customized by RWA or the designer.

Products

Richard Watts Associates provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral	RAW8051/8052	238	–	Now
	BareCore 8052-X	240	–	Now
	RISC805x microcontroller	248	–	Now

Additional Services & Features

Richard Watts Associates provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Sapien Design

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http://www.sapiendesign.com

Overview

Sapien Design offers standard IP products for PLDs. These products include USB synthesizable megafunctions and a USB simulation test environment. The megafunctions include a USB function controller and a host controller for embedded systems.

Products

Sapien Design provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI and other bus interfaces	USB function controller	214	Solution Brief 24	Now
	USB host controller	218	Solution Brief 28	Now

Additional Services & Features

Sapien Design provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

SICAN Microelectronics Corp.

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http://www.SICAN-micro.com

Overview

SICAN is one of the largest independent microelectronics design and technology licensing companies world-wide, specializing in communications, multimedia and networking applications. Founded in 1990, SICAN focuses its design projects around the integration of reusable core technology into customer-specific solutions to improve the quality of the designs as well as to accelerate their time-to-market.

DesignObjects are pre-designed soft cores implementing industry-standard functions required in a variety of designs. Licensing such technology in the form of soft cores gives the customer's design team the freedom to focus on the functionality that will set its design apart from the competition. The DesignObjects encompass a broad spectrum of technologies, including:

- Cryptographic Functions (DES, RSA, Hash)
- Bus Interfaces (IIC, PCI, 1394, SmartCard, CAN)
- Microcontrollers For Embedded Systems (8051, CAN, PIC, 4-bit RISC)
- ATM (AAL, Utopia)
- Audio and Video Coding Techniques (MPEG-2 Video and Audio, AC-3)
- Broadband Media Access (Reed-Solomon, Viterbi, HDLC, FEC, QAM, QPSK)

DesignObjects are delivered as an all-inclusive assembly of RTL source code or netlist, technical specifications, design specifications, test benches, synthesis scripts and application support. Some DesignObjects also include reference designs, application notes, and behavioral models. With these deliverables, SICAN offers the most comprehensive collection of support documentation available from an IP provider.

All of the cores have been developed by SICAN experts who are retained on staff in order to provide first-hand technical support for maximum efficiency. Although not all of these cores are currently available through Altera, additional information on DesignObjects can be obtained directly from SICAN.

Products

SICAN provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI & other bus interfaces	CAN bus	196	Solution Brief 22	Now
	Inter integrated circuit (IIC) master interface	204	Solution Brief 40	Now
	IIC slave interface	206	Solution Brief 39	Now
	Sony/Philips digital audio interface (input)	208	–	Now
	Sony/Philips digital audio interface (output)	210	–	Now
	Smart card interface (ICC)	212	–	Now
Processor & peripheral	DES-Core	258	–	Now

Additional Services & Features

SICAN Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Simple Silicon, Inc.

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Cupertino, CA 95014
Tel. (408) 873-2260
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info@simplesi.com

Overview

Simple Silicon, Inc. is a provider of leading-edge digital connectivity solutions for consumer electronics, computing, audio, video, and mass storage applications. Simple Silicon's products can dramatically shorten the time-to-market and ensure first-time silicon success for your PLD-based designs.

Simple Silicon makes reusable building blocks based upon the emerging bus standards of IEEE Std. 1394 and USB for key market segments. ASIC designers can use these functions as is inside their designs to create high-speed serial interfaces.

Products

Simple Silicon provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI & other bus interfaces	IEEE 1394 link layer controller	200	–	Now
	USB function controller	216	–	Now
	USB hub controller	220	–	Now

Additional Services & Features

Simple Silicon provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

SIS Microelectronics, Inc.

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Overview

SIS Microelectronics, Inc., a subsidiary of Aspec Technology, Inc., is a leader in chip integration and related professional services. Since 1982, SIS has developed the expertise in chip development that makes tomorrow's products a reality today. SIS excels when time-to-market, cost, and performance goals must all be met. The company's blend of technical expertise and program management, combined with a library of proven functional building blocks, forges strong partnerships with SIS customers and delivers consistent "first-time" working silicon.

SIS Microelectronics is founded on the principle that success in the electronics marketplace requires a partnership between the system designer and the chip manufacturer. SIS's proven team approach provides its partners with the equivalent of an "in-house" chip supplier, providing assistance for chip design and integration to companies requiring design support through the development process. SIS also works in partnerships to develop proprietary products for embedded applications in the laser printer, network, telecommunications, and mass storage markets.

Products

SIS Microelectronics provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI & other bus interfaces	IEEE 1394 bus FireFox link layer controller	198	Solution Brief 36	Now
	IEEE 1284 parallel slave interface	202	–	Now
	Speedbridge	224	Solution Brief 13	Now

Additional Services & Features

SIS Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Stargate Solutions, Inc.

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Suite 210
San Jose, CA 95131
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http://www.sgates.com

Overview

Since 1996, Stargate Solutions, Inc. has provided its customers with high-quality IP products in the areas of communications and consumer electronics. Led by pioneers in the communications industry, the Stargate Solutions technology team has experience in all areas of integrated circuit (IC) design, from architectural descriptions, to place, route, and emulation. Stargate Solutions currently markets proven, modular, reusable solutions for USB, IEEE Std. 1394, PCI, ethernet, and synchronous dynamic random access memory (SDRAM) applications.

Products

Stargate Solutions, Inc. provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Communications	10/100 Ethernet media access controller	143	–	Now
Processor & peripheral	SDRAM controller	290	–	Now

Additional Services & Features

Contact Stargate Solutions, Inc. for additional services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Tensilica, Inc.

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Nashua, NH 03063
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info@Vhq.tensilica.com
http://www.tensilica.com

Overview

Tensilica specializes in the development of application-specific microprocessor solutions for embedded systems. Tensilica was founded in 1997 by experts in the areas of microprocessor architecture, ASIC and very large-scale integration (VLSI) design, advanced software development, and electronic design automation (EDA). The company's goal is to create the world's first truly configurable and extensible microprocessor architecture and support environments, enabling embedded system designers to build the highest-quality products possible.

Tensilica currently employs over 50 engineers, and provides research, development, and customer support from offices located in Santa Clara, California; Waltham, Massachusetts; and Tokyo, Japan.

Products

Tensilica, Inc. provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor & peripheral	Xtensa 32-bit microprocessor	255	–	Now

Additional Services & Features

Contact Tensilica, Inc. for additional services and features.

VAutomation

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Tel. (603) 882-2282
Fax (603) 882-1587

ampp@Vautomation.com
http://www.vautomation.com

Overview

VAutomation's synthesizable HDL megafunctions provide designers with solid, stable, easy-to-use standard functions such as microprocessors or microperipherals. These functions allow the designer to concentrate on unique value-added features without re-inventing standard functions. Combining VAutomation megafunctions with other functional blocks and custom logic can produce systems-on-a-chip.

The designer can target VAutomation megafunctions for any architecture, including PLDs, ASICs, gate arrays, or standard cells, and a wide range of operating voltages and fabrication processes. VAutomation AMPP megafunctions are designed to allow prototyping in Altera PLDs and later migration to a custom device in a suitable target architecture.

VAutomation uses strictly synchronous HDL designs with D flipflops and logic gates that are reliable and easy to synthesize and analyze; feedback loops, multi-cycle paths, latches, and flipflop clear or set pins are not used. VAutomation megafunctions are available in both VHDL and Verilog HDL source codes. The cores come complete with verification and synthesis scripts.

Products

VAutomation provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
PCI and other bus interfaces	USB device and host controller (VUSB)	222	–	Now
Processor and peripheral	6502 microprocessor	246	–	Now
	8-µRISC	251	–	Now
	VZ80 microprocessor	253	–	Now

Additional Services & Features

VAutomation provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

ACAP Design Services

September 1999

ACAP Partners

The following table lists the ACAP partners and the services they provide.

Partner	Expertise					Offering
	DSP	Communications	Buses/Interfaces	Processors/Peripherals	Board Products	
Advanced Logical Design, Inc. 12280 Saratoga-Sunnyvale Rd. Suite 201 Saratoga, CA 95070 Tel. (408) 446-1004		✓	✓	✓	✓	Full-service system design and manufacturer of high-speed digital and microprocessor-based products.
Applied Computing Technology, Inc. 1020F Commerce Park Drive Oak Ridge, TN 37830 Tel. (423) 220-0777	✓		✓	✓		Customized test, measurement, and diagnostic electronic instrumentation development company that provides a full scope of services from idea, to design, to prototyping, to the final manufacturing stage. Applied Computing Technology uses its unique electronic design expertise for product miniaturization using state-of-the-art electronics.
Applied Microelectronics Inc. 1046 Barrington Street, Halifax Nova Scotia, Canada, B3H 2R1 Tel. (902) 421-1250	✓	✓	✓			Expertise in hardware and software design services for embedded systems, including custom IC development, board level systems, and product development.
BARCO SILEX Rue du Bosquet 7 1348 Louvain La Neuve Belgium Tel. (32) 10-45 49 04	✓		✓	✓		Provides a full-service design house with the following engineering capabilities: embedded functions, processors and peripherals/buses, interfaces, digital video and image processing, and digital signal processing (DSP) for digital filtering.

Partner	Expertise					Offering
	DSP	Communications	Buses/Interfaces	Processors/Peripherals	Board Products	
Bright Design Services 10436 NE 112th Street Seattle, WA 98033 Tel. (425) 576-1524	✓	✓			✓	Electrical engineering and system design consulting, specializing in video and image processing technologies.
Coded Solutions Pty Ltd 65 Johnston Street Annandale, NSW 2038 Australia Tel. (61) 2 9518 7011		✓	✓	✓		Digital design services, including software development and embedded microcontroller applications.
DesignPRO Inc. 35 Stafford Road, Unit 1 Nepean, Ontario, Canada, K2H 8V8 Tel. (613) 596-5030		✓	✓		✓	Full-service PLD/ASIC design organization, specializing in telecom/datacom applications, including PLD/ASIC design and verification, printed circuit board (PCB) design and testing, firmware and software development, and hardware and software integration and testing.
Digital Design Solutions 6696 Fossil Creek Dr. Memphis, TN 38120 Tel. (901) 759-1802	✓		✓	✓	✓	Specialize in design and development of embedded hardware and programmable logic.
DMC Manufacturing, Inc. 7025 Central Highway Pennsauken, NJ 08109 Tel. (609) 665-5400					✓	Full-service contract manufacturer providing engineering design, PCB design, prototyping, and volume manufacturing services.
Eberwein & Associates, Inc. 9449 Briar Forest, #507 Houston, TX 77063 Tel. (713)-784-1226	✓		✓	✓		Product development and turnkey systems
Gid'el Ltd. 14 Ein Ayyala Israel 30825 Tel. (972)-6639-1708 Email. **w_reuven@gidel.com**	✓	✓			✓	Provides time-saving technology with PROC 10K parallel development of software and hardware. Also provides consulting and turnkey.

Partner	Expertise					Offering
	DSP	Communications	Buses/Interfaces	Processors/Peripherals	Board Products	
Innovative Configuration, Inc. (ICI) 712 via Palo Alto Aptos, CA 95003 Tel. (831) 688-6917	✓	✓	✓		✓	Turnkey system design and prototyping; including design of algorithms, software, hardware, board layout, assembly, and test and packaging (PC-AT, VME, PC104)
Intrinsix 33 Lyman St. Westboro, MA 01581 Tel. (508) 836-4100	✓	✓	✓			Independent ASIC and systems design services company with design centers in 18 locations in the United States. Also, provides comprehensive FPGA, ASIC, embedded software development, and system verification services.
I/O Consulting A/S Gaaseagervej 6 DK-8250 Egaa Tel. (45) 87 43 80 74		✓		✓	✓	Independent research and development company specializing in electronic systems, hardware, and software.
Lewis Innovative Technologies, Inc. 11405 Alabama Highway 33 P.O. Box 624 Moulton, AL 35650 Tel. (256) 974-8931			✓	✓	✓	High-speed timing and control systems, High-speed arithmetic functions, board level and turnkey product design, and complete design of electronic components.
Locke's Digital Developments Ltd. & New Offices, New Street, Marnhull, Dorset, England. DT10 1PY Tel. (44) 0 1258 821 222	✓	✓	✓			Electronic design services, including PLD design, board-level design, and software development
Mettrix Technology Corporation 25 Corporate Park Drive, Suite C Hopewell Junction, NY 12533 Tel. (914) 897-4960		✓	✓	✓	✓	Full-service electronic product development company, including custom/ASIC design, board layout, prototyping, software development, and small scale manufacturing.
Northwest Logic Design, Inc. 1905 NW 169th Place, Suite 121 Beaverton, OR 97006 Tel. (503) 533-5800	✓	✓	✓	✓		Contract engineering design company specializing in programmable logic, board-level design, and intellectual property (IP) development.

Partner	Expertise					Offering
	DSP	Communications	Buses/Interfaces	Processors/Peripherals	Board Products	
Norton Engineering Consultants 2307 Damuth Street Oakland, CA 94602 Tel. (510) 482-1818		✓				System architecture, design and concept-to-product development for high-speed networks, datacom, and telecom applications.
Nova Electronic Design & Analysis Corporation 459B Carlisle Drive Herndon, VA 20170 Tel. (703) 618-2877		✓		✓	✓	FPGA/board design and simulation; transmission line simulation for high speed boards and backplanes.
Plandscapes, Inc. 101 Kingland Dr. Stow, MA 01775 Tel. (978) 562-6462	✓		✓	✓	✓	Providing contract design services ranging from design specification to finished product for over 10 years. Also, offers consulting and systems analysis services, on- and off-site engineering support, and system architecture design
Prodrive B.V. Scienc Park 5025, Postbus 28030 5602 JA Eindhoven The Netherlands Tel. (31) 40 2676200	✓				✓	Engineering company that designs according to customer requirement. Supplier of basic building blocks.
RPA Electronics Design, LLC 1285 Chenango Street Binghamton, NY 13901 Tel. (607) 771-0393	✓		✓	✓	✓	Full-service systems design house, including system design, circuit design, board-level hardware and software development, and prototype fabrication and test services.
RTI 10560 Main St., Ste. 417 Fairfax, VA Web. **http://www.rti-world.com** Tel. (703) 293-9662	✓	✓		✓	✓	Specialize in embedded and distributed real-time hardware and software development on numerous mainstream platforms and languages.
Sam Lowenstein & Associates 118 Melody Lane, SW Vienna, VA 22180 Tel. (703) 724-2082	✓	✓				Full-service multimedia design house, including software development and standards compliance services.

Partner	Expertise					Offering
	DSP	Communications	Buses/Interfaces	Processors/Peripherals	Board Products	
SyncAccess, Inc. 5279 Folsom Blvd. Sacramento, CA 95819 Web. **http://www.syncaccess.com** Tel. (916) 457-4838 Fax. (916) 456-8505		✓	✓		✓	Provider of innovative solutions for high-speed networking, computing and cryptographic systems by applying exceptional design services and products.
Szabo Electronic Systems 40 Purvis Street Watertown, MA 02472 Tel. (617) 924-0618	✓		✓	✓		Comprehensive design and consultation services. Significant video, CCD, embedded systems, and DSP experience. C, C++, and assembly-level software development.
Tantau Australia P.O. Box 1232, Lane Cove 1595 Sydney, Australia Tel. (44) 02 9555 9375				✓		Hardware and embedded software projects based on microcontrollers, DSPs, and Altera® complex programmable logic devices (CPLDs).
Vulcan ASIC Ltd., Unit 6, The Maltings, Royston, Herts, SG8 5DY, England Tel. (44) 0 1763 248163	✓	✓	✓	✓		Engineering and consulting services, IP supply and integration.

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September 1999

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Abbreviations

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ACIA	Asynchronous communications interface adapter
ADC	Analog-to-digital converter
ADV	Analysis, design, and verification
ADPCM	Adaptive differential pulse code modulation
AGP	Accelerated graphics port
AHDL	Altera Hardware Description Language
ALU	Arithmetic logic unit
AM	Amplitude modulation
AMPP	Altera Megafunction Partners Program
ASIC	Application-specific integrated circuit
ASK	Amplitude shift keying
ASSP	Application-specific standard product
ATM	Asynchronous transfer mode
AWT	Adaptive wavelet transform
BAR	Base address register
BCD	Binary coded decimal
BCH	Binary coded hexadecimal
BCT	Binary coded ternary
BIST	Built-in self-test
CAD	Computer-aided design
CAN	Controller area network
CCITT	International Telegraph and Telephone Consultation Committee
CODEC	Coder/decoder
CPLD	Complex programmable logic device
CPM	Continuous phase modulation
CPU	Central processing unit
CRC	Cyclic redundancy code
DAB	Digital audio broadcast
DAC	Digital-to-analog converter
DCME	Digital circuit multiplication equipment
DCT	Discrete cosine transform
DDS	Direct digital synthesis
DFT	Discrete Fourier transform
DIF	Decimation in frequency
DMA	Direct-memory access
DRAM	Dynamic random access memory
DSP	Digital signal processing
DSS	Digital satellite system
DSSS	Direct sequence spread spectrum

DUT	Device under test
DVB	Digital video broadcast
EAB	Embedded array block
ECC	Error correction coding
ECL	Emitter-coupled logic
ECP	Extended capabilities port
EDA	Electronic design automation
EEPROM	Electrically erasable programmable read-only memory
EISA	Extended industry-standard architecture
ESC	Engineering service circuits
ETS	European Telecommunication Standards
DCME	Digital circuit multiplication equipment
DES	Data encryption standard
FEC	Forward error correction
FFT	Fast Fourier transform
FIFO	First-in first-out
FIR	Finite impulse response
FLEX	Flexible Logic Element MatriX
FM	Frequency modulation
FSK	Frequency shift keying
GUI	Graphical user interface
HDL	Hardware description language
HDLC	High-level data link controller
HEC	Header error control
IC	Integrated circuit
ICR	In-circuit reconfigurability
IDCT	Inverse discrete cosine transform
IIC	Inter integrated circuit
IP	Intellectual property
IEEE	Institute of Electrical and Electronic Engineers
IIR	Infinite impulse response
I/O	Input/output
ISA	Industry-standard architecture
ISI	Inter-symbol interference
ISP	In-system programmability
ITU	International Telegraphy Union
ISDN	Integrated services digital network
JPEG	Joint Photographic Experts Group
LAN	Local-area network
LFSR	Linear feedback shift register
LIFO	Last-in first-out
LMS	Least-mean square
LSB	Least significant bit
LUT	Look-up table
MAC	Multiplier-accumulator
MAX	Multiple Array MatriX
MCU	Microcontroller unit

MIDI	Musical instrument digital interface
MOR	Models on request
MPEG	Motion Pictures Expert Group
MSB	Most significant bit
NCO	Numerically controlled oscillator
NRZ	Non-return-to-zero
OAM	Operation and maintenance
OEM	Original equipment manufacturer
PBX	Private branch exchange
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCI-SIG	Peripheral component interconnect Special Interest Group
PCM	Pulse-code modulation
PCMCIA	Personal computer memory card international association
PCS	Personal communications system
PHY	Physical layer
PID	Proportional-integral-derivative
PLD	Programmable logic device
PLL	Phase-locked loop
PN	Pseudo-random number
POTS	Plain old telephone service
PPI	Programmable peripheral interface
PSK	Phase shift keying
PVP	Packetized voice protocol
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RAM	Random access memory
RAMDAC	Random access memory digital-to-analog converter
RF	Radio frequency
RISC	Reduced instruction set computing
RLE	Run, length encoding
ROM	Read-only memory
RTL	Register transfer level
SCVL	Standard component VHDL library
SIG	Special interest group
SRAM	Static random access memory
TCM	Trellis coded modulation
TTL	Transistor-to-transistor logic
UART	Universal asynchronous receiver/transmitter
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
UTOPIA	Universal xxx and operations physical interface for ATM
VME	Versa module eurocard
VLSI	Very large-scale integration
WAN	Wide-area network
XMIDI	Extended musical instrument digital interface