clklock (Phase-Locked Loop)

Parameterized Phase-Locked Loop Megafunction

The `clklock` megafunction enables phase-locked loop, or ClockLock, circuitry available on selected ACEX 1K and FLEX 10K devices. The `clklock` megafunction can reduce Clock delay and skew and can be used to generate internal Clocks that operate at frequencies equal to or twice the frequency of the system Clock. The `clklock` megafunction can also improve setup and hold times. Once `clklock` is locked onto the Clock, it generates a Clock signal which appears to have a negative delay with respect to the incoming Clock. The negative delay is designed to approximate the delay from `clklock` to the register, thus minimizing the apparent delay from the Clock pin to the register. For ACEX 1K and FLEX 10K devices, Altera recommends using the `clklock` megafunction rather than the `pll` megafunction.

You can use the **genclk** utility to create a simulation model for this function for use in third-party simulators. Type `genclk -h` ↵ at a DOS or UNIX prompt for information on how to use this utility.

AHDL Function Prototype (port name and order also apply to Verilog HDL):

```
FUNCTION clklock (inclk)
   WITH (CLOCKBOOST, INPUT_FREQUENCY)
   RETURNS (outclk);
```

VHDL Component Declaration:

```
COMPONENT clklock
   GENERIC (INPUT_FREQUENCY: POSITIVE;
      CLOCKBOOST: POSITIVE);
   PORT (inclk: IN STD_LOGIC;
      outclk: OUT STD_LOGIC);
END COMPONENT;
```

Ports:

INPUTS

Port Name	Description

inclk	Clock input to ClockLock circuit.

OUTPUTS

Port Name	Description
outclk	Clock output from ClockLock circuit.

Parameters:

Parameter	Type	Required	Description
CLOCKBOOST	Integer	Yes	Multiplier factor used to determine how much faster the outclk port should be than the inclk port; e.g., to indicate a 2x Clock, specify 2. The CLOCKBOOST parameter takes advantage of the ClockBoost circuitry available in some ACEX 1K and FLEX 10K devices. Legal CLOCKBOOST values for ACEX 1K and FLEX 10K devices are 1 and 2.
INPUT_FREQUENCY	String	Yes	Time value in MHz. Estimated frequency of the Clock at the inclk input to the clklock function; e.g., to indicate a 50-MHz estimated frequency, specify 50. You may also specify an "UNUSED" value.

The clklock megafunction automatically uses one of the two global Clock pins on the device to implement the ClockLock. The following rules apply to clklock megafunctions:

- A clklock megafunction must be fed directly by a dedicated input pin, which can feed only other clklock megafunctions that have the same INPUT_FREQUENCY value.
- Multiple clklock megafunctions with the same CLOCKBOOST parameter values are merged.
- A clklock megafunction can feed only the Clock inputs to registers (including lpm_ff and lpm_latch) or RAM functions. No inversion or other logic is permitted between the clklock output and the register or RAM Clock inputs.
- You can simultaneously use both single (1x) and double (2x) Clock frequencies. Both global signals can be driven from the same global Clock pin, with both 1x and 2x Clocks locked. To implement this feature, instantiate two clklock megafunctions, one with a CLOCKBOOST parameter value of 1, the other with a CLOCKBOOST parameter value of 2.

You can also implement a design with a single locked Clock by turning on the *CLKLOCKx1 Input Freq* logic option on an input pin instead of instantiating a `clklock` megafunction with a `CLOCKBOOST` parameter value of 1.

See also:

Megafunctions/LPM